

Thermal System Identification Analyses of Chip Interconnects To Facilitate DVFS Implementation

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Abstract

With each advancing generation of process technology, the CPU power continues to rise, creating additional issues for thermal/mechanical packaging design. A common theme in next-generation CPU offerings will be the use of Dynamic Voltage and Frequency Scaling (DVFS) to manage the chip power during operation. With a DVFS policy, it becomes all the more important to study the potential impacts of imposed temporal variation in power on the thermo-mechanical reliability. In this study, we demonstrate a system identification approach for a practical CPU application and exemplify the trade-offs involved in creating a DVFS policy that is satisfactory to both thermal/mechanical reliability engineers and CPU design teams.

Keywords

DVFS, thermo-mechanical reliability, power fluctuations

1. Introduction

In high performance computing, the use of multi-core processors featuring hardware threading is becoming more common. These advanced microprocessors are used in high end servers that perform intensive data manipulation, graphical visualization and floating point computations.

As transistor technology evolves and gate lithography shrinks, chip power has continued to rise, and in particular the contribution of static leakage power to the total chip power continues to grow. Since the dynamic power (ie switching power) dissipated by a silicon chip is proportional to the square of the supply voltage and the frequency, a common theme to manage power in high end applications is through so-called Dynamic Voltage and Frequency Scaling, or DVFS [1,2].

In normal die operation, the heat transferred from the chip to the ambient manifests in a temperature field in the cooling solution, and also in the hardware attached to the cooling solution- i.e. the boards to which the chip package is attached, the electrical interconnect (socket) and so on (Fig. 1). With a DVFS policy in place the temperatures of the solder joints in the connector/socket are likely to be influenced; and the fluctuating temperatures are likely to cause aging of the solder joints, reduced connector life and ultimately the failure of the interconnect.

In this study we use identification methods to obtain dynamic models for the thermal response of flip-chip packages to power transients, and use the system models to correlate DVFS with thermal

behavior of packages, and ultimately package connector reliability.

2. Methodology

To mimic the behavior of a real CPU module (Fig. 1), a test vehicle was designed with a thermal test package containing a die of comparable dimensions as the real microprocessor. The stackup of materials in the package and module board were identical to those in the real application, and the assembly was done using identical processes and equipment to ensure consistency of findings. Nine locations of interest in the 3rd level interconnect region were identified, and thermocouples were attached. A production-quality heatsink was attached to the package using a commercially available thermal grease. The sink had a thermocouple embedded in its base to record the sink temperature. Temperatures onboard the silicon die were read using an array of embedded thermal diodes.

A step load of 100W was applied to the thermal test die, and the corresponding temperatures of the interconnect, silicon junction, and heatsink were recorded in real time.

3. Model Identification

Multiple techniques exist in the literature to obtain linear, time-invariant, causal SIMO (Single Input Multi Output) system models [3-7]. In this study the approach of Sinha and Lastman [7] was used to determine the transfer functions $H_i(s)$ from the applied power input to each of the connector,

CPU junction and sink temperatures.

Figures 2-4 show the Bode plot for the CPU junction, heatsink and a selected interconnect temperature respectively. A Bode plot shows the magnitude and phase characteristics of the transfer function of a variable of interest (e.g. temperature, speed etc.) in response to applied input(s). The frequency of the input signal's excitation is plotted on the x-axis, and the magnitude/phase of the transfer function is plotted on the y-axis. For simplicity, only the magnitude of the Bode plots are presented here.

4. Interpretation

The easiest way to read a Bode plot is by considering a 'step' application of the load (or input power as in this case). For the CPU junction, the power normalized temperature rise noted in the experimental testing was 0.179 C/W. Now looking at Fig. 2, the left asymptote (which corresponds to quasi static or low frequency loading, i.e. a step application of power) has a value of -14.95. Since Bode plots are made using decibel scales, we have

$$20 \log_{10}(G) = -14.95 \quad (i)$$

where G is the magnitude of the transfer function at that frequency. Solving (i) shows that G is 0.179C/W, so that the rise in CPU temperature will be 17.9 C if the applied power has a 100W magnitude.

The physical interpretation of Bode plots such as the ones in Figs. 2-4 are then straightforward, based on the preceding explanation. As the frequency of the 'excitation' (applied power) increases, the 'response' enters a transition zone where it reduces, and then stays flattened. At such (high) frequencies of excitation (power fluctuation), there is hardly any response (power normalized temperature rise) for each of the CPU junction, heatsink and the interconnect. At that point, the power fluctuation is so rapid that the system (CPU junction, interconnect, or sink) does not respond at all. As an illustration, consider a power fluctuation at 100Hz. As the CPU junction temperature Bode plot (Fig. 2) shows, the response spectrum magnitude for a 100Hz excitation is -70 dB. The corresponding power normalized temperature rise is

$$G = 10^{(-70/20)} = 0.00032 \text{ C/W}$$

So if the magnitude of the power is 100W, this would result in a $100 \times 0.00032 = 0.032 \text{ C}$ rise in the CPU temperature! It is noteworthy to compare this with the 17.9 C temperature rise alluded to earlier.

4. Predictions

The system models can be used to assess the impact of a DVFS policy on the CPU junction, heatsink and interconnect temperatures. In turn, the estimated interconnect temperatures may be fed into

a detailed solder joint reliability modeling study to assess the connector life.

As an example of a hypothetical DVFS policy, Figures 5 and 6 show potential power fluctuations in the CPU- at (low) 0.001 Hz and (high) 0.25 Hz respectively.

Figures 7 & 8 show the response of the CPU junction temperature to the power fluctuation in Figs. 5 and 6 respectively. Parallel responses for the heatsink temperature appear in Figs 9 & 10, and those for the interconnect in Figs. 11 & 12 respectively.

Figure 13 shows a "realistic" profile of a CPU power transient as an illustrative example. The corresponding Fourier spectrum, showing the frequency content of the power transient appears in Fig. 14. The thermal responses of the CPU junction, heatsink and selected interconnect thermocouple are shown in Figs. 15-17, and may be fed into a solder joint reliability study to evaluate possible impacts.

5. Conclusions

In this study we have demonstrated the use of rigorous system identification analyses to characterize transient system thermal responses (CPU junction, heatsink, interconnects) to applied CPU power fluctuations. Our study shows that high frequency excitations have little effect on the junction/sink/interconnect temperature rise. By applying the methodology outlined here, chip design teams and thermal/reliability engineers can collaboratively identify opportunities to implement a DVFS policy without compromising either thermal or mechanical reliability.

6. References

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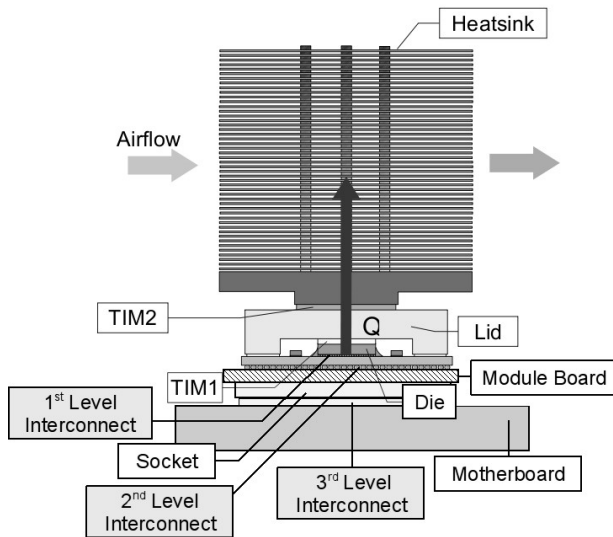


Fig. 1 CPU Cooling & Interconnect Scheme

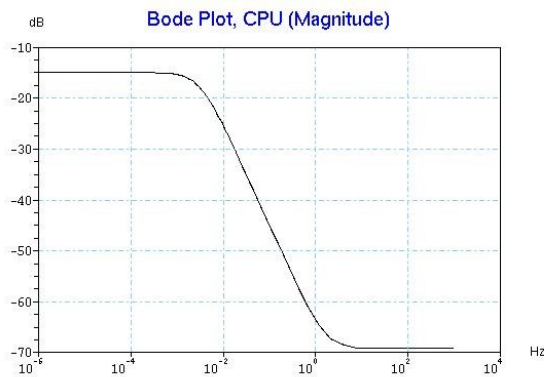


Fig 2. CPU Temperature Frequency Response

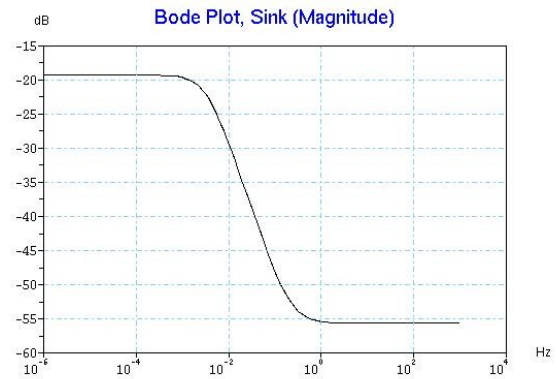


Fig. 3. Heatsink Temperature Frequency Response

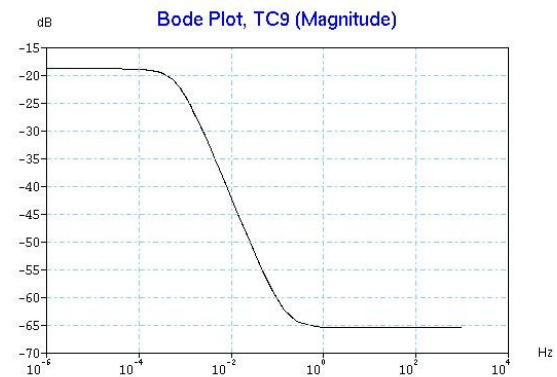


Fig. 4. Interconnect Temperature Frequency Response

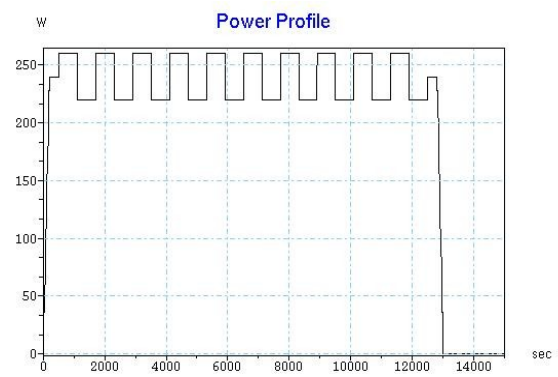


Fig. 5. 'Low Frequency' Excitation Model

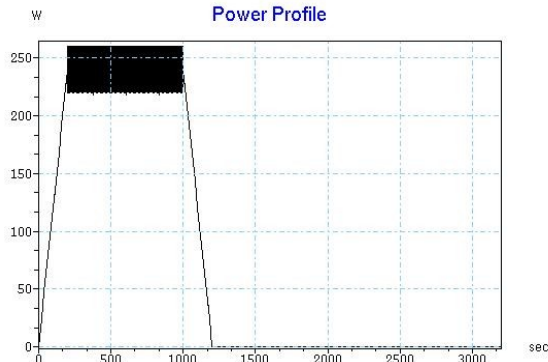


Fig. 6. 'High Frequency' Excitation Model

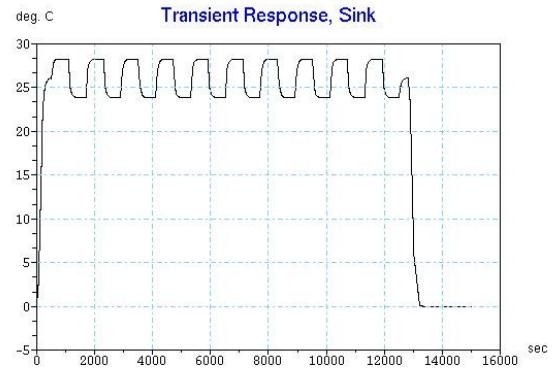


Fig. 9. Heatsink Temperature Response to 'Low' Frequency Power Fluctuation

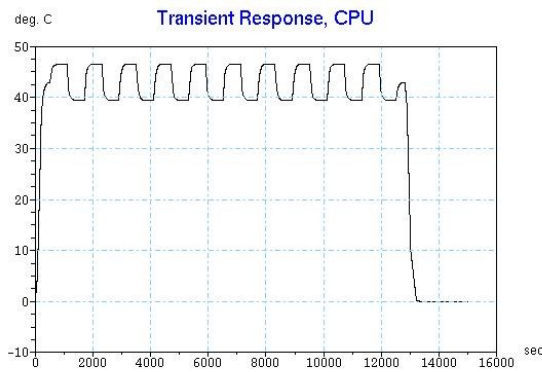


Fig. 7. CPU Junction Temperature Response to 'Low' Frequency Power Fluctuation

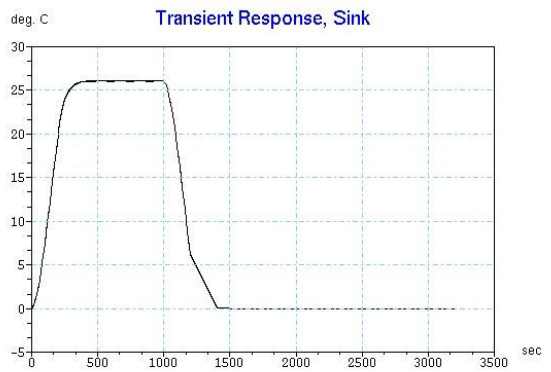


Fig. 10. Heatsink Temperature Response to 'High' Frequency Power Fluctuation

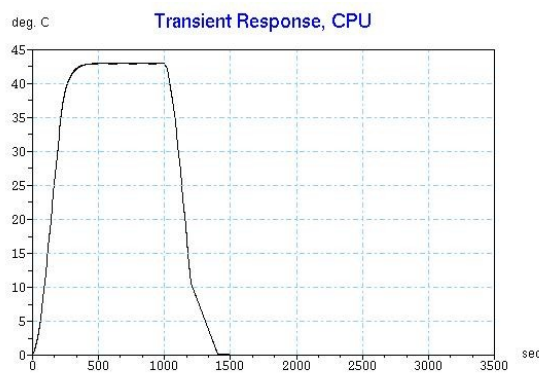


Fig. 8. CPU Junction Temperature Response to 'High' Frequency Power Fluctuation

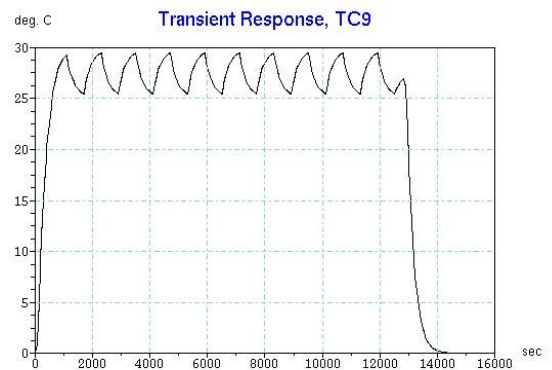


Fig. 11. Interconnect Temperature Response to 'Low' Frequency Power Fluctuation

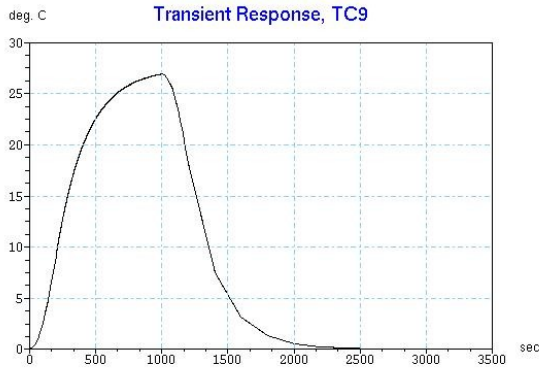


Fig. 12. Interconnect Temperature Response to 'High' Frequency Power Fluctuation

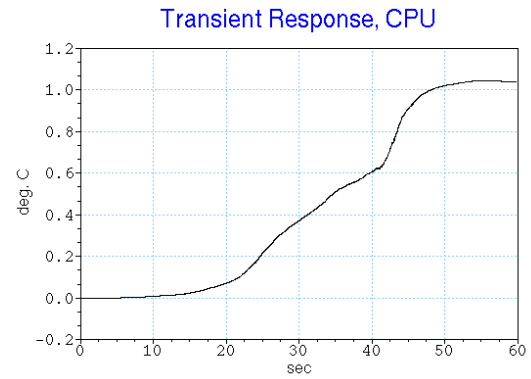


Fig. 15. CPU transient response to “realistic” power profile

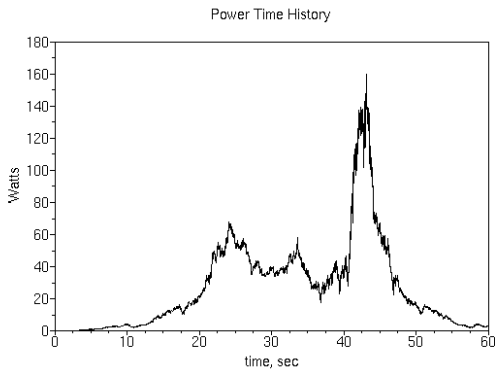


Fig. 13. “Realistic” Power Profile

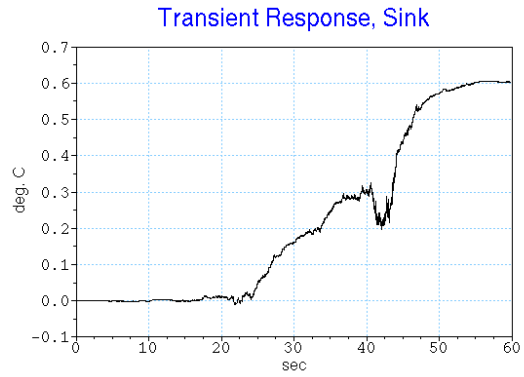


Fig. 16. Sink transient response to “realistic” power profile

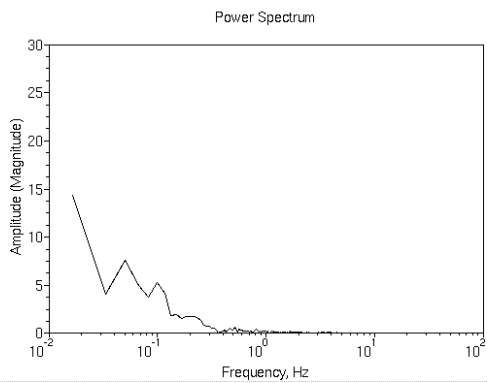


Fig. 14. Fourier spectrum for “realistic” power profile

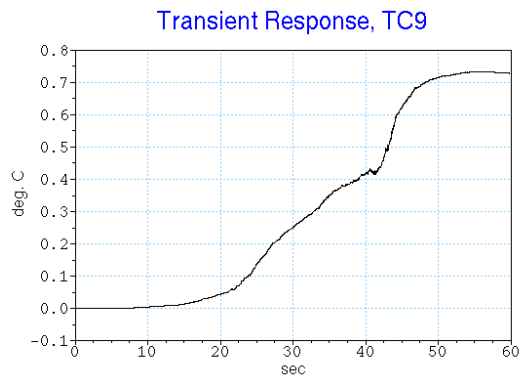


Fig. 17. Interconnect thermal response to “realistic” power profile