

A novel green process to manufacture ultra high density packaging substrates

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Abstract

Regarding green manufacturing, the production of PCB & IC substrate leaves a lot of issues in waste management. Not only in production line setting-up but also in routine operation, the management costs of hazardous chemicals and poison wastes in the processes of PCB & IC substrate are huge. In this paper, we disclose an efficient production process which requires the least kind of chemicals and can recycle most of the solvent. Regarding the details, we integrate 3 evolutionary processes in manufacturing of packaging substrate: metal lift-off, temporary wafer bonding and spin-on dielectric layer. In a pilot operation, the complete process of packaging substrates only requires 3 chemicals excluding a photoresist and a dielectric material. Despite improving the waste issues, our substrates still have excellent performance. Regarding high density routing, our substrate can fan out 3-rows flip chip bump array of 105 μm pitch in just one routing layer. It is much ahead of ITRS roadmap. In addition, thin thickness is another characteristic of our substrates. In a real case, the thickness of our 8-layer packaging substrates is just 90 μm . It is much thinner than the conventional packaging substrates. With the light and thin characteristics, therefore, our substrates can provide a lot of benefit for packaging of electronics

Key words: packaging substrate, green process, high density, metal lift-off

Overview of PCB process

The function of IC substrates and printed circuit boards (PCBs) is an interposer. Regarding their structures, they are multi-layer interconnections and used for electric connections between each component. Regarding their functions, IC substrates are the interposers of first-level packaging and PCBs are the interposers of second-level packaging. In order to analyze their structures further, we can distinguish them into 3 components: metal traces, dielectric layers and VIAs. In this article, we analyze the sub-structures of IC substrates and offer a novel

process to manufacture IC substrates and PCBs. This novel technology can simplify manufacturing process and reduce process materials. Additionally, it can increase routing density and decrease the thickness. This technology is environment-friendly and can produce high performance products.

Metal process

Conventionally, metal traces are made by etching process or semi-additive process. The etching process is shown in Figure.1. First, a metal layer is provided. Next, a photoresist pattern is made on the metal layer for the mask in etching process. Then,

etching solution is used to remove parts of the metal to form patterns. Finally, the photoresist is removed and the process is finished. In the etching process, four kinds of chemicals, including photoresist, developing solutions, etching solutions and photoresist stripping solutions are required and many waste etching solutions containing harmful copper ions will be generated.

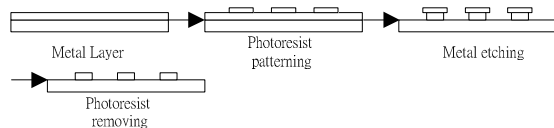


Figure.1 Metal etching process

Regarding semi-additive process, the process flow is shown in Figure.2. First, a seed layer is made on the substrate surface. Next, photoresist patterns are made on the seed layer for the mask in plating process. Then, metal patterns are made by an electro-plating process. After that, the photoresist is removed by photoresist stripping solution. Finally, the seed layer is removed by etching process. The semi-additive process is more complex. It requires five chemicals, including photoresist, developing solutions, electro-plating solutions, etching solutions and photoresist stripping solutions and inevitably generates much harmful chemical waste in plating and etching processes.

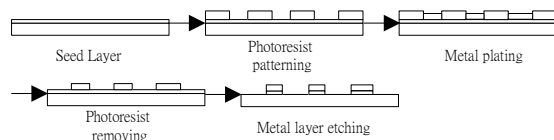


Figure.2 Semi-additive process

In this paper, we use metal lift-off process. Its process is shown in Figure.3. First, we make photoresist patterns for the mask of metal deposition. Next, we deposit a metal film on the substrate by

physical vapor deposition. Finally, we remove the photoresist and the metal film on the photoresist. So that, the metal film attached on the substrate is left and the metal patterns are done. One merit of this process is less consumption of chemicals. In the metal lift-off process, only three kinds of chemicals are required, including photoresist, developing solutions and photoresist stripping solutions. All of these materials are ordinary. For example, our photoresist are normal negative type photoresist, and the developing solution is common alkali solution. Even the photoresist stripping solutions, we choose an ordinary organic solvent. We never use any hazardous chemicals. Moreover, in our metal lift-off process, the photoresist stripping solutions can be recycled and reused and generate less chemical wastes.

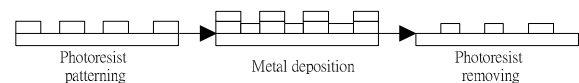


Figure.3 Metal lift-off process

Etching process has been used in the metal pattern manufacture for a long time. However, in the etching process, undercut effects will occur under the photoresist mask. This phenomenon causes metal patterns to duplicate the shapes of photoresist pattern imprecisely and also limits the size of metal traces. Therefore, for making fine line, semi-additive process is introduced into metal line process. Even though semi-additive process, there is a limitation. Because the seed layer has to be removed by the etching process, an isotropic etching process will change the shapes of metal patterns. Therefore, there are some differences between metal patterns and photoresist patterns. This also generates the limitation of the size of metal traces. Figure.4 is the technology roadmap of Jisso. It shows 7 μ m line is

the best record of present technology. Regarding our process, as aforesaid, our metal lift-off requires less process chemicals. Furthermore, because there is no etching process, metal pattern can be precisely duplicated the shapes of photoresist patterns and make finer metal traces. The best record of our process is 5 μ m line under the 1:1 aspect ratio. Figure.5 shows the result of 5 μ m line.

Item	Class	2006	2008	2010	2012	2014	2016
Min. Line Width (μ m)	A	30	30	20	20	15	15
	B	20	15	15	7	7	7
	C	15	7	7	5	5	5
Min. Space Width (μ m)	A	30	30	20	20	15	15
	B	20	15	15	7	7	7
	C	15	7	7	5	5	5
Min. Land Diameter for Laser Micro Via (μ m)	A	110	90	90	80	80	70
	B	90	70	60	60	50	50
	C	70	60	50	40	40	30

Figure.4 2007 Jisso Technology Roadmap

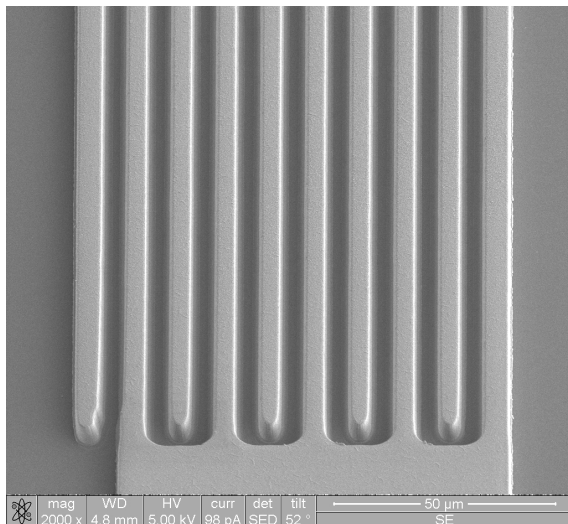


Figure.5 5 μ m metal traces

Dielectric layer process

Regarding dielectric layer, dielectric layers of PCBs are formed by compressing copper clad laminates (CCL) and pre-pregs. The manufacturer of CCL and pre-pregs provides the dielectric layers and also confines their characteristics. PCB manufacturers can not change the characteristics of dielectric layer just by themselves. It is the same way in high density interconnection (HDI). The dielectric layers of HDI are formed in the process of resin coated copper

(RCC) or dielectric film. These two materials are also provided by their manufacturers, but not by HDI manufacturers themselves. Therefore, neither PCB manufacturers nor HDI manufacturers can wholly control the characteristics of dielectric layers in their processes.

On the contrary, in our process, the characteristics of dielectric layers can be controlled by ourselves. We use liquid film coating process to make dielectric layers. In our process, we just need liquid dielectric material and one coating step. The processes become much easier and cost less energy and materials. More importantly, we can make thinner dielectric layer.

Handling issue is a serious problem in the processes of thin dielectric films. Although thin dielectric films can be made by liquid film coating, we still have to overcome the handling issue. Therefore, we develop a unique temporary carrier process. All dielectric layers and metal layers are made on the temporary carrier and released from the carrier after whole IC substrate is done. Regarding the results, we had made a 8-layer IC substrate whose thickness of each dielectric layer was just 8 μ m. Figure.6 shows this substrate.

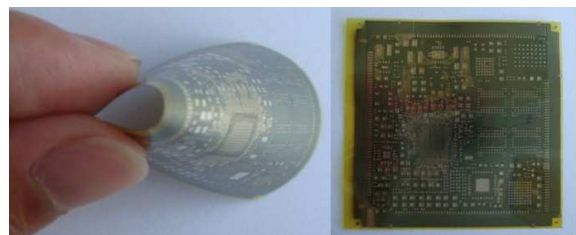


Figure.6 Princo's 8-layer IC substrate

VIA process

Furthermore, the rigid characteristic of temporary carrier can lead the overlay alignment to higher accuracy. In conventional PCB and HDI process, the

best overlay alignment accuracy is $\pm 20\mu\text{m}$. However, in our temporary carrier process, the overlay accuracy can reach $\pm 5\mu\text{m}$. Thus both up and bottom VIA lands can be just $30\mu\text{m}$ if the VIA size is $20\mu\text{m}$. By comparing with technology of Jisso, the specification of our VIA land is much ahead of present technology. Naturally, the routing density is much increased. For example, by aforesaid design rules of VIA, even with rules of $15\mu\text{m}$ line and space, an 3-row area grid array in $105\mu\text{m}$ pad pitch can be easily fanned out in just one routing layer. Regarding international technology roadmap of semiconductor (ITRS) shown as Figure.7, our substrates have no limitation to match the future trend of flip chip packaging.

Year of Production ^o	2007	2008	2009	2010	2011	2012	2013	2014	2015
Substrate cross-section core thickness (μm)^o									
Coreless buildup layer ^o	40	40	35	35	30	30	30	30	30
Blind via diameter (μm)^o									
Coreless ^o	60	50	50	40	40	35	35	30	30
Bump pitch (μm)									
Coreless ^o	130	120	110	100	100	90	90	80	80
Lines/space width (μm)^o									
Coreless ^o	20	15	15	10	9	8	8	6.8	6.4

Figure.7 ITRS2007 Roadmap

System demonstration

For demonstrating practicability of our substrates, a multi-chip SIP system prototype was made. Figure.8 is its photograph. This SIP system, including 5 flip chips, 17 CSP components, 6 connectors and 261 SMD passives used a 8-layer substrate which had totally 2042 pads. Even so, the substrate size was just $39\text{mm} \times 39\text{mm}$ and its thickness was only $90\mu\text{m}$. Figure.8 shows the operation of the system. An Android demo system in one packaging was made. With running by 266 MHz ARM based CPU, this prototype shows perfect functionality. Therefore, this technology of packaging substrates was proved to successfully integrate a complete computing system.

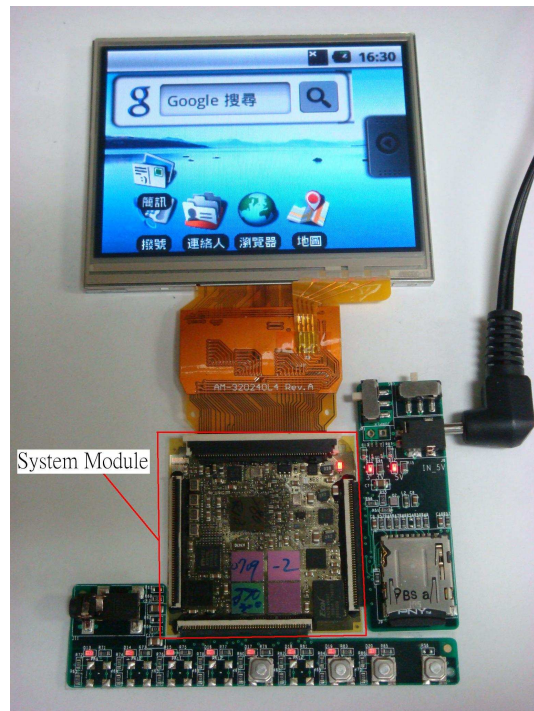


Figure.8 Android demo system in one packaging
Summary

In summary, we have developed a novel and simplified process for PCBs and IC substrates. In this process, material consumption and chemical waste can be reduced. It only requires photoresist, dielectric materials and 3 chemical solutions. Thus this technology is not only efficient but also environment-friendly. Moreover, this technology improves the routing density of IC substrates to a higher level, matches present technology roadmaps and is even much ahead of them.

References

- [1] ITRS, "International technology roadmap for semiconductor- assembly and packaging", 2007 edition.
- [2] Henry Hisanobu Utsunomiya, "Challenge on Packaging Substrate Technologies toward next decade", Proceedings of the 3rd IMPACT and 10th EMAP joint conference, Taipei Nangang Exhibition Center Taipei, Taiwan, October 22-24, 2008