

New Methods for Mechanical Mating Characterization of Surface Mount Technology Card to Board Interconnections

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Abstract

Large scale system packaging density requirements continue to place increased demand on improving card to board interconnections in the areas of electrical performance as well as physical density. To address these needs, card to board assemblies with new high density, surface mount technology (SMT) waferized interconnect systems have been developed, along with new methods to assess their mating characteristics to ensure both sufficient initial mating as well as long-term connection reliability. Applying existing measurement devices, new methodologies are presented to record interconnection alignment and the stress in solder connections. Exploiting the physical construction of the interconnection system, analytical and experimental techniques are detailed to reveal how solder attach strength and connector mating strains can be coupled to predict SMT solder strains during the mating cycle as well as during package environmental stress testing.

Introduction

Recent trends in computer server packaging design have focused towards 2nd-level integration and sharing of larger numbers of logic resources, including processing units (PU), volatile memory, and an array of I/O functions. In doing so, these applications have placed increased demand on interconnecting multiple physical entities to create reliable, high-speed, large symmetric multi-processing images in efforts to maximize performance and enable continued system availability. To meet these ever increasing computing demands, new, highly-dense, surface mount technology (SMT) connectors have been developed, which challenges the industry to create new and innovative means to evaluate system interconnect quality and overall system application design robustness.

It has long been established that tools and measurement means exist to design, analyze and test system electrical characteristics; including signal integrity, power distribution losses, and the influence of specific interconnect designs on overall system electrical performance. Conversely, fully defined tools sets for system-level mechanical evaluations have only been recently established. In general such methods were not required in the past as prior system

designs used combinations of pin-in-hole (PIH) and compliant pin connector styles. However, with the advent of increased signal speeds (e.g., > 3Gb/s – single-ended), a need to create an overall high density, SMT interconnection construction with improved electrical performance sufficient to allow the bypass of circuit board signal integrity process enhancements (e.g. Back drilling for via stub reduction) was established. In doing so, new methods to assess mechanical interconnect robustness were also required and established.

This paper highlights these mechanical assessment methods and describes an end-to-end approach used for evaluating a large, waferized, connector system now used in several server applications. Specifically, by coupling existing analytical methods and measurement tools, a means to evaluate strains on connector solder interfaces is described. This description spans studies conducted during system mating/unmating cycles, during in-situ system-level fragility testing, and also includes a complimentary evaluation method used to correlate resultant strains to critical in-system connector angularity required to ensure plugging robustness.

General Application Description

A recently introduced server system employed a new SMT attached connector system [1, 2] (ref. Fig. 1). This connector's system is constructed of a series of wafers that are encased by end guide blocks and interior joiner modules. The wafers, the guide blocks, and the joiner modules are positioned and retained by a stainless steel organizer. Each wafer consists of 14 signals with complementary reference contacts at the mating interface which provide three contact leads (i.e. one signal and two references) at the soldered interface per signal. For the specific application described, a 120 wafer version of the connector was used, yielding 1680 mated signals and 5040 soldered connections.

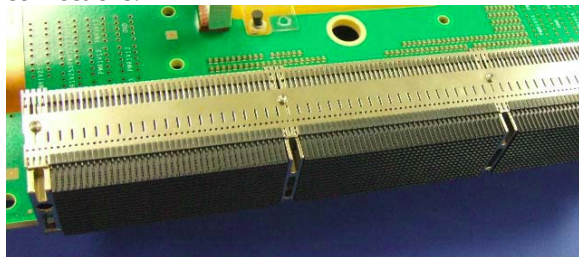


Figure 1. 14 Row Ventura™ Connector

Right angle receptacle and header versions of the connector were SMT attached to large daughter card and motherboard assemblies², respectively (ref. Figures 2a & 2b). Each daughter card receptacle is guided and mated to the respective back-plane slot vertically within a central electronic complex (CEC) using specially designed actuation hardware (see Figure 3).

As depicted, the actuation hardware consists of a node actuation mechanism (NAM) and a node lock mechanism (NLM). The NAM uses a screw-driven wedge scheme and incorporates telescoping ball-bearing slides to facilitate horizontal installation into and out of the CEC assembly and vertical actuation (i.e., mating/unmating of the connector), respectively. The NLM is also a screw-driven, wedge drive mechanism with vertical spring-loaded compliancy. The connector mating is completed by actuating the NAM, installing the NLM and then applying a ¼-turn of reverse rotation on the NAM's drive screw. This last step relieves stress on the mated connector and sets the load transmission path characteristics of the mated system.

Given the nature of the vertical mating orientation and the concern with solder joint integrity and mating angularity both static and dynamic strain limits were established. To validate the design a series of coupled analyses and experiments were

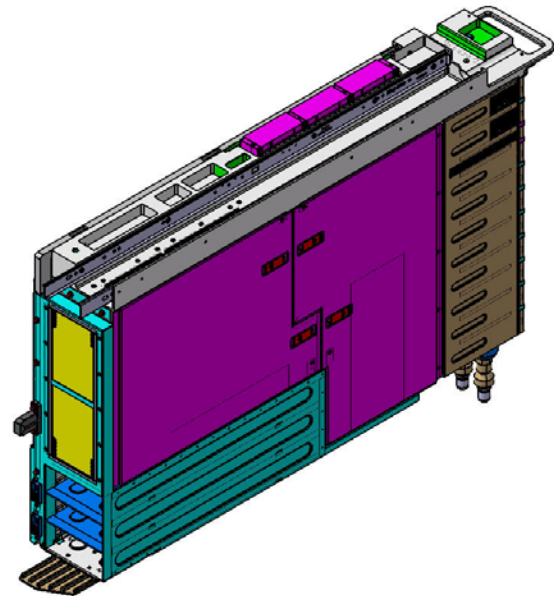


Figure 2a. Enclosed Daughter Card Assembly

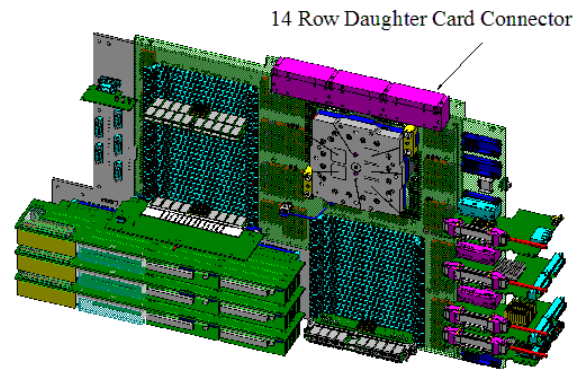


Figure 2b. Exposed Daughter Card Assembly

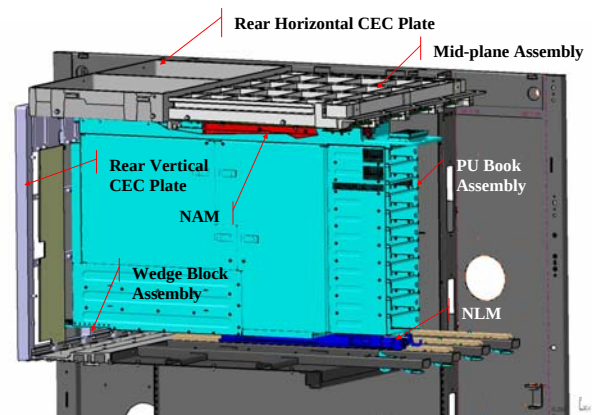


Figure 3. Daughter Card Assembly within a CEC

devised to quantify the effectiveness of the system's actuation mechanism and structural characteristics. Key elements to this approach included (1) using multiple linear variable differential transformers to

quantify the connector's angularity (i.e., pitch & roll) during mating relative to the mating connector, (2) creation of a wafer-level and connector-level finite element analysis approach coupled with a wafer-level strain-gauge measurement technique to predict solder joint strain during connector mating and (3) the use of multiple in-situ strain gages, housed within a daughter card connector assembly to verify both static and dynamic wafer strains during connector mating and system-level fragility testing, respectively.

Connector Mating Angularity Measurement

By specification, the mating of the connector has to meet both mechanical and electrical requirements [2]. Specifically, as the daughter card connector approaches the stationary header connector, the mechanical roll angle during engagement is required to be kept within ± 0.6 degrees. Figure 4a shows a node with a Cartesian coordinate system on which the angular motion of the node is defined. Due to changes in connector insertion force during engagement and actuation dynamics the connector roll angle is expected to change during the mating process. While pitch and yaw angles are important, they are considered to be less influential in stressing the SMT solder joint due to wafer flexibility out of plane. In addition to roll angle specification, electrical functionality of the connector requires a minimum connector engagement or a maximum gap between the daughter card and header connector end-blocks to be established. Specifically, the residual gap at the end of the mating operation is required to be less than 100 μm , so that the electrical wipe length of the connector pins can maintain signal integrity.

In order to estimate roll and pitch angles as well as residual gaps during the mating phase, four gap sensors were employed mating connector halves. From four independent outputs of the gap sensors the two roll and pitch angles were estimated. One key challenge was to embed miniature position sensors that can give reliable gap information for a 5 mm stroke length or connector engagement while providing an accurate measure of the final (residual) gap. Figure 4b shows two distinct sensor types evaluated. The first sensor is a non-contact type based on an optical assembly that transmits infrared light and receives a portion of reflected light from a target surface. The second sensor requires mechanical contact and is based on the principle of a linear variable differential transformer (LVDT) in which a spring loaded plunger is moved by the stationary target surface (i.e., header). After multiple evaluations with different headers, it was found that

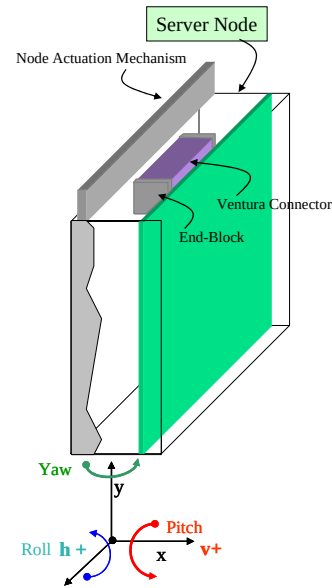
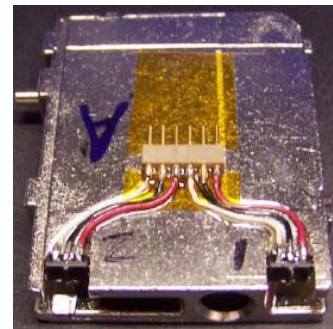
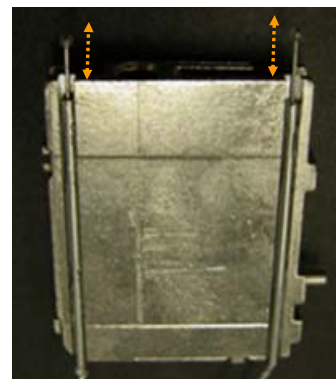


Figure 4a. Cartesian Coordinate System for Daughter Card Mating



End-Block with Optical Gap Sensor



End-Block with LVDT Gap Sensor

Figure 4b. Non-contact and Contact based Sensors

optical variability of the target surface could corrupt the measurement process. For simplicity in testing, it is desirable to retain one set of calibration parameters independent of the target surface. In this regard, the

contact based LVDT sensors proved more reliable, and could be used with single set of calibration parameters. Thus the testing of various server mounting locations on a given rack was simplified using LVDT-based sensing technique. In doing so, the sensors produced an equivalent 1-sigma noise of 3.5 μm , sensitive enough to determine the residual gap.

As noted previously, the connector contains 120 wafers housed between two end blocks numbered sequentially end to end with contact columns within a wafer denoted by characters A through P starting at PWB (printed wiring board) surface. The four corners of the connector assembly are thereby referred to as A1, P1, A120 and P120. Figure 5a shows the parameters needed to estimate the roll and pitch angles. The time history of the gap data and separation distance between the sensors (i.e., $L_R = 27.2$ mm and $L_P = 255$ mm), are required to estimate the pitch and roll angles.

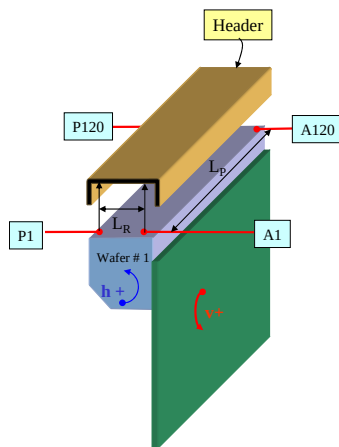


Figure 5a. Non-contact and Contact based Sensors

Figure 5b shows the estimated roll and pitch angle as a function of time per trial. Observe that the node actuation process was completed within 11 seconds, with the mating process producing dynamic effects during this period. NLM installation and NAM $\frac{1}{4}$ -turn back-off operations require tool changes, thereby producing a time dwell. To improve visualization, the pitch and roll data are plotted with respect to “gap” distance between mating connectors (ref. Figure 5c), whereby various portions of the mating process are categorized into phases indicated by symbols A through F.

As shown in Fig. 5c, the daughter card and header connectors come into initial mechanical contact [phase-A] when the gap is about 7.5 mm, while the LVDT sensors become valid after the gap is reduced to about 5 mm. Continuing engagement, the daughter card connector pins enter the header during

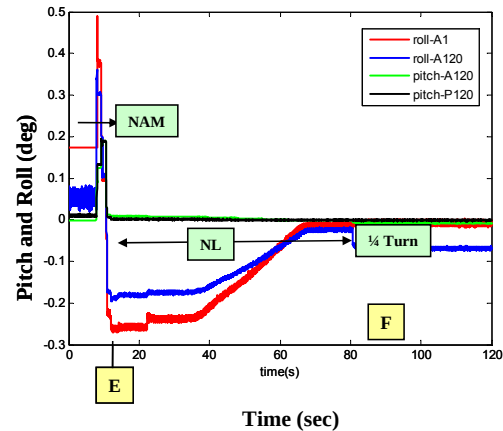


Figure 5b. Actuation Sequence; Mating Angle vs. Time

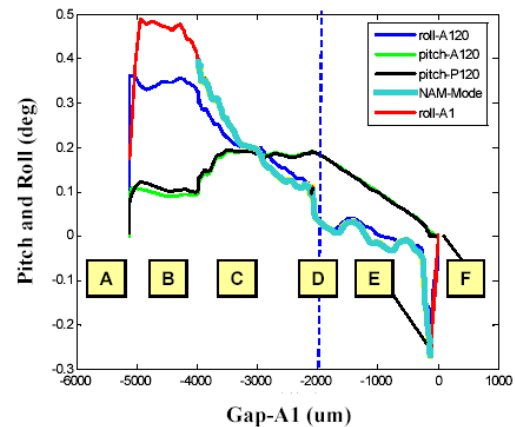


Figure 5c. Actuation Sequence; Mating Angle vs. Mating gap

phase B, where contact friction begins. Electrical wipe begins during phase-C, when the gap is 4 mm. increasing the insertion force per contact while reducing roll angle from 0.5 deg to near 0.0 deg at the end of mating. Phase-D shows onset of pitch angle change, where the characteristics indicate one end block becoming in physical contact with the header (i.e., gap = 0 μm). Phase E is the culmination of the mating process. Phase F corresponds to the end of NLM installation, followed by $\frac{1}{4}$ -turn back-off process. Note, that the roll and pitch estimates using the four sensors more or less track each other. This confirms that the relative motion between the mating pairs is equivalent to that of a rigid body motion even though some variation in roll angle indicates a potential torsional deformation in the system.

Wafer- and Connector-level Solder Joint Strain Quantification

For wafer- and connector-level solder joint strain quantification, the SMT connector was divided

into three bays each consisting of several wafers. A single wafer is a composite of stamped grounding structure with thermoplastic resin components. These structures are described below. The strain in the soldered connection between each wafer to daughter card assembly is an important quantity to study when trying to predict the degree to which the connector is stressed when it encounters any number of mechanical exposure conditions. The method used to examine the wafers' solder strain was to create a macro finite element (FE) model of an individual connector wafer, subject it plugging loads or other conditions and then use macro reaction force and moment outputs (measured at a split plane near the soldered lead connections) These were then used as inputs to a micro finite element model of an individual soldered lead with solder strain results being queried at the solder fillet. Correlation of the macro wafer FE model with strain gage results from experimental wafer loading provided confidence in the modeling technique and supported the running of the FE models to many, varied, connector load conditions and the comparison of the solder strains at the wafers connection to the daughter card. Conversely, a daughter card connector, with several connector wafers instrumented with rosette-style strain gages, was assembled to provide strain gage measurements during system-level fragility testing. These results were then used to estimate wafer solder fillet strain.

Modeling of wafer-level strain

The macro FE model of a single connector wafer (ref. Figure 6) was constructed as an assembly of thermoplastic components, a stamped metal grounding structure as well as a series of metal signal leads over molded in thermoplastic. The FE model was built in ANSYS [3] and consisted of approximately 200k hexahedral and tetrahedral solid elements with a total of 1.5M degrees of freedom. The detail in this macro wafer model allowed for the easy output of force and moment reaction forces. These were then used as inputs in the micro solder lead/fillet model, shown as the shared cut plane in the area of the signal lead (ref. Figure 7). Using this macro-micro analysis method, a variety of connector plugging scenarios were simulated to test various connector header to daughter card alignment tolerances, making it possible to compare the resulting solder fillet strains (ref. Figure 8).

A macro-micro modeling approach was also used to model the individual solder lead response of the single wafer. The force vectors and moments obtained from the earlier macro model were used as

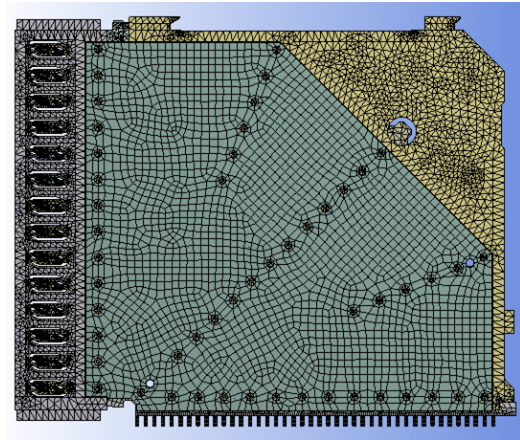


Figure 6: Finite Element Model of a Single Connector Wafer

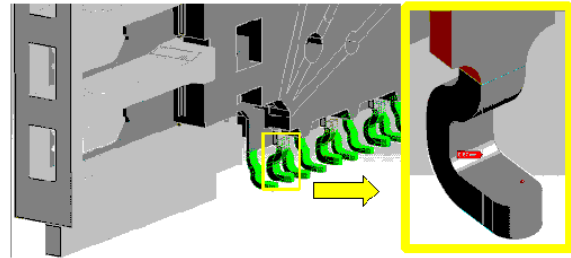


Figure 7: Shared Reaction Plane Location at the Signal Lead (outlined in red)

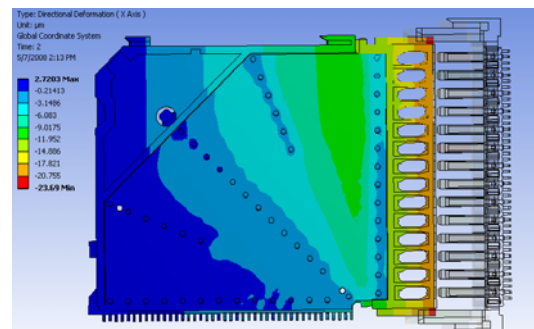


Figure 8: Example of a Daughter Card Wafer to Connector Header Plugging Simulation Modeling of Signal Ground Solder Lead Response and Relationship of Wafer Strain to Solder Stress

inputs to the micro model. The finite element micro model (FEMM) consisted of one signal and two ground leads with their respective solder profile and copper pads. The solder profile was mapped from a representative solder micrograph and constructed as 3D solids. Careful consideration was given to the solder fillet and heel profile on the signal and ground leads. The solder material used in the model was a eutectic solder with material non linearity of

plasticity and creep. The plasticity was defined by using the kinematic hardening rule and the creep properties of the solder were obtained through an extensive literature search [4]. Figure 9 shows a typical solder profile for signal and ground leads used to understand the mechanism of load transfer through finite element analysis. The complete FEMM is shown in Figure 10.

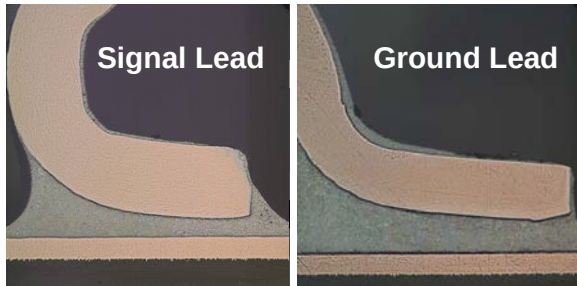
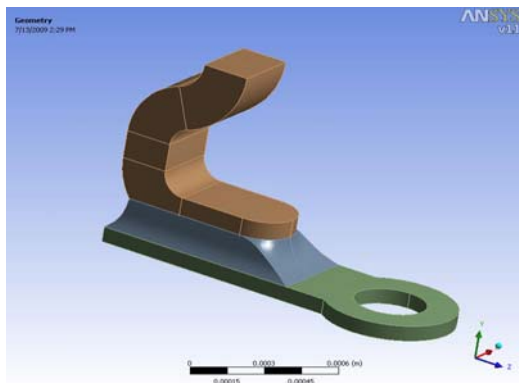


Figure 9: Solder Fillet SEM micrographs



then applied to the macro FE model of a single connector wafer. Correlation of the resulting component strain correlating with that measured by the wafer strain gages is provided Figure 12.

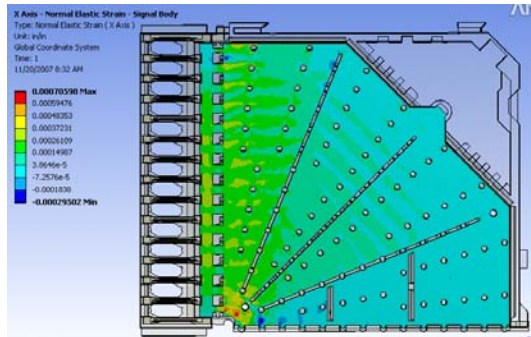


Figure 12: Wafer Strain Resulting from 8lbf Wafer Face Load

Once this was completed, whole waferized connectors (containing 8 to 10 wafers with strain gages mounted to them dispersed along the length of the connector) were specially built and mounted to PCB boards. These PCBs were then built into pluggable nodes. These nodes were installed in a system, during which, the strain gaged wafers were monitored. Figure 13 shows the test node set up prior to plugging. Based on these results, the node plugging methods were refined to minimize strains applied to the SMT joints.

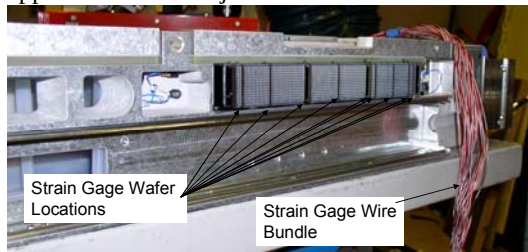


Figure 13: Node plug testing set up Results and Discussion

Force vectors and moments from the macro model were used to derive acceptable load limits for individual wafers based on the stress state of solder fillet. These results were experimentally verified and are shown in Figures 14 and 15. A wafer force greater than 8 lb per wafer resulted in solder stress greater than yield stress of the solder and in some cases higher than its ultimate strength. Therefore, the acceptable force was reduced via modeling to be between 5 to 8 lb. Figure 16 shows the acceptable wafer strain values related to these conditions. The wafer strain results due to node plugging experiments are shown in Figure 16. These results show that during node actuation, maximum strain values occurred in Bay 1 and Bay 3 of the connector (i.e., the wafers near the end guide blocks). Specifically,

the strains at wafer 35 (Bay 1) and wafer 119 (Bay 3) exceeded max strain value of 300 microstrain. For plug sequence #3 (i.e., with quarter turn back-off), all the strain numbers were below 300 microstrain limit [5].

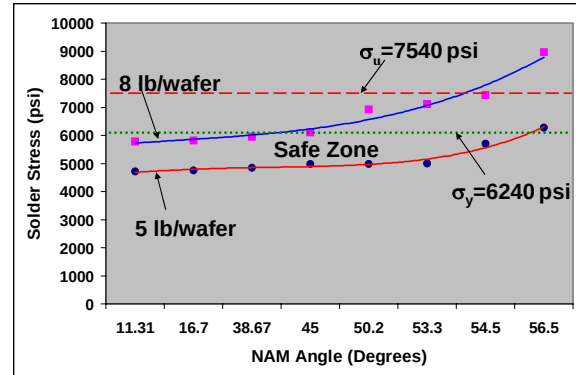


Figure 14: Correlation of force vector from macro model to solder fillet stress values using micro model

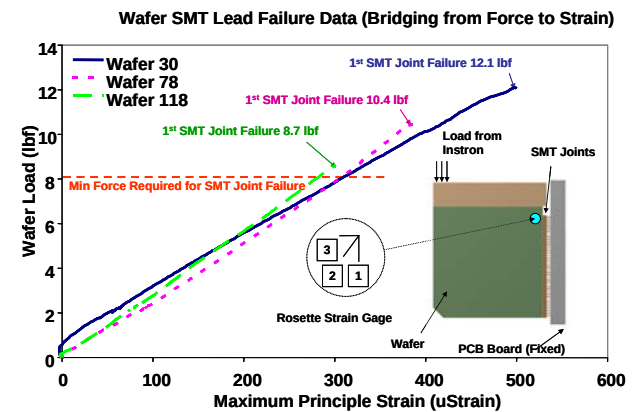


Figure 15: Wafer SMT lead failure data

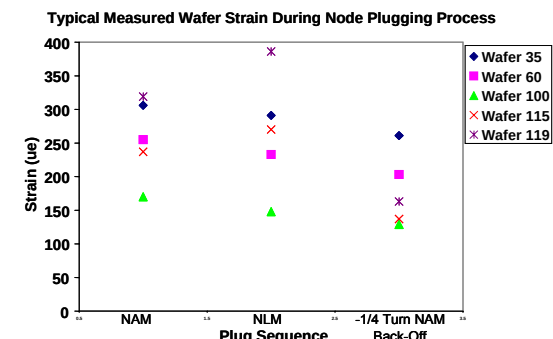


Figure 16: Wafer strain data during node plugging process

Connector-level Dynamic Strain Measurement

Complimenting the aforementioned mating studies, system-level fragility testing has traditionally

been employed as part of the final product testing phase. Performed in both minimum and maximum configurations, test plans typically include a number of pre-and post-exposure mating cycles, a simulated thermal shock exposure as well as vertical and horizontal shock and vertical vibration testing (ref Table 1).

Table 1: Typical System-level Fragility Test Plan

Seq. #	Sequence Step	Sequence Description
A	Initial Incoming Inspection	
1	Hardware Characterization	Record mechanical efficiency of all actuation hardware
2	Hardware preparation	Install monitoring accelerometers on strain
B	Preparation	
1	Thermal Conditioning (non-strain gaged nodes)	Temperature excursion; -40 to +60C (10x)
2	Install strain gaged node	Record strains during mating cycle
3	System preparation	Install specified shipping brackets using provided installation instructions
C	Unpalletized Horz. Impact	
1	Horizontal Impact	Excitation (@ 0.75 m/s) - side orientation (2x)
2	Horizontal Impact	Excitation (@ 0.75 m/s) - rear orientation (2x)
3	Horizontal Impact	Excitation (@ 0.75 m/s) - rear edge (2x)
4	Post-test	Complete visual inspection of all components
F	Unpalletized Shock	
1	Vertical drop test	Drop height - 4.5" (2x)
2	Vertical drop test	Drop height - 2" (10x)
3	Post-test	Complete visual inspection of all components
G	Unpalletized vibration	
1	Random Vibration	Excitation - 0.84 g rms
2	Sine Sweep	Excitation 0.5g from 2-200 Hz for 30 min.
3	Post-test	complete visual inspection of all components
H	Palletized Shock	
1	Vertical drop test	Drop height - 4.5" (2x)
2	Vertical drop test	Drop height - 2" (10x)
3	Post-test	Complete visual inspection of all components
I	Palletized vibration	
1	Random Vibration	Excitation - 0.84 g rms
2	Sine Sweep	Excitation 0.5g from 2-200 Hz for 30 min.
3	Post-test	complete visual inspection of all components

This final step is completed using functional hardware, for system validation which can be very expensive, especially when unexpected failures occur. To enhance this, the aforementioned strain-gage technique was employed. In doing so, the dynamic strains of the mated daughter card connector could be assessed prior to functional testing and be used as a key indicator of the system's design robustness. Figure 17 shows an example of how the wafer strains could vary during the mating process. Furthermore, employing this technique also provided a means to evaluate various design enhancements (i.e., various add-on shipping support brackets, etc.).

Summary & Conclusions

Recent trends in large scale system packaging have required the development and evaluation of new, high density, surface mount technology attached card to board connectors. Exploiting their waferized construction, new methods have been developed to assess their mating characteristics to ensure both sufficient initial mating as well as long-term connection reliability by using/applying:

- embedded LVDTs to complete mating angularity studies

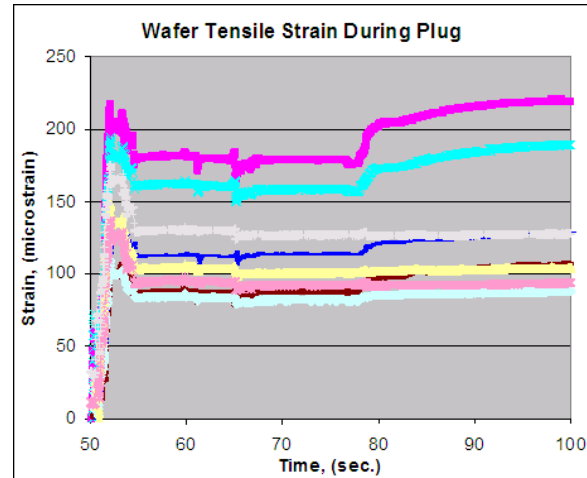


Figure 17: Dynamic Wafer Strain

- combined macro- & micro-model wafer-level & connector-level FEA methods coupled with empirically evaluating soldered strain gaged wafers to identify maximum mated force and solder attach strain limits.
- strain gage measurement technique during system-level fragility testing to identify mated connector solder attach robustness as well as the effectiveness of shipping support hardware, all prior to final functional testing.

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