

Electromigration Study of μ PILR™ Platform for Fine-Pitch Flip chip Interconnects

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Abstract:

Flip chip packaging technology is typically used for high-performance devices that require the interconnects to have the capability to carry high currents at elevated temperatures for extended periods of time. The current values can be as high as many hundreds of mili Amperes, which translates to more than $10,000 \text{ A/cm}^2$. Increasing number of I/O per die and shrinking form factor has been in greater number and smaller size of the first level flip chip interconnections. This increases current density and translates to higher current crowding on both the die and substrate sides of the interconnects. In recent years this trend has been a driving factor for raising awareness of electromigration related failure for design and development of high-end flip chip interconnections. There are different solutions being implemented in the industry to address this concern, such as changing the UBM structure, adding barrier layers, changing the composition of solder, etc.

In this paper, the μ PILR interconnect is investigated for flip chip electromigration characteristics. The μ PILR platform is implemented by use of Cu bumps on substrate to facilitate first level flip chip interconnections. Two μ PILR flip chip interconnect designs are discussed in this study. For the package-level testing of the first design, a test vehicle was built with a die size of $18 \text{ mm} \times 20 \text{ mm} \times 0.75 \text{ mm}$, which was packaged on a substrate measuring $40 \text{ mm} \times 40 \text{ mm} \times 1.24 \text{ mm}$. The package has more than 10,000 μ PILR based interconnects with a minimum pitch of 0.150 mm , and a maximum pitch of 0.2 mm . The chip has 0.105 mm diameter Sn/2.5Ag solder bumps attached to it. The μ PILR interconnects are present over the substrate pads with a solder mask opening of 0.090 mm . 1000 hours of test results are discussed for three current levels of 0.5 A , 1 A and 1.5 A corresponding to current densities of $1.5 \times 10^4 \text{ A/cm}^2$, $3.0 \times 10^4 \text{ A/cm}^2$ and $4.5 \times 10^4 \text{ A/cm}^2$ respectively. Temperatures for these tests are kept at 120° C , 130° C and 150° C respectively. The result shows failure mechanism of electromigration void growth near die UBM whereas no substrate side void growth is observed. Next a modification in the μ PILR flip chip joint design is discussed which involves Cu bump fabricated on a flip chip substrate by a controlled Cu-Cu joining process using Sn. Electromigration test results are presented for a simple Cu-Sn-Cu test structure that mimics a modified part of the interconnect structure representing $30 \mu\text{m}$ diameter Cu bump on substrate. These tests done at 160° C for current density of $7 \times 10^4 \text{ A/cm}^2$ show no void growth for 1000 hours of current stressing and not more than 3 % increase of initial test structure resistance.

In conclusion, a flip chip interconnect structure is investigated for its electromigration performance with fine pitch. Experimental results show more than 995 hours of lifetime at a current value of 1.5 A ($4.5 \times 10^4 \text{ A/cm}^2$) and chip temperature of 150° C for the 0.15 mm pitch μ PILR flip chip package.

Key words: μ PILR, Flip Chip, Electromigration, UBM, Reliability.

Introduction

Demanding requirements such as high-end graphics capabilities and mobile computing are pushing consumer electronics products toward smaller size, weight and reduced cost. Microprocessor chips are being packed with an ever increasing number of transistors with aggressively scheduled goals to go toward 22 nm nodes. These

advancements in front-end silicon processing technology are making processors and ASICs more powerful and feature rich. At the same time flip chip packages that accommodate these silicon dies are being designed to allow higher I/O densities while targeting smaller form factors. Altogether these requirements have made it necessary to design flip chip bumps with pitches of $150 \mu\text{m}$ and below. The

International Technology Roadmap for Semiconductor-2007 suggests that area array flip chip interconnect pitches will reduce to less than 100 μm and the number of I/Os in high-performance ASICs will exceed over 6000 by 2015 [1]. Intermediate wiring inside silicon is expected to handle more than 2x times higher current densities than the present levels. In short, flip chip bump sizes are shrinking and at the same time higher current carrying capability is desired.

Electromigration phenomena occurs as an outcome of momentum transfer from electrons flowing in an electrical field to the ions of interconnect metal. Due to inherent variation in microstructural properties of the metal conductor net positive or negative atomic flux divergence occurs which results in void formation. High current densities and directional change of current due to interconnect geometry produces current crowding inside the interconnect, which is defined as localized increase in current density. Higher localized current densities in turn produce joule heating and resulting thermal gradient produces thermal migration. Once void initiates in the interconnect it further increases current crowding and joule heating and eventually results in interconnect failure. In VLSI silicon circuits electromigration of Cu and Al interconnect has been studied over the last few decades but in the microelectronics packaging realm electromigration related reliability issues have recently gained attention and are relatively unexplored as failure phenomena. The lead free packaging initiative and the performance, form factor and cost demands discussed above have made it critical to consider electromigration reliability at early stage of design to meet challenging time-to-market schedules.

μPILR Flip Chip

Organic substrate used in flip chip packages currently is the most costly component of the package and at the same time is a bottleneck that limits performance. This requires innovative flip chip substrate technologies to meet the future demand of the industry. With respect to demanding market driven requirements, today's flip chip substrate technology faces many technical challenges to overcome. The flip chip I/Os are not only required to shrink in size and pitch and increase in count but are also required to carry electrical signals more efficiently and need to be more thermally conductive in order to provide better design flexibility by reducing hot spots and improving thermal management. Thermo-mechanical reliability requirements and high temperature operating conditions [2] are providing additional challenges with aggressive feature size scaling combined with low-k dielectric usage. With shrinking bump size and

pitch (order of 100 μm and below) conventional flip chip assembly processes and substrate designs are facing the greatest of challenges since the advent of flip chip technology.

The μPILR platform is being examined to address many of these critical issues for flip chip substrate design and reliability [3]. A μPILR flip chip bump substrate with flip chip bump area array of 18 mm x 20 mm is shown in Figure 1(a) measuring 40 mm x 40 mm x 1.24 mm of overall size with more than 10000 bumps. A typical μPILR flip chip substrate has truncated conical shape Cu bump structures on substrate pads. These Cu bump structures are manufactured for desired shape and size according to design requirements.

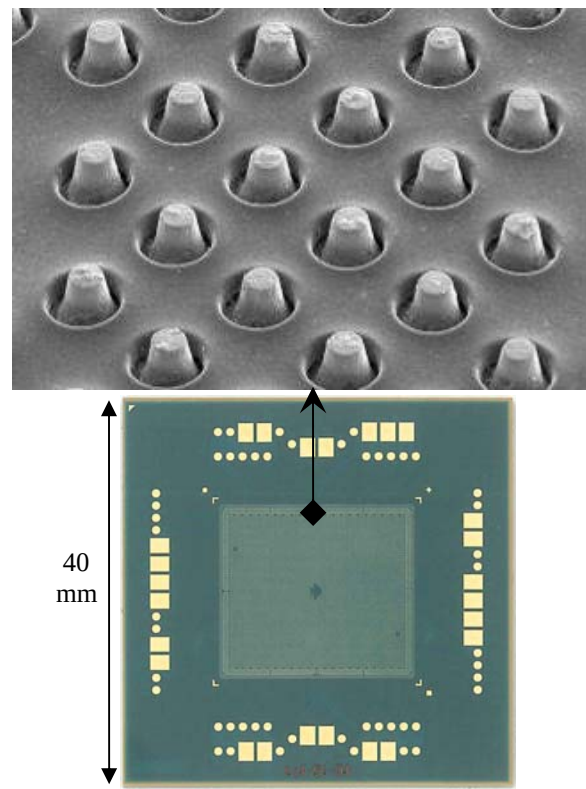


Figure 1(a) 18 mm x 20 mm area array μPILR flip chip substrate with bump pitch of 0.15 mm and 0.20 mm.

A schematic of a typical μPILR flip chip joint after flip chip assembly and under-fill process is depicted in Fig. 1(b). μPILR flip chip interconnects do not require solder on substrate pads, are scalable to very fine pitch and provide promising thermal cycle reliability [3]. The μPILR interconnect structure can be designed to leverage the existing infrastructure for substrate manufacturing and two different designs in this regard will be discussed in this article.

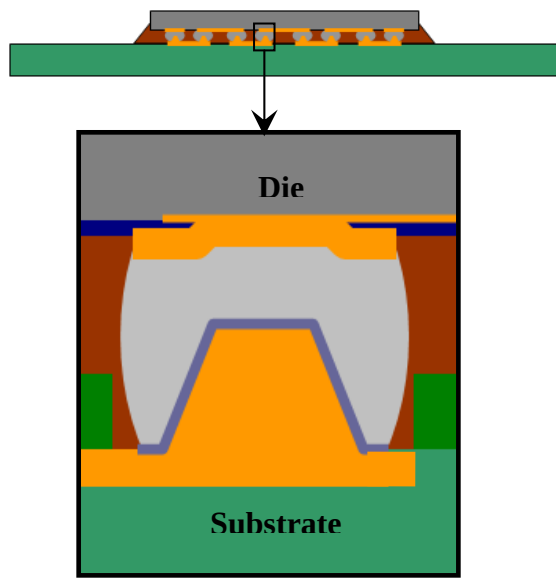


Figure 1(b). Schematic of μ PILR platform based flip chip assembly showing typical interconnect structure.

Electromigration Test Setup

In order to perform Electromigration tests a test facility (Fig. 2), with automated data acquisition, was developed according to guidelines provided in JEDEC standard JEP154 [2] for electromigration testing. A convection oven is used in order to achieve DUT temperatures above 110 °C. The oven has been pre-calibrated to confirm that the temperature variation remain within the JEDEC specified limitations. Multichannel power supplies have been incorporated into the test system to accommodate statistically enough sample size in future. Temperature sensors connected to automated data acquisition cards are used for measuring die back

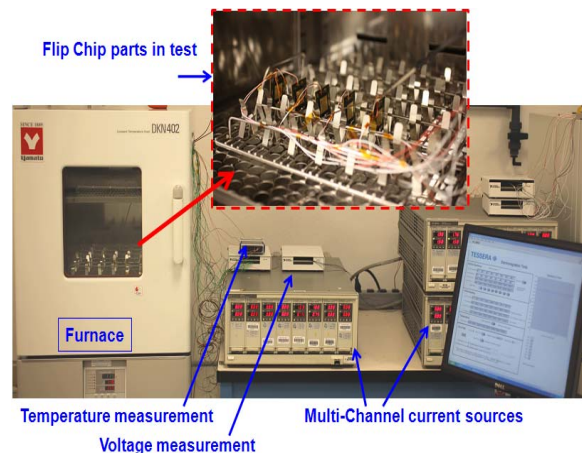


Figure 2. Electromigration Test Setup.

side temperature. To capture accurate temperature rise due to joule heating the electromigration test system is equipped with semi-automatic TCR (Temperature Coefficient of Resistance) measurements capability prior to electromigration tests on individual test vehicles. Independent current sources and voltmeters were used with a 4-point probe method for accurate daisy chain resistance measurements. TCR was computed using the minimum possible current level during the calibrations for each individual sample. The current is kept constant until the oven temperature stabilizes during each data point measurement on the TCR curve to ensure temperature uniformity across the die. A complete TCR curve from 50°C to 160°C was recorded for better predictions of time-zero resistances of each flip chip test vehicle. A typical resistance measurement curve for fabricated flip chip test vehicle daisy chain is shown in Fig. 3.

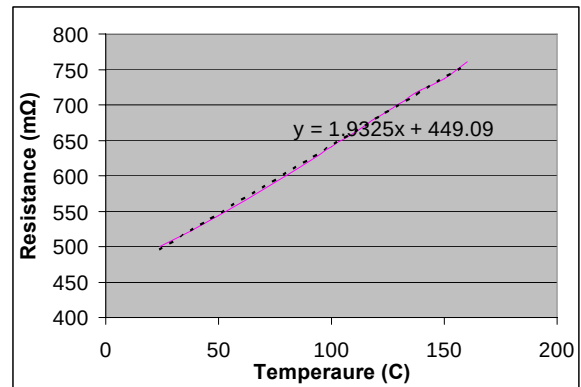


Figure 3. Typical resistance-temperature curve for test daisy chain.

μ PILR Interconnect type 1:

The μ PILR interconnect type 1 involves 3D copper bump structure shaped monolithic pad on organic flip chip substrates. A μ PILR flip chip test vehicle for such a design is shown in Fig. 4. The test vehicle is flip chip assembly made with 0.75 mm thick die of 18 mm x 20 mm size and a 1.24 mm thick substrate of size 40 mm x 40 mm. The μ PILR substrate is designed with more than 9500 flip chip interconnects (total of more than 10,000 μ PILR bumps) and bump pitches of 150 μ m and 200 μ m. Die side passivation opening size is 65 μ m and die metal line thickness is 3 μ m in these test vehicles.

Die side metal has 0.2 μ m thick Ti/W and 12 μ m Cu UBM. The substrate pads have a Cu bump structure that has base and tip diameters of 65 μ m and 40 μ m and height of 50 μ m. These Cu bump pads are metalized with Au(0.05 μ m)/Ni(4 μ m). Flip chip joints are formed using Sn-2.5Ag solder with a

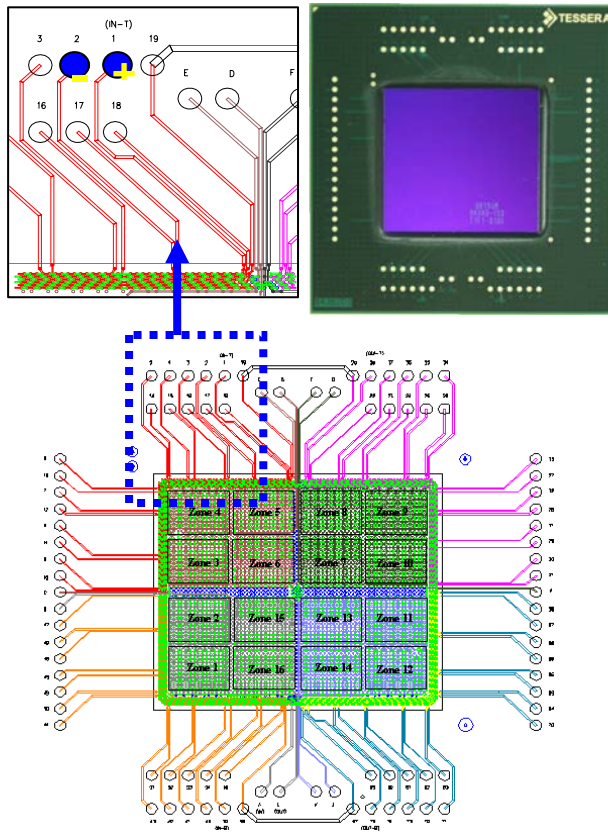


Figure 4 Flip chip package and the daisy chain used in the Electromigration test.

diameter of approximately 120 μm and overall flip chip bump standoff is 85 μm from die metallization to base of μPILR Cu bump. Several daisy chains were designed for electromigration with a number of bumps ranging from 9 to 12 per chain. One such daisy chain is shown in enlarged view in Fig 4. These chains are located near the die edge for convenient failure analysis after the test. A time zero

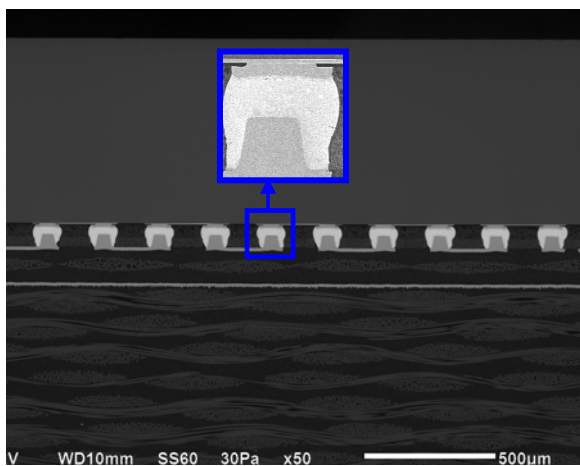


Figure 5 μPILR flip chip daisy chain for Electromigration testing.

cross-section for such a sample is shown in Fig. 5 with all the bumps in daisy chain located in single straight row parallel to die edge.

Test Results

Electromigration tests were performed for three different temperatures, and current level on three test vehicles. The aim of this study is to understand electromigration failure modes with use of μPILR flip chip substrates.

Current (A)	Temp ($^{\circ}\text{C}$)	Current Density (A/cm^2)	% Increase in Resistance	Test Time (Hours)
0.5	120	1.51×10^4	0.10	995
1	130	3.01×10^4	0.65	995
1.5	150	4.52×10^4	6.29	995

Table 1. μPILR type 1 Electromigration test results.

The daisy chain configuration of the electromigration test vehicle allows current stressing of flip chip bumps with electron flow from die to substrate side and vice versa. Thus both the die and the substrate side of the flip chip bump UBM can be tested simultaneously for their electromigration resistance. Three daisy chains tested at 0.5 A, 1 A and 1.5 A current at 120 $^{\circ}$ C, 130 $^{\circ}$ C, and 150 $^{\circ}$ C respectively. Resulting current density calculated based on 65 μm of die passivation opening is shown in Table 1. After 995 hours of current stressing minimal increase in resistance was observed with the maximum resistance increase in the part with the highest current density of 4.52×10^4 A/cm^2 . Fig. 6 shows resistance data collected for each case over test duration of 995 hours. With more detailed study involving enough temperature and current density combinations, Black's equation [2] can be solved for current exponent and activation energy which is outside the scope of this study and will be considered for future work. The part with the highest current density shows the maximum increase in resistance up to 6 %. This part was cross sectioned to examine the effect of current stressing and the cross section of the bump with highest amount of void is shown in figure 7a and 7b. The electron flow for this bump is from die side UBM toward substrate. After reflow, during the flip chip assembly process, a small amount of Cu_6Sn_5 IMC is formed at the interface between the die Cu UBM and solder alloy. During current stressing Cu diffusion continues from Cu_6Sn_5 IMC toward solder. This results in a shortage of Sn into the Cu_6Sn_5 IMC. This combined with enough Cu supply results in Cu_3Sn IMC formation near UBM. Subsequently higher atomic flux densities give rise to

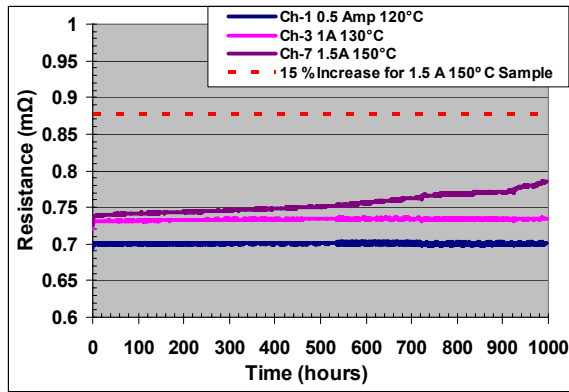


Figure 6 Resistance change of Electromigration test daisy chains after 995 hours of current stressing at various temperatures.

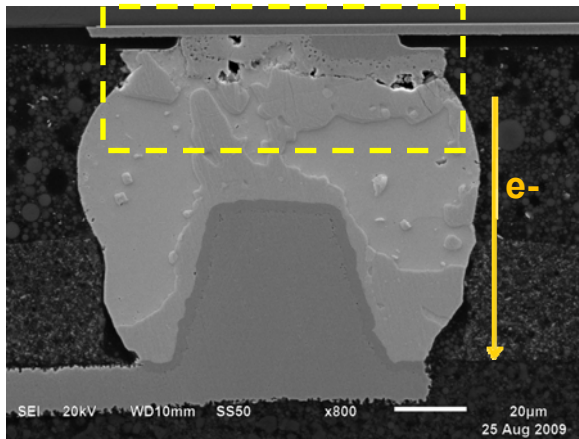


Figure 7a Section of μ PILR joint after current stressing of $4.5 \times 10^4 \text{ A/cm}^2$ after 1000 hours. Die side is cathode and substrate side is anode.

small Kirkendall void formations in Cu_3Sn . Enlarged view of the die side UBM of the bump in Fig 7a is shown in Fig 7b. Subsequently due to larger atomic flux divergence more voids and larger IMCs are formed in the bump. It can be clearly seen that smaller Kirkendall voids are near Cu rich Cu_3Sn IMC while larger voids are seen near the boundary between Cu_3Sn and Sn rich phase Cu_6Sn_5 IMCs. These larger voids mainly result in subsequent resistance increases of the flip chip solder joint. Cu_6Sn_5 IMC can be clearly seen below larger voids and surrounding the Cu bump structure on the μ PILR substrate. No damage in Ni coated Cu structure is observed on the substrate side of the flip chip bump. After almost 1000 hours of current stressing almost all Cu UBM is consumed and transformed into IMCs with voids. Here the Cu UBM initial thickness is $12 \mu\text{m}$ which provides Cu supply for longer periods of time before large voids start forming. Several studies have shown the effect of using thick Cu UBM in order to retard void formation[5]. When the flip chip

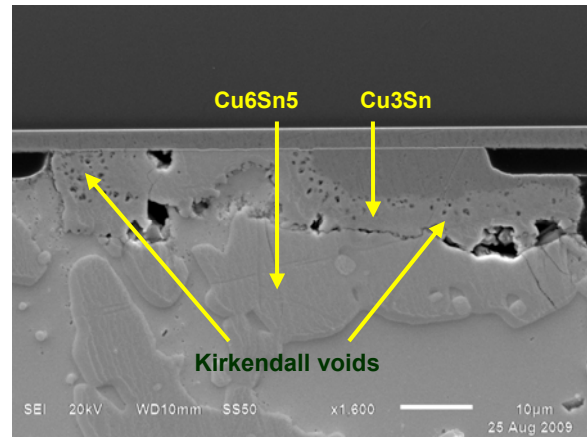


Figure 7b Void generation and Cu UBM depletion on die side of the μ PILR joint after current stressing of $4.5 \times 10^4 \text{ A/cm}^2$ after 100 hours

bump experiences reverse polarity such that the die side of the bump is anode and substrate side of the bump is cathode, void formation is expected to occur at the substrate side [6,7]. In Fig. 8a, SEM image of a bump in the daisy chain with reverse polarity, with substrate side as cathode and die side as anode, showing 995 hours of current stressing. Minimal void formation lesser IMC formation is seen in this bump. In the corner of the bump where electrons enter the substrate pad current crowding can be expected. Cu diffusion from substrate side is retarded by Ni barrier and consumption if Cu is thus slowed down [4]. Although due to expected current crowding at the location where electrons enter into the bump smaller void formation is seen. SEM image of this area of the bump is shown in Fig. 8b. Also very small voids can be seen at the tip of the Cu bump structure with Cu-Ni-Sn IMCs. On Die side UBM (Fig. 8a) Cu_6Sn_5 IMC is formed and small Kirkendall voids are found near Cu UBM on die side. Minimal Cu consumption

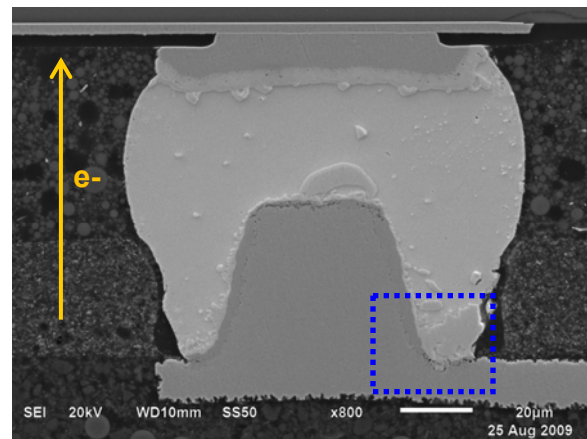


Figure 8a Section of the μ PILR joint after current stressing of $4.5 \times 10^4 \text{ A/cm}^2$ after 100 hours. Die side is anode and substrate side is cathode.

as well as no considerable void formation is observed on die side as well as substrate side for this bump.

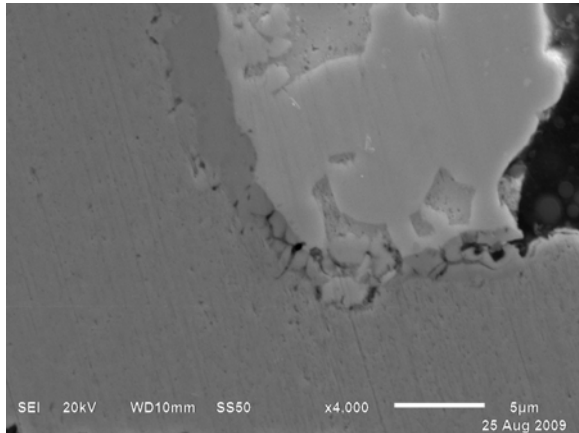


Figure 8b Section of the μ PILR joint after current stressing of $4.52 \times 10^4 \text{ A/cm}^2$ after 100 hours. Die side is anode and substrate side is cathode. Ni layer degradation is observed at the highest current crowding point.

μ PILR Interconnect type 2

A modified μ PILR flip chip bump design (type 2) that has similar 3D copper bump structures on the substrate pads is considered next. This design is intended to exploit the available infrastructure of flip chip substrate manufacturing. The μ PILR flip chip substrate for this design can be manufactured by forming a 3D Cu structure on a flip chip substrate using a Cu-Sn-Cu joining process. A schematic of the μ PILR flip chip bump with such a design is shown in Fig. 9 with prototype sample cross-section. Electromigration tests on these prototypes will be

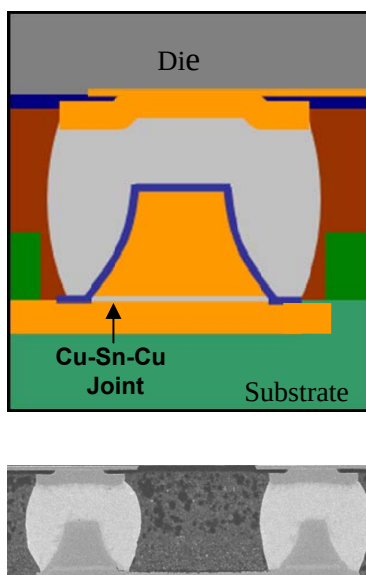


Figure 9 μ PILR type 2 design for flip chip interconnect.

considered in future work. In order to access the electromigration reliability of the Cu-Sn-Cu joint for this design a simple strip-line test structure with the Cu-Sn-Cu bond was designed as shown in Fig. 10. Two copper metal lines of $50 \mu\text{m}$ and $18 \mu\text{m}$ thickness are bonded with each other by circular tin area of $30 \mu\text{m}$ diameter and $2 \mu\text{m}$ thickness to mimic the μ PILR substrate 3D metal structure. This structure does not represent the actual flip chip joint but provides an early approximated reliability assessment of the Cu-Sn-Cu joining process as well as resulting bond line structure.

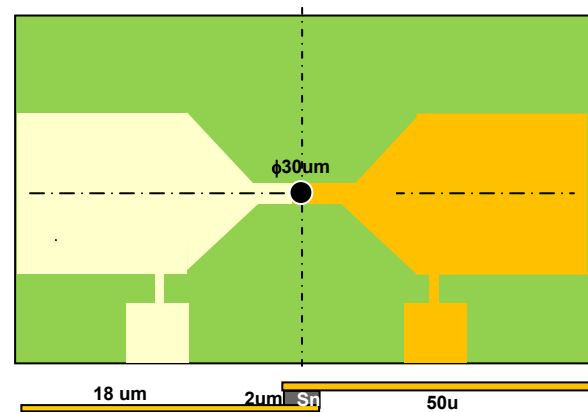


Figure 10 Strip-line test structure design showing bond area in top and side view.

Test Results

The strip-line test structures described above were tested in an Espec AEM1000 electromigration test chamber. Five such samples were tested for electromigration at 160°C at current level of 0.5 A which corresponds to $7.07 \times 10^4 \text{ A/cm}^2$. Test results are shown in Fig. 11 for resistance measurements of the test structures. At the end of 1000 hours of current stressing resistance increase

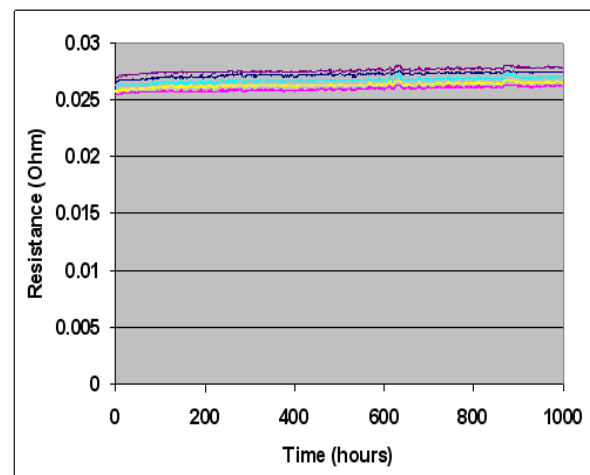


Figure 11 Strip-line test structure design showing bond area in top and side view.

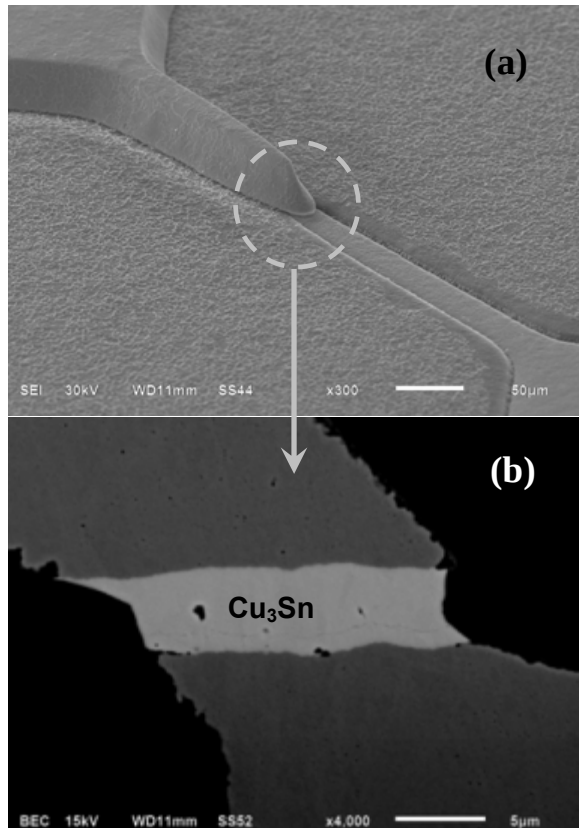


Figure 12 SEM micrograph of (a) Strip line structure for Cu –Sn-Cu bond line. (b) Cross section of the sample showing structure after 1000 hours of current stressing at 160° C and $7.07 \times 10^4 \text{ A/cm}^2$.

spans between 3 to 2.5 % for all the samples. One such sample was cross sectioned after the test and the SEM micrographs are shown in Fig. 12 (a) and (b). All the Sn between bonded Cu lines is converted into Cu_3Sn . A very small amount of voids can be seen in the structure after the current stressing. A couple of big voids seen in the cross section are expected to be manufacturing related and not from electromigration.

Conclusions

Two different μPILR flip chip bump structures were considered for their electromigration performance. μPILR structure type 1 test vehicles were build and tested with current densities of up to of $4.52 \times 10^4 \text{ A/cm}^2$ and temperatures of up to 150° C. Maximum resistance increase of 6 % is observed with no open failure after 995 hours of current stressing. Die side UBM consumption and void generation is observed mainly which will eventually result in failure of the flip chip joint. Minimal voiding was observed on substrate side with both positive and negative polarity cases. A simple strip

line structure was build and tested for current stressing at stressing at 160° C and $7.07 \times 10^4 \text{ A/cm}^2$. After 1000 hours no significant voids were found and maximum of 3 % resistance increase is observed in the test samples. The test results show good electromigration reliability using μPILR flip chip interconnect technology and future work will involve prototype testing of μPILR type 2 interconnect with MTTF analysis.

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