

Flip Chip Process Using the Cu-Sn-Cu Double-Pillar-Bump Bonding

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Abstract

Compared to the flip-chip process using solder bumps, Cu pillar bump technology can accomplish much finer pitch without compromising stand-off height and enable microelectronic packages to have better electrical and thermal characteristics. Flip-chip process with Cu pillar bumps can also be utilized in radio-frequency packages where large gap between a chip and a substrate as well as fine pitch interconnection is required. Conventional Cu pillar bump consists of a solder cap on a cylindrical Cu, and flip-chip bonding is accomplished by reflowing the solder cap on UBM of a substrate. Conventional Cu pillar bump technology may have several drawbacks such as necessity of deep photoresist patterning and severe UBM consumption. In this study, a flip-chip process using Cu-Sn-Cu double pillar-bump bonding has been investigated to avoid disadvantages of the conventional Cu pillar bump technology. Cu pillars with and without Sn caps were formed by electrodeposition, and Cu pillar bumps with Sn caps were flip-chip bonded to the Cu pillar bumps without Sn caps to form the Cu-Sn-Cu double-pillar-bump joints. Contact resistances and chip shear forces of the flip-chip specimens were measured with variation of the Sn-cap thickness. Thermal cycling reliability of the Cu-Sn-Cu double-pillar-bump joints was also evaluated.

Keywords: Flip chip, Cu pillar bump, double pillar bump, RF package, contact resistance, chip shear force

1. Introduction

To accommodate high density and fine pitch interconnection between semiconductor chips and substrates, low cost flip chip technology has been developed by attaching semiconductor chips directly to organic substrates such as plastic ball grid array (PBGA) substrates, flexible circuit carriers, and printed circuit boards [1-6]. Low cost flip chip technology has become the trend in electronic packaging for low-cost and large-volume production of consumer goods because of the need of multiple function and better performance consumer products, in turn the need of more on-chip I/O, makes the technology attractive.

Traditionally, flip-chip bonding has been achieved by reflowing solder bumps [1,7,8] of a semiconductor chip to attach to the under bump metallurgies of a substrate. The size and pitch of solder bumps are substantially decreasing to fulfill requirement of the ever-increasing number of I/O pads. However, smaller bump size results in the decrease in the gap distance between the chip and the substrate, which may cause difficulty of unterfill

process [9]. Also, the electrical current density and the thermal energy density per bump-joint increase with reducing the solder bump size [10], deteriorating the reliability of flip-chip solder-joints. It has been also pointed out that fine pitch bonding with small solder bumps might cause the bump bridging during the solder reflow [11].

As an alternative to avoid the disadvantages of smaller solder bump for fine-pitch bonding, a flip-chip process utilizing Cu pillar bump has been extensively investigated in recent years [9-12]. Compared to the flip-chip process using solder bumps, Cu pillar bump technology can accomplish much finer pitch without compromising stand-off height and enable electronic packages to have better electrical and thermal characteristics with lower electrical resistivity and higher thermal conductivity of Cu than those of solder alloys [10]. Cu pillar bump technology, which can realize fine-pitch interconnection without decreasing the gap between a chip and a substrate, can be also utilized in radio-frequency(RF) packages for high speed communication systems, automotive radar, and high resolution medical imaging systems [13-15]. In RF

packages, the decrease in the gap distance between chip and substrate may cause deterioration of the RF characteristics due to parasitic capacitance increase. Thus, the large gap distance of the flip-chip joints as well as good mechanical reliability and low contact resistance of the joints is required for flip-chip process of RF packages.

As shown in Fig. 1, conventional Cu pillar bump consists of a solder cap on a cylindrical Cu of 50 ~ 80 μm height, and flip-chip bonding is accomplished by reflowing the solder cap on UBM of a substrate [9-12]. Photoresist patterns deeper than 50 ~ 80 μm are inevitable to form such tall Cu pillar bumps by electroplating, which may increase in the process cost of the Cu pillar bump technology. For the bump-joint structure shown in Fig. 1, UBMs on the substrate pads may be consumed severely with a prolonged reaction with the reflowed solder caps on the Cu bumps, causing deterioration of long term reliability.

In this study, a flip chip process using Cu-Sn-Cu double-pillar-bump bonding, as shown in Fig. 2, has been investigated to avoid the disadvantages of the conventional Cu pillar bump technology. Cu pillars with and without Sn caps were formed by electrodeposition and were flip-chip bonded to form the Cu-Sn-Cu double-pillar-bump joints. Contact resistances and chip shear forces of the flip-chip specimens were measured with variation of the electrodeposited Sn cap thickness. Thermal cycling reliability of the Cu-Sn-Cu double-pillar-bump joints was also evaluated.

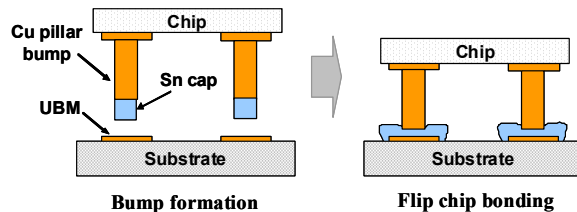


Fig. 1 Schematic illustration of the conventional Cu pillar bump structure.

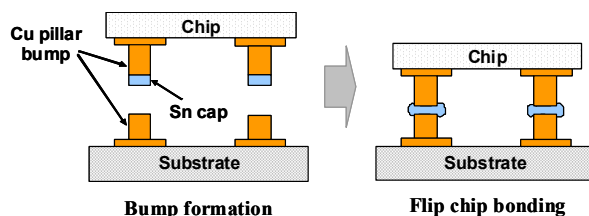


Fig. 2 Schematic illustration of the Cu-Sn-Cu double pillar bump structure.

2. Experimental Procedure

To make a chip specimen (4 mm x 4 mm size) consisted of Cu pillar bumps with Sn caps, 0.1 μm -thick Ti and 2 μm -thick Cu were sequentially sputter-deposited on a Si wafer and patterned to form 100 μm -wide metallization lines. Cu pillar bumps were electrodeposited on the Cu layer of the Ti(0.1 μm)/Cu(2 μm) metallization at a current density of 10 mA/cm². The height and the diameter of a Cu pillar bump were fixed as 20 μm and 25 μm , respectively. Table 1 lists the composition of the Cu electrodeposition solution. On top of the Cu pillar bumps, 10 μm -thick or 20 μm -thick Sn caps were electroplated using a commercial Sn electroplating solution at a current density of 10 mA/cm². To make a substrate specimen (7 mm x 7 mm size) consisted of Cu pillar bumps without Sn caps, 0.1 μm -thick Ti and 2 μm -thick Cu were sequentially sputter-deposited on a Si wafer and patterned to form 100 μm -wide metallization lines. Cu pillar bumps of 20 μm height and 25 μm diameter were electrodeposited on the Cu layer of the Ti(0.1 μm)/Cu(2 μm) metallization at a current density of 10 mA/cm².

Table 1 Composition of the Cu electrodeposition solution

Composition	Quantity (g/L)
CuSO ₄ ·5H ₂ O	62.42
H ₂ SO ₄	98
CuCl ₂	0.17
PEG	0.3
MPS	10 ppm

A chip specimen consisted of Cu pillar bumps with Sn caps were flip-chip-bonded to a substrate specimen consisted of Cu pillar bumps without Sn caps at 250°C for 1 min with a bonding force of 1 N. Microstructures of the Cu-Sn-Cu double pillar-bump joints were observed using scanning electron microscopy(SEM). The average contact resistance of the double pillar-bump joints in a flip-chip-bonded daisy-chain specimen was evaluated by measuring the daisy-chain resistance of the flip-chip-bonded specimens as a function of the number of the double pillar-bump joints. To evaluate the mechanical integrity of the double pillar-bump joints, a chip shear test was performed to measure a shear force required to separate a bonded chip from a substrate. It should be noted that underfill was not applied to the flip-chip-bonded specimens for both contact-resistance measurement and chip shear test to eliminate the effect of NCA on the electrical and mechanical properties of the joints.

3. Results and Discussion

Fig. 3 shows the SEM micrographs of Cu pillar bumps with the 10 μm -thick and 20 μm -thick Sn caps, respectively. SEM micrographs of the Cu-Sn-Cu

double pillar-bump joints after flip-chip bonding were also illustrated in Fig. 4. Thickness of the sandwich layer including Sn and intermetallic compounds between two Cu pillar bumps was maintained as about 10 μm and was not much varied with the thickness of the electrodeposited Sn cap. Instead, Sn was squeezed out between two Cu pillar bumps with increasing the thickness of the electrodeposited Sn cap from 10 μm to 20 μm .

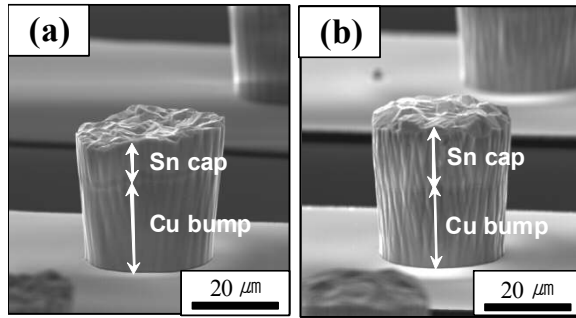


Fig. 3 SEM micrographs of the electrodeposited Cu pillar bumps with (a) 10 μm -thick and (b) 20- μm thick Sn caps.

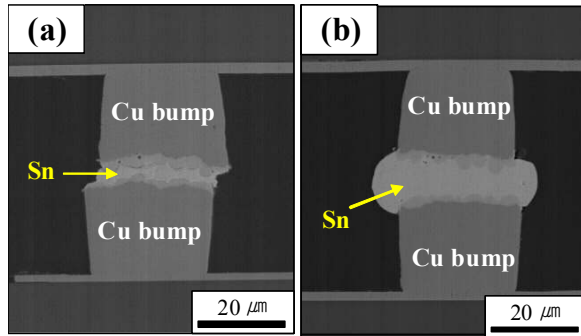


Fig. 4 SEM micrographs of the Cu-Sn-Cu double pillar-bump joints processed with Cu bumps consisted of (a) 10 μm -thick and (b) 20- μm thick Sn caps.

Average contact resistance and chip shear force of the double pillar-bump joints were illustrated in Fig. 5. With increasing the thickness of the electroplated Sn cap from 10 μm to 20 μm , average contact resistance was lowered from 13 m Ω /bump to 12 m Ω /bump and chip shear force increased from 1.6 N to 3.6 N. While improvement of the contact-resistance characteristics was minimal with increasing the thickness of the electroplated Sn cap from 10 μm to 20 μm , the chip shear force was substantially enhanced possibly due to the Sn squeezed out between two Cu pillar bumps.

Fig. 6 shows variation of the contact resistance as a function of the number of thermal cycles at temperatures between -45 $^{\circ}\text{C}$ and 125 $^{\circ}\text{C}$. In the thermal cycling test, one thermal cycle took 30 min

with maintaining for 15 min at each temperature of -45 $^{\circ}\text{C}$ and 125 $^{\circ}\text{C}$. With increasing the number of thermal cycles, the contact resistances of the double pillar-bump joints was slightly raised due to the growth of intermetallic compounds and formation of Kirkendall voids with reaction between the sandwiched Sn layer and the Cu pillar bumps [11]. Increase in the contact resistances of the Cu-Sn-Cu double pillar-bump joints could be maintained below 25% even after the thermal cycle test for 1000 cycles.

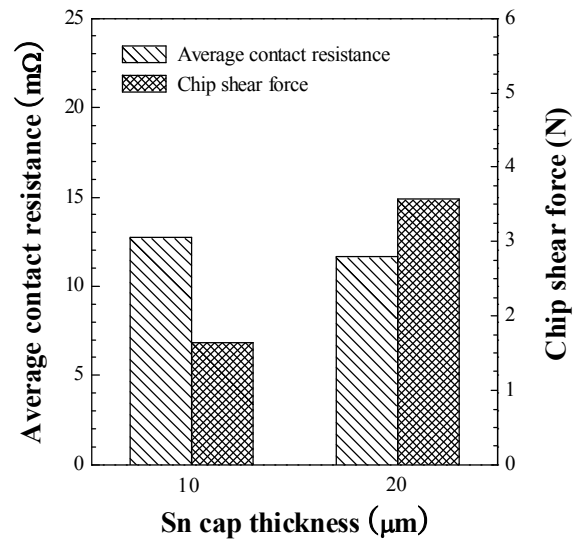


Fig. 5 Average contact resistances and chip shear forces of the double pillar-bump joints processed with Cu pillar bumps consisted of 10 μm -thick and 20- μm thick Sn caps.

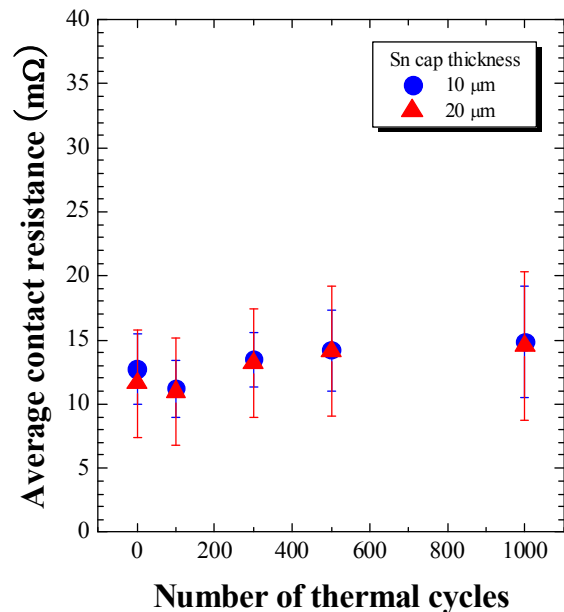


Fig. 6 Average contact resistances of the double pillar-bump joints, processed with Cu pillar bumps consisted of 10 μm -thick and 20- μm thick Sn caps, as a function of the number of thermal cycles.

Fig. 7 compares the chip shear forces measured before and after the thermal cycle test for 1000 cycles. Especially for the specimen processed with the Cu pillar bumps consisted of the 20 μm -thick Sn cap, the chip shear force was substantially reduced by the thermal cycling test. Decrease in the chip shear force could be also attributed to the interface weakening by intermetallic growth and Kirkendall void formation at the Cu/Sn interfaces of the Cu-Sn-Cu joint structure [11].

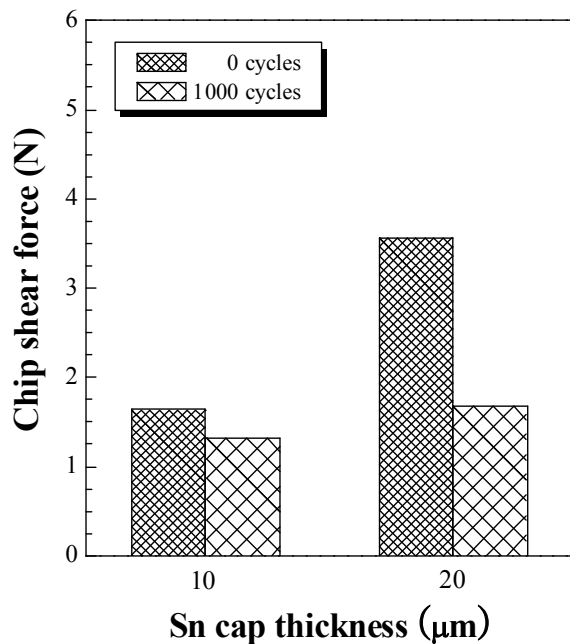


Fig. 7 Chip shear forces of the double pillar-bump joints, processed with Cu pillar bumps consisted of 10 μm -thick and 20- μm thick Sn caps, before and after the thermal cycling test for 1000 cycles.

4. Conclusion

To avoid the potential disadvantages of the conventional Cu pillar bump technology, we investigated a flip chip process using Cu-Sn-Cu double-pillar-bump bonding. Cu pillar bumps and Sn cap layers were formed by electrodeposition and flip-chip bonded to form the Cu-Sn-Cu double pillar-bump joints. Thickness of the sandwich layer including Sn and intermetallic compounds between two Cu pillar bumps was maintained at about 10 μm . The double pillar-bump joints exhibited the average contact resistances of 12 ~ 13 m Ω /bump and the chip shear forces of 1.6 ~ 3.6 N. While the contact resistance was little varied, improvement of the chip shear force was substantial with increasing the thickness of the electroplated Sn cap from 10 μm to 20 μm . With the thermal cycling test for 1000 cycles between -45 $^{\circ}\text{C}$ and 125 $^{\circ}\text{C}$, the contact resistance of the double pillar-bump joints was raised less than

25%. Decrease in the chip shear force with the thermal cycling test for 1000 cycles was 20 ~ 53%, depending upon the thickness of the electroplated Sn cap. Increase in the contact resistance and decrease in the chip shear force with thermal cycling could be attributed to the interface weakening by intermetallic growth and Kirkendall void formation at the Cu/Sn interfaces of the Cu-Sn-Cu joint structure.

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