

Underfill Selection for Flip Chip BGA Warpage Control

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Abstract

Flip chip packages are becoming more popular due to many factors such as electrical performance, functionality and high I/O interconnections. To fulfill such needs in different applications, chip sizes are gradually becoming larger. Due to the large die sizes with high pin count, small bump pitch and low-K inter-metal-dielectric material, reliability concerns are arising at the interfaces of die, solder bumps and substrate. Of concern are package warpage issues, bump cracks, underfill void/delamination/cracks and die cracks, etc. The reliability issues can be solved by selecting more appropriate underfill materials to relief mechanical stress from CTE mismatch. Many commercial brands of underfill materials are available in the market and the underfill properties such as Tg, modulus, CTE, viscosity, flow characteristics, and adhesion need to be characterized before implementation. In this project, the underfill properties are studied and discussed and stress modeling for large dice in large packages is performed. Package data such as warpage, bump crack and delamination are measured for verification. The optimum underfill material for large die flip chip packages has been implemented in mass production. [1][2]

Introduction

Due to high electrical performance demands and more functionality with high I/O needs, the flip chip packages are becoming more popular and common. To fulfill such needs in different applications, the chip sizes are gradually becoming larger. Due to large die sizes with high pin count, small bump pitch and low-K inter-metal-dielectric material, reliability concerns are arising at the interfaces of die, solder bumps and substrate. Of concern are packaging warpage, bump cracks and underfill void/delamination, etc. The reliability issues can be solved by the selecting more appropriate underfill materials

to relief mechanical stress, and therefore, material properties are becoming critical for package reliability. Many commercial brands of underfill materials are available in the market and the underfill properties such as Tg, modulus, CTE, viscosity, flow characteristics, and adhesion need to be characterized and are discussed in this paper. Stress modeling of underfill materials for large dice in large packages is performed and package data such as warpage, bump crack and delamination are measured for verification. In this study, twelve commercial underfills have been implemented and studied in a 37.5x37.5mm HFCBGA package with 17x18mm die. Two candidates out of twelve underfills with best performance will be chosen as the underfills for 21x18mm die in 42.5x42.5mm HFCBGA (device A) and 22x22 mm die in 45x45 mm HFCBGA packages (device B). Simulation modeling of stresses for large die size and package is performed and package data such as warpage, package stress and bump crack/delamination are measured for verification.

The underfill selection criteria are based on a number of performance indicators as listed in the following: Tg (temperature of glass transition), viscosity, CTE (coefficient of temperature expansion), modulus, toughness and curing conditions. These values provide only an indicator, as the actual optimized values of the parameters will depend on the type of package and specific process conditions. [3][4][5]

- Viscosity: -- Higher viscosity materials most likely have higher filler loadings which cause higher moduli and lower CTEs and may be more reliable material properties to protect solder bumps. But they may cause die cracking and lower throughput to impact mass production.
- Tg (Temperature of glass transition): -- Higher Tg materials can prevent phase changes during temperature cycling and provide better protection for solder bumps due to higher moduli. But a higher Tg induces higher warpage and higher

residual stress on components and a decreasing trend on TC performance for low-K wafers. High Tg materials get better performance in HAST test due to more robust material structures and can resist moisture penetration.

- CTE (Coefficient of Thermal Expansion): -- Low CTE is always positive but most likely it comes with higher viscosity and higher modulus which increase die cracking, high stress and warpage trends on the components. Modulus: -- High modulus can provide good protection on solder bumps but will cause high warpage and higher initial stress which increase the impact on wafers with low K materials.
- Fracture toughness: -- Higher fracture toughness is better prevention for underfill cracking and moisture penetration.
- Alpha Ray Emission: -- Low alpha ray emission is required. Since almost all fillers are synthetic, underfill materials are low alpha materials.
- Curing condition: -- Underfills need to be cured under specified curing profiles. The material properties need to be certified again for any changes in curing profiles.

Warpage, Stress and Strain Simulation

	Type	E (GPa)	α (ppm / °C)	Tg	ν
Die	Silicon	131	2.8	-	0.3
	UA	7	32 / 110	70	0.28
Underfill	UB	9.2	30 / 110	85	0.28
	UC	10	30 / 100	74	0.28
	UD	8.5	28 / 90	100	0.28
Adhesive	AD-1	8	48 / 99	75	0.35
Solder mask	SM-1	2.7	50 / 140	100	0.3
BT	BT-1	4	XY: 46 / 120	156	0.3
			Z: 47 / 155		
Copper	-	121	16.9	-	0.3
Substrate (Core)	Core-1	27	XY: 14	160	0.3
			Z: 25 / 110		
Eutectic solder	63Sn/37Pb	C0= 75.84	25.4	-	0.35
		C1=-0.15			
TIM	TIM-1	20.2	320	-	0.35

Table 1. The properties of underfill UA, UB, UC and UD for ANSYS 10.0 simulations.

Simulation for four underfill, UA, UB, UC and UD, used in large dice Heat spreader Flip Chip BGA (HFCBGA) has been done. The package is 45x45mm body size and 22x22mm die size. The table 1 shows the properties of four underfills. And the full solid model is shown in figure 1.1, 1.2 and 2.

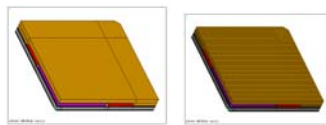


Figure 1.1 and 1.2 full solid model

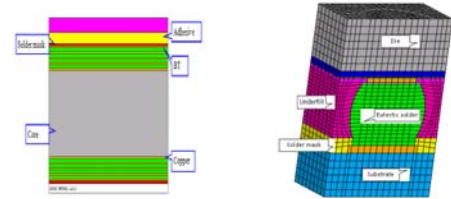


Figure 2, substrate and solder bump sub-model.

The package warpage data is shown in table 2. Package warpage with underfill UC is the smallest. The modulus of underfill UC is higher than others. I.e. the more constrain between die and underfill and its CTE is closed to soldermask's CTE, hence, the CTE mismatch is smaller than others.

Underfill	UA	UB	UC	UD
Warpage (um)	58.1	57.0	56.4	58.7

Table 2. Package warpage simulation data.

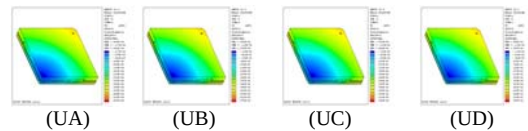


Figure 3, 1/4 Package warpage contours of using underfill of UA, UB, UC and UD.

The potential of die crack through investigation of 1st principal stress has been simulated and is shown in table 3. The stress over of package also shows in figure 4.

underfill	UA	UB	UC	UD
σ_1 (MPa)	229	254	271	213

Table 3. Package stress simulation data.

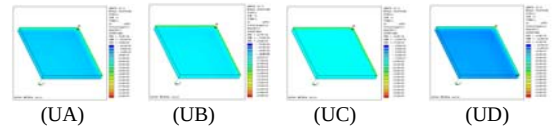


Figure 4, 1/4 Package stress contours of using underfill of UA, UB, UC and UD.

The die is immune of crack if the stress is in compressive. Figure 4 shows the σ_1 principal stress distribution on the die at 25°C. The maximum stresses are located on the corner of top surface. The stress (σ_1) of underfill UD is smallest. The high modulus of underfill is high constrained between underfill and die. I.e. the thermal stress can't be released by shear deformation of the underfill. Beside, the maximum 1st principle stress in die occurs as interface between die and underfill. The data of the potential of solder bump failure through investigating of the von Mises total strain is shown in table 4. To examine the failure of the solder bump, a sub-model for the outermost solder bump on die edge is set. Figure 5 shows contours of the strain on the critical solder bump.

underfill	UA	UB	UC	UD
Von. Mises strain	1.58%	1.66%	1.67%	1.91%

Table 4. Package strain simulation data.

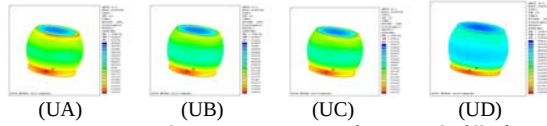


Figure 5. Package strain contours of using underfill of UA, UB, UC and UD.

The lower region close to substrate is much strain than upper region on die side. The CTE of solder bump with underfill UA, UB, UC and UD is 53.6, 48.5, 48.98 and 39.1 ppm / °C, respectively. The solder mask's CTE at 25 °C is 86 ppm/°C. The solder bump would have larger deformation in Underfill UD due to large CTE mismatch.

Overall, the Tg, modulus and CTE of underfill are major factors that cause package bigger warpage, higher stress and bump cracking issues occur.

Design of Experiments

Viscosity impacts underfill flow. A fast underfill flow is no doubt a significant improvement since the underfill process is usually the bottleneck process in flip chip assembly due to long underfill flow time especially for large die size FCBGA. It means the throughput of Units-Per-Hour (UPH) of underfill process can be significantly increased when fine filler underfill is applied in standard underfill. The elimination of flow striations is a preferred result as it means more homogenous underfill and less risk of voids, and hence better package reliability as well. For effective under filling process via capillary flow the underfill material is expected to have low viscosity at dispense temperature, low contact angle for excellent wetting to the interfaces, and high surface tension for quick capillary underfill process. Further the underfill is expected to have uniform flow front, so that no flow voids are created. There are two capillary force components in the underfill process, one is caused by the surface tension between chip and substrate that is the function of gap height (horizontally), and the other is caused by the space between solder bumps which is the function of the pitch (vertically). By considering both capillary forces, it was found that on a full array solder bump pattern, the capillary flow was actually faster for finer pitch case in some arrangement. [5]

A DOE (design of experiment) has been composed and twelve underfills from four suppliers are used for this study. The material properties are shown in table 1 and 2.

Vendor	Underfill	R1	R2	R3	R4	T1	T2
Filler Size (Avg)	Um	2	2	2	2	0.7	1.5
Filler	%	55%	60%	60%	55%	60%	65%
Viscosity	Pa.s	60	30	50	20	14	60
Tg	°C	70	85	100	135	125	120
CTE α_1	ppm/C	32	30	30	40	29	26
CTE α_2	ppm/C	110	110	110	120	98	92
Modulus (<Tg)	G Pa	7	9.2	10	7.9	7.6	10
Curing Condition	C/min.	165/90	150/ 120	150/ 120	165/90	165/90	150/ 120

Table 5-1 : Underfill properties

Vendor	Underfill	T1	T2	S1	S2	S3	V1	V2	V3
Filler Size (Avg)	Um	0.7	1.5	0.8	0.8	1	1	1	1
Filler	%	60%	65%	60%	60%	40%	65%	60%	65%
Viscosity	Pa.s	14	60	40	28	13	20	11	30
Tg	°C	125	120	118	88	140	110	115	110
CTE α_1	ppm/C	29	26	32	32	50	31	32	34
CTE α_2	ppm/C	98	92	105	100	125	101	110	98
Modulus (<Tg)	G Pa	7.6	10	6.9	6.7	4.8	9.4	7.4	8.2
Curing Condition	C/min.	165/90	150/ 120	165/ 120	165/ 120	165/ 120	165/ 120	165/ 120	165/ 120

Table 5-2: Underfill properties

HFCBGA Package with 37.5x37.5mm body size is used and the size of 65nm low-K die with polyimide passivation is 17 x18 mm. The bump composition is high lead with bump pitch 200 um. Substrate is 3-2-3 buildup substrate with 800um core thickness. Total package thickness is 2.55mm. The flip chip assembly process is shown in figure 6. The package is shown in figure 7. The wafer is high lead (Sn/Pb 95/5 %) bumped. In parallel with wafer mount and wafer saw, the buildup substrate is baked at 150C/2hours and then processed through plasma clean, chip-cap pre-solder and chip-cap mount on build-up substrate. This is followed by flip chip bonding, underfill dispensing and underfill curing, heat spreader attach and curing, ink marking, solder ball attach and solder flux cleaning, and then final visual inspection.

After flip chip assembly, the parts go through warpage measurement and multiple reflows with readout points after 3 times, 5 times and 10 times, and then going through pre-condition, and TCB test

with readout points at 200, 400, 600, 800, and 1000 cycles. The test results are shown in tables 3.

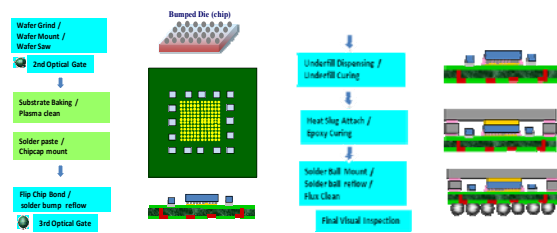


Figure 6. Flip Chip assembly process flow.

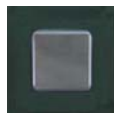


Figure 7: HFC BGA package before Heat Spreader Attach. Die size 17x18 mm is bonded on 37.5x37.5mm HFCBGA.

UF	Tg	Modulus	Warpage	Multi-Re-flow	Pre-con	TCT 200	TCT 400	TCT 600	TCT 800	TCT 1000
R1	70	7	○	○	○	○	○	○	○	○
R2	85	9.2	○	○	○	○	○	○	○	○
R3	100	10	X	○	○	○	○	X		
R4	135	7.9	X	○	X					
T1	125	7.6	X	○	○	X				
T2	120	10	X	○	○	X				
V1	110	9.4	○	X	○	○	X			
V2	115	7.4	X	X	○	○	X			
V3	110	8.2	X	○	○	○	X			
S1	118	6.9	X	○	○	○	X			
S2	88	6.7	○	○	○	○	○	○	X	
S3	140	4.8	X	○	○	X				

Table 6. Reliability test result of twelve underfills

Parts encountered underfill void / delamination or die crack or substrate popcorn and delamination as indicated by 'x', except for underfill materials R1 and R2. Both R1 and R2 passed TCT 1000cycles. The failure modes are shown in figure 8~15 – as defined in [6][7][8].

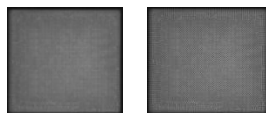


Figure 8: R1/R2 passed TCB 200, 400, 600, 800 and 1000 cycles.

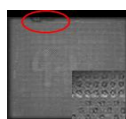


Figure 9: R3 Underfill crack and tiny delam after TCB 600.

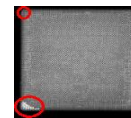


Figure 10: R4 Lower left corner delam after precondition.

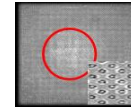


Figure 11: T1/T2 Underfill Tiny delam after TCB 200

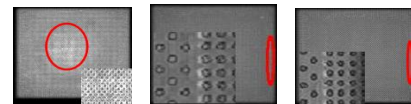


Figure 12: V1/V2/V3 Underfill tiny delam after TCB 400.

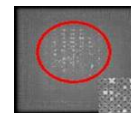


Figure 13: S1 Underfill tiny delam after TCB 200.

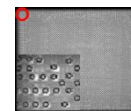


Figure 14: S2 Underfill Tiny delam after TCB 800

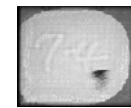


Figure 15: S3 Underfill large area delam after TCB 200.

Underfill voids are one of the most common assembly defects, which depended on the die standoff, substrate and die surface conditions, process temperature, and material properties. The solder bump is usually in the way of the material flow and it is typical to see a series of underfill voids on one side of the bumps. It is also possible that some air adjacent to a bump is trapped by the material flows from two sides of a bump. After the underfill is cured, the air bubble is left in the epoxy. For big area voids, so called underfill delamination, results from a mismatch of material properties or the surface condition of the substrate: adhesion of underfill to substrate, adhesion to die passivation, and adhesion to solder bump. Underfill cracking is another major defect mode and is a combination of high stress and die defects, such as handling damage, edge cracking and stepping from dicing. Also, underfill cracking is generally related to underfill and passivation material properties. Strong adhesion between underfill and passivation, high underfill modulus, and brittle underfill and passivation material could result in

cracking or delamination. Underfill properties contribute much to the die stress. A compliant layer such as polyimide could reduce the risk of cracking failure mode.

The small voids or delamination around bumps in R3/T1/T2/V1/V2/V3/S1/S3 were possibly the result of poor adhesion of underfill with passivation during reliability test. On S3/R4 large delamination on the die were found, the possible root cause is high Tg of underfill materials. The appropriate underfills will be selected from lower Tg for next DOE trial run.

Package warpage (CPL) data was collected for understanding the relationship of underfill properties and package warpage. Figure 16 shows that R1, R2, V2 and S2 have better coplanarity results than those underfills with higher Tg values. If the reliability data is combined with all the assembly data, underfills R1 and R2 will be considered two suitable candidates for bigger die sizes and larger package sizes. Underfill R1 and R2 were selected for further data collection, i.e. reliability and more coplanarity data.

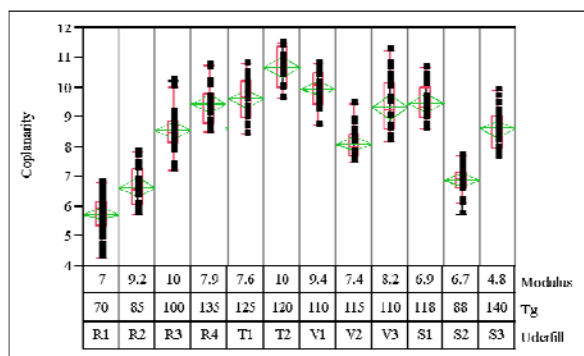


Figure 16: 12 underfill coplanarity comparison chart

Figure 17 shows the coplanarity prediction by using JMP optimization analysis. All the properties of different underfills were input and the result show that higher Tg underfill material will cause higher warpage and it fits a linear model.

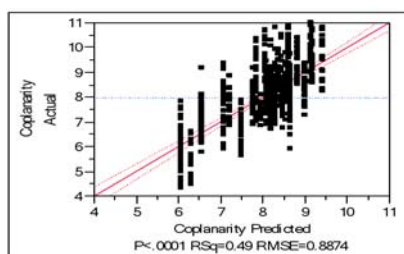


Figure 17: Coplanarity prediction chart

The prediction results in figure 18 show that if Tg is lower (about 61C) and the modulus is lower (about 4.8 Gpa), the coplanarity could have reach the lowest value.

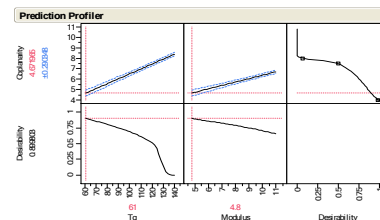


Figure 18: Warpage Prediction

Design of Experiment for Larger Dice Packages

Two candidates are used for larger die and larger package body size for the next study. The detail package information is shown in table 7. The assembly process was the same as in DOE 1.

Device	Wafer Tech.	Passivation	Bump Pitch	Bump Comp.	Die Size mm	PKG type	Heat Spreader
A	45nm	PI	170	EU	22x18	HFC BGA	ring, 1HS, 2HS
B	55nm	PI	200	EU	22x22	HFC BGA	ring, 1HS, 2HS

Table 7. Package information: Ring = stiffener, 1 pc HS = one piece heat spreader, 2pcs HS – two pieces heat spreader.

Results and Discussion

Device	underfill	Ring only		1pcs HS		2pcs HS	
		Assembly Coplanarity	Reliability TCT 1000 cycles	Assembly Coplanarity	Reliability TCT 1000 cycles	Assembly Coplanarity	Reliability TCT 1000 cycles
A	R2	X	O	O	X		O
	R1	O	O	O	O	O	O
B	R2	X	O	O	X	X	X
	R1	X	O	O	O		

Figure 19: Large die reliability test result.

(A) Ring only (stiffener) FCBGA structure:

All underfill fail at Package coplanarity (CPL) test except for underfill R1 which passed in device A. Both underfill R1 and R2 passed reliability test in device A and device B. No reliability concerns are found for R1 and R2 underfill materials. Package warpage (CPL) improvement is required.

(B) One pieces heat spreader FCBGA structure:

Underfill R1 and R2 are pass package coplanarity test in both devices. Underfill R1 pass reliability test and R2 has delamination issue after TCB test in both devices.

(C) Two pieces heat spreader FCBGA structure:

Underfill R1 passed final coplanarity test but R2 fail. Both of underfill R1 and R2 passed reliability test on device A. R2 has delamination in device B.

only R1 underfill can meet the reliability for package type A.

Conclusion

An appropriate underfill can reduce overall package coplanarity/warpage and reliability issues. To find a set of suitable underfill properties for large die size and big body side package, the fundamental understanding and the modeling data has been studied, the underfill properties, Tg, modulus and CTE, are the major indexes for underfill selection. High Tg material can prevent phase changes during temperature cycling and provide better protection for solder bump due to high modulus. But high Tg induces high warpage and high residual stress on components and has a negative effect on TC performance for low-K wafers. High Tg materials get better performance in HAST tests due to more robust material structures and can resist moisture penetration. High moduli can provide good protection on solder bumps but cause high warpage and higher initial stress which increase the impact on wafers with low-K layers. Low CTE is always positive but most likely it comes with higher viscosity and higher moduli which cause die cracking, high stress and warpage on components. Based on the material properties data, the underfill R1 was selected as the underfill material to solve coplanarity and reliability issues of large die sizes and large body size packages.

Acknowledgments

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