

Reduction of Signal Line to Power Plane Coupling Using Controlled-Return-Current Transmission Lines

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Abstract

In printed circuit boards, transmission of high-speed digital signals is achieved using single-ended or differential transmission lines, typically using a microstrip or stripline configuration. This requires continuous reference planes, which is difficult to maintain in multilayered IC packages or boards. As a result, the signal return current may need to flow between different reference planes due to a cut-out in the reference plane or a signal via transition. The uncontrolled path of the return current results in signal integrity and electromagnetic interference problems. We propose a new controlled-return-current transmission line design to reduce this problem. Our approach is based on guard traces to help control the return currents.

Keywords: Return path discontinuity, signal integrity, ground plane, microstrip over slot

I. INTRODUCTION

In most printed circuit board (PCB) designs, improving the signal integrity (SI) helps to reduce electromagnetic interference (EMI) as well. One such case is the edge radiation from the power planes of a PCB at high frequencies. There are various sources for a noisy power plane such as the current demand of the core logic of a microprocessor. This noise is typically filtered at high frequencies by the IC package and numerous decoupling capacitors on the IC, package, and board. Another source of noise on the power planes is the high-speed I/O signals. When such a signal is coupled to the power planes, it can create high-frequency noise and unpredictable crosstalk between distant transmission lines. This noise is magnified in the presence of simultaneously switching I/O drivers, but even a single I/O link may have signal integrity problems if it is coupled to a power plane.

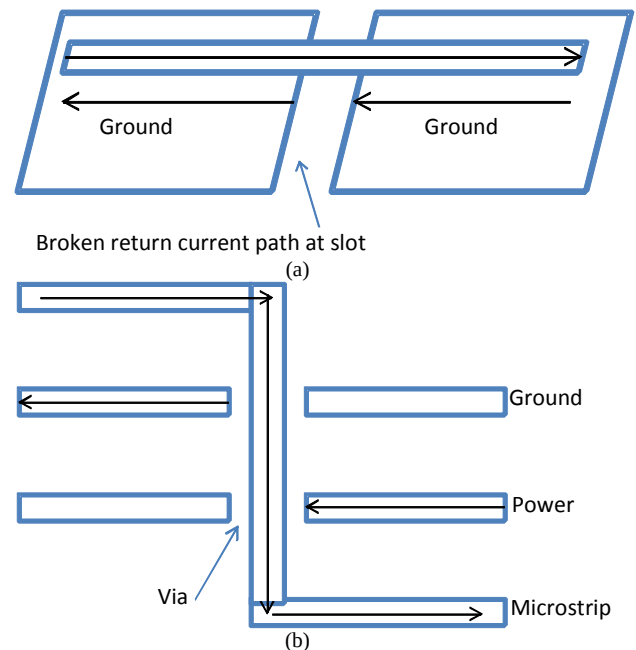


Fig. 1 Return path discontinuities due to a (a) slot; (b) via transition in microstrip lines. The arrows show the direction of currents.

In printed circuit boards, transmission of high-speed digital signals is achieved using signal ended or differential transmission lines, typically using a microstrip or stripline configuration. This requires continuous reference planes, which is difficult to maintain in multilayered IC packages or boards. As a result, the signal return current may need to flow between different reference planes due to a cut-out in the reference plane or a signal via transition as shown for the example of a microstrip line in Fig. 1.

The return path discontinuity due to vias, and its affect on signal integrity has been shown for various via transitions in [1, 2]. In case of a microstrip line via transition, if both reference planes carry the same DC voltage, they can be shorted using vias to provide a low-impedance return path [3]. If the reference planes have different potentials, such as shown in Fig. 1(b), additional planes can be used in the layer stack-up to control the return path, but this may not be acceptable due to thickness considerations and additional cost [4, 5]. Note that decoupling capacitors are only effective up to a few 100 MHz to provide a low-impedance return path. To reduce the effect of non-ideal return paths, differential signalling can be used, but even for differential signals, the return path discontinuity needs to be considered [6]. In addition to the signal integrity problems, the coupled noise to power ground planes can significantly increase the electromagnetic radiation from the board [7, 8].

In this paper, we present a new transmission line design, called Controlled-Return-Current Transmission Line (CRCTL), to overcome the SI and EMI problems due to return-path discontinuities. In the new design, a low-impedance return path is achieved by making use of guard traces. Guard traces have been used before to reduce crosstalk. In this paper we use them for a totally new purpose – to control the return currents.

In the next section we present the details of CRCTL.

II. CONTROLLED-RETURN-CURRENT TRANSMISSION LINES

The new CRCTL design is shown in Fig. 2(b). The conventional via design as shown in Fig. 2(a) has the major drawback that the return current has to jump between the power and ground planes around the via hole. This causes a return-path discontinuity. In the new CRCTL design approach, we do not only design the signal line, but also design its return path. In the new design, the guard traces along with the additional ground vias help to provide an alternative path for the return currents so as to minimize the coupling between the microstrip and parallel-plate modes. A proper design of the guard traces and ground vias can eliminate the coupling between the signal line and the power plane by providing the return currents of the bottom microstrip line solely on the guard traces.

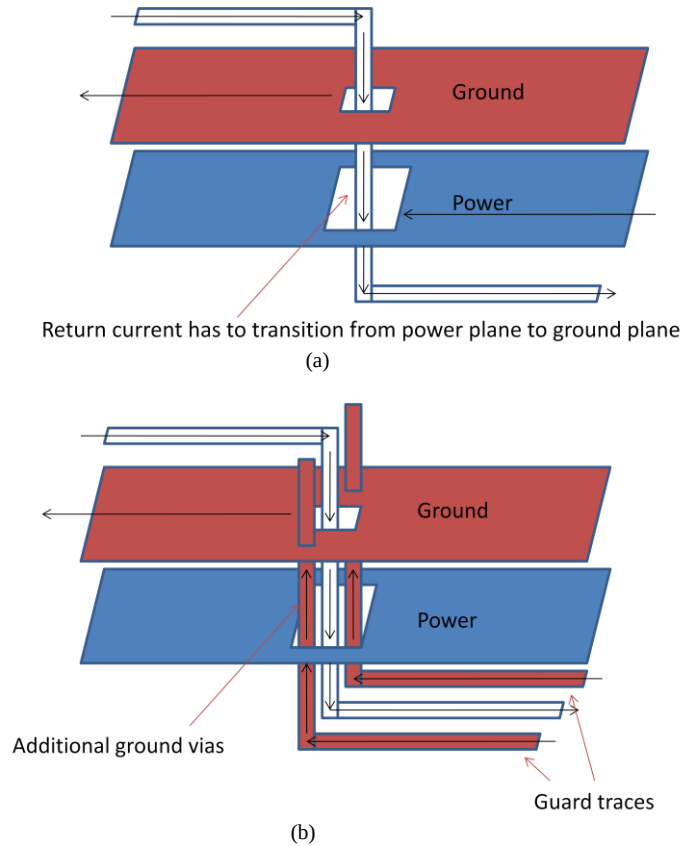


Fig. 2 Current paths shown using arrows for (a) typical via design; (b) new CRCTL design.

III. NUMERICAL RESULTS

To investigate the performance of the CRCTL design, we considered the example shown in Fig. 3. In this example, a microstrip line with a width of 300 μm on the top layer is connected with a microstrip line on the bottom layer. A second via connects the bottom microstrip line with another microstrip line on the top layer. The dielectric substrate has a dielectric constant of 4.5 and a loss tangent of 0.025. The power and ground planes have a length of 3.4 cm and width of 3 mm. The S-parameters of this 3-cm long transmission line including the two via transitions was extracted using the full-wave EM simulator Sonnet¹.

¹ Sonnet version 11.56

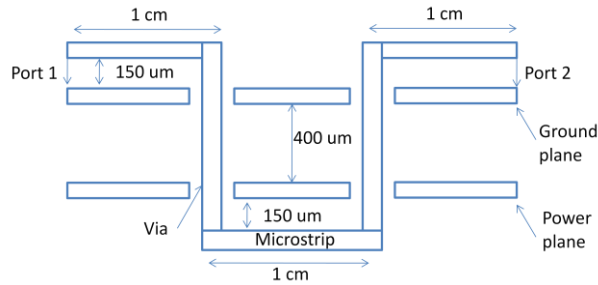


Fig. 3 Side view of the via transition that was simulated using EM solver.

Next, the same transmission line was simulated using additional ground vias and guard traces making use of the CRCTL design approach. The 3D view of the CRCTL design is shown in Fig. 4. The two small micro vias at both ends of the transmission line represent the ports of the simulation and do not actually short the signal line to the ground plane in the simulation.

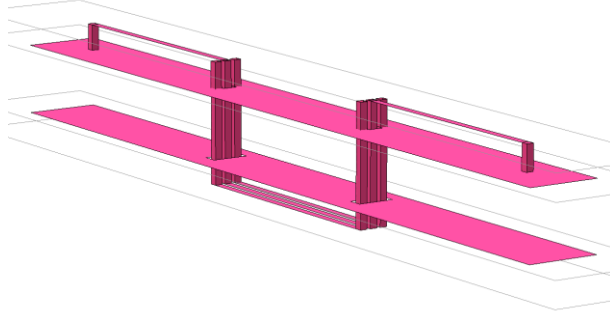
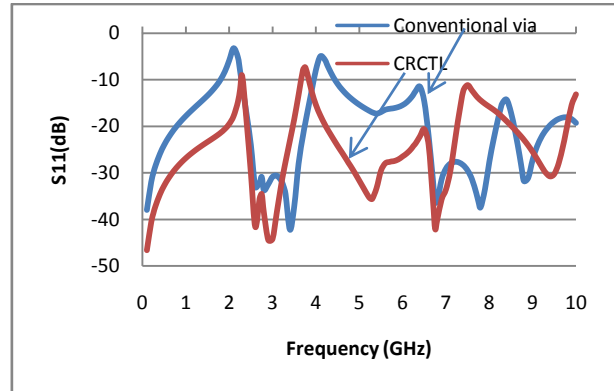


Fig. 4 3D view of the CRCTL via transition having the same dimensions as in Fig. 3 (dielectric thicknesses and via heights are not up to scale).

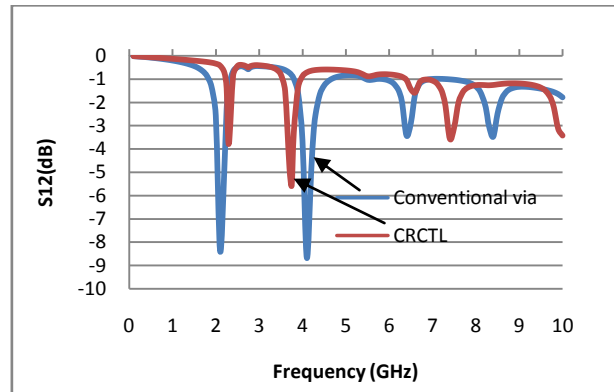
The simulated S-parameters are shown in Fig. 5. Significant improvement can be seen when the CRCTL design is applied. The reflection loss is improved by about 5-10 dB for most frequencies up to 7 GHz. The maximum insertion loss is also improved by about 3 dB.

Although there is significant improvement, resonance can still be observed in the CRCTL S-parameters, indicating that the coupling between the transmission line and power plane is not completely eliminated. There are two possible reasons for this coupling. First, the bottom microstrip line with the guard traces is not optimized for a 50-Ohm impedance. Ideally, the two guard traces should behave as the negative net of a differential pair, where the positive net is the bottom microstrip line. So the differential impedance of this pair should be about 50 Ohm. In Fig. 4, note that all the microstrip lines and guard traces have the same width, which results in a differential impedance considerably higher than 50 Ohm. The second main reason for the coupling is the via transition, which has several parameters (e.g., number and location of return vias, via

clearances, etc.) that can be tuned to reduce the mode conversion around the via hole.



(a)



(b)

Fig. 5 The simulated S-parameters comparing the structures in Fig. 3 (conventional design) and Fig. 4 (CRCTL).

To further investigate the effect of the differential impedance formed by the bottom microstrip line and the guard traces, a second simulation was done where the width of the guard traces was doubled to 600 μm in order to reduce the differential impedance closer to 50 Ohm. The new CRCTL design with wider guard traces provided an additional 1-2 dB improvement in insertion and reflection loss for most frequencies. To investigate the coupling between the signal line and the power planes, a third port was defined on one corner of the power plane on the side of port 1. Fig. 6 shows the isolation between port 1 and port 3. The CRCTL design considerably improves the isolation, about 5 dB for most frequencies up to about 7 GHz. Using wider guard traces also slightly improves the performance of the CRCTL as shown in the figure.

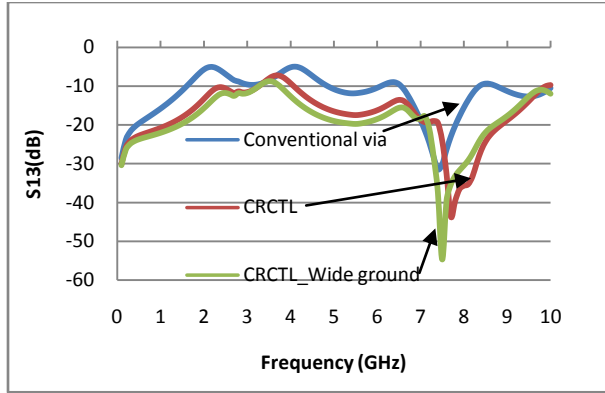


Fig. 6 Coupling between signal line and power plane due to a via transition.

IV. EQUIVALENT CIRCUIT MODELS FOR CRCTL

Equivalent circuit models have been developed for the considered via transitions. For the conventional via design, the equivalent circuit model is shown in Fig. 7. Note that a 4-terminal microstrip transmission line model is required to be able to simulate this structure. The TLINP4 model, which provides a 4-terminal model for a lossy transmission line, in ADS² has been used in this example. Note that the two microstrip lines on the left and right represent the signal lines on the top layers, whereas the microstrip line in the center of the figure represents the signal line on the bottom layer. The reference terminals of the microstrip lines have to be correctly connected to either the power terminal (P) or the ground terminal (G) of the power/ground plane model at the appropriate locations.

Based on the geometrical and materials properties, the microstrip lines have a characteristic impedance of 48.2 Ohm and an effective dielectric constant of 3.43. The power/ground plane pair has been modeled using a parallel-plate transmission line model due to its thin structure. The characteristic impedance of the parallel-plate transmission line was extracted as 23 Ohm using the analytical equation $Z_0 = \sqrt{\mu/\epsilon}d/w$, where μ is the permeability, ϵ is the permittivity, d is the dielectric thickness (400 μ m), and w is the width of the power plane (3 mm).

The equivalent circuit model as shown in Fig. 7 was implemented in ADS. The scattering parameters were calculated and compared against full-wave simulation results obtained previously using Sonnet. As an example, Fig. 9 shows the comparison of both simulation results for the magnitude of S12, where excellent agreement can be observed.

For the modeling of the CRCTL design, the guard traces need to be considered as well. They can be

modeled using microstrip transmission line models with proper connection of the reference terminals to the power plane as shown in Fig. 8. The comparison between the equivalent circuit model and the full-wave EM simulation using Sonnet is shown in Fig. 10. The agreement is good up to about 7 GHz. The deviation in results at high frequencies may be due to the coupling between the guard traces and microstrip line, which has not been included in the circuit model. Note that the parasitic inductance and capacitance of vias have not been included in the equivalent circuit models, since the fundamental effect of the via transitions in the considered cases is not the via parasitics but the abrupt discontinuity in the return currents.

The presented equivalent circuit models can be used to develop a better understanding of the return path discontinuities in conventional vias or CRCTL designs. For example, the CRCTL model in Fig. 8 indicates that at a via transition, the return current of the bottom microstrip line can be provided by the guard traces or the power/ground planes. This suggests that the CRCTL design may be further improved by interrupting the return current on the power plane, for example by removing a portion of the power plane close to the via.

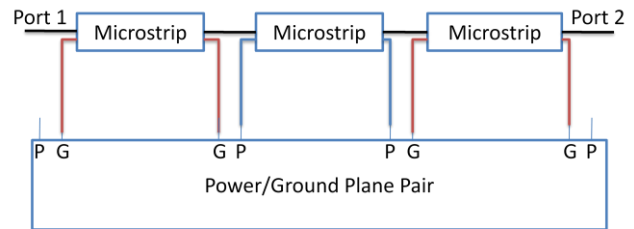


Fig. 7 Equivalent circuit model for the conventional via transition shown in Fig. 3.

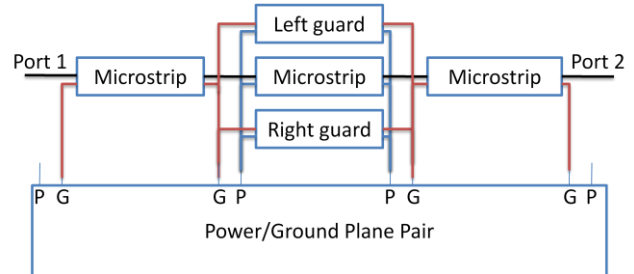


Fig. 8 Equivalent circuit model for the CRCTL shown in Fig. 4.

² ADS from Agilent Technologies, Version 2008 Update 2

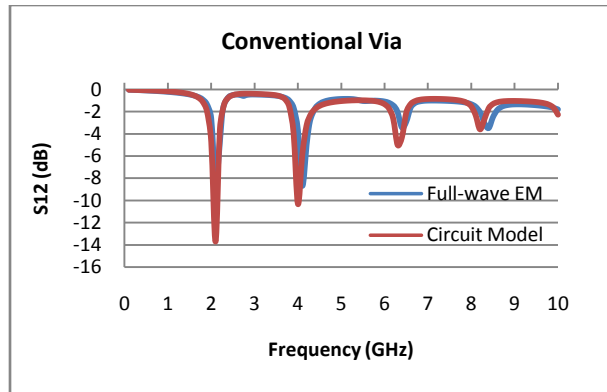


Fig. 9 Comparison of the equivalent circuit model in Fig. 7 with the full-wave simulation result for the conventional via structure.

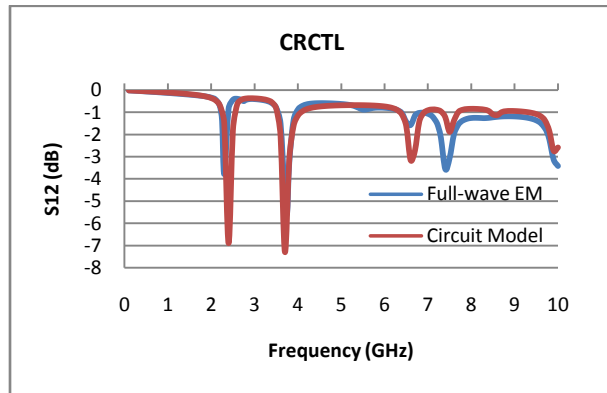


Fig. 10 Comparison of the equivalent circuit model in Fig. 8 with the full-wave simulation result for the CRCTL design.

V. CONCLUSION

In high-speed PCB designs, high-speed nets are designed using transmission lines, but typically not much care is given to the return path assuming that the return currents will be able to return back to the source by means of a nearby decoupling capacitor or by means of the parasitic capacitance of the power planes. None of these approaches work for high-frequency signals due to the parasitic inductances, and the coupled high-frequency signals in the power/ground planes result in increased EMI and SI problems.

In this paper, we show for the first time a controlled-return-current transmission line (CRCTL) design. We emphasize that it is essential to design the return path together with the signal path for a high-speed transmission line. This is especially true for single-ended lines, which are more receptive to power/ground noise.

The new CRCTL demonstrated improvement compared to a conventional via design in suppressing

the coupling between the signal lines and power plane at a via transition. We expect to further improve the CRCTL design by fine-tuning its parameters such as the number and location of the ground vias, via clearances, and the spacing and width of guard traces.

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