

Comprehensive Multilayer Substrate Models for Co-Simulation of Power and Signal Integrity

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Abstract

Physics-based via and trace models have been integrated into a general method to simulate multilayer board structures. In the past, our approach has been successfully applied to link simulation and has been validated against other numerical techniques and measurements. A notable improvement of the computation speed of over three orders of magnitude has been observed when compared to full-wave electromagnetic simulations.

In this paper, the models are reviewed and it is shown that they can also be applied to simulate power distribution networks with arbitrary power/ground via and plane configurations. This approach is general enough to handle indistinctively power and signal nets and it is therefore suitable for co-simulation of both power and signal integrity domains in a comprehensive and efficient manner. Different configurations are studied in this paper, including also decoupling capacitors, and the simulation results are compared against full-wave simulations in terms of accuracy and efficiency.

Key words: Interconnects, Multilayer Substrate, Physics-based Models, Power Integrity, Signal Integrity, Via Model.

I. Introduction

Multilayer substrates such as packages or printed circuit boards (PCBs) are widely used to interconnect different components like memory and processing units of electronic systems in the Gigabit/s range. The power distribution network (PDN) –defined by the power vias and planes– and the signal nets –formed by the signal traces and the vias to interconnect different levels– become tightly coupled at high frequencies. Signals traveling over vias penetrate the power planes and excite parasitic modes supported between adjacent power planes (Figure 1). This mechanism offers a coupling path between power and signal nets and leads to signal and power integrity problems. The prediction and mitigation of this interaction in an early design stage is difficult to achieve due to the high density and complexity of typical interconnect systems.

Diverse numerical (e.g. [1-2]) and semi-analytical techniques (e.g. [3-4]) have been proposed in the past addressing the problem of efficient modeling and simulation of off-chip interconnects.

In previous works of the authors, physics-based models have been proposed to describe the via

transitions [5-8] and the traces connecting them [9-10]. These representations have been incorporated into a general method to simulate multilayer substrates, which has been validated against diverse numerical techniques and measurements [10]. The main advantages of this approach are:

- The models are concise and general enough to handle an arbitrary number of elements. The chosen partitioning approach allows a clear definition of interfaces interconnecting the model building blocks. This makes it possible to develop a better insight into the physics of the problem and to evaluate the contribution of the different model components.
- The models can be computed mostly using analytical formulae. This provides a very good numerical efficiency and enables the simulation of complex structures.
- The models can be parameterized and they are therefore appropriate for fast prototyping and optimization studies.

In this paper, the models are used to study the interaction between signal and power nets. It is shown that this technique is suitable for simulating the response of structures with mixed reference planes

and other PDN elements, such as decoupling capacitors (decaps).

The paper is organized as follows. Section II explains the models and the simulation method for multilayer structures; Section III shows an application example and compares the results against the ones obtained with a full-wave electromagnetic field solver; Section IV explores different via configurations and the effect of decoupling capacitors, focusing on the interaction between signal nets and the PDN; Finally, Section V draws the conclusions.

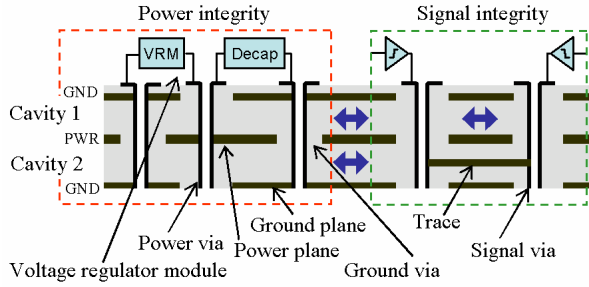


Figure 1: Conceptual description of the signal and power integrity domains and their main components for multilayer substrates (two cavities are illustrated).

II. Modeling Approach

The modeling approach makes use of a cavity-based partitioning strategy and the assumption that vias provide the only coupling path between cavities. Hence, the via segments crossing a resonant cavity formed between two adjacent power planes constitute the basic elements to be described. The physics-based model [5-7] portrays this via transition by means of two mechanisms: the parallel-plane impedance (Z_{pp}) and the via-to-plane capacitance (C_v).

The parallel-plane impedance [5] models the current return path for vias, which at the same time is associated with the excitation of parallel-plane modes inside the cavities formed between power planes. For multiple vias, Z_{pp} becomes a matrix with entries defined at each via location. Diverse techniques can be used to compute Z_{pp} ; analytical formulations are available for regular board shapes (e.g. cavity model [11-12]) and special cases (e.g. infinite planes [13]). Since the cavities are usually very thin in comparison to the shortest wavelength of interest, Z_{pp} corresponds to a planar (2D) solution. The impedance matrix needs then to be expanded in order to provide the upper and lower cavity ports that are required to handle multilayer structures [8].

Vias crossing a power plane through a clearance hole (antipad) induce a near-field that is normally not modeled by Z_{pp} . This near-field interaction between the via barrel and the antipad rim is instead approximated as a displacement current that can be mapped to an equivalent capacitance [5-6]. Analytical formulae [14] or quasi-static solvers can be used to compute these via capacitance values.

The models have been extended to account for internal traces connecting vias by describing the transition in terms of two modes, namely, the parallel-plane mode and the trace transmission line mode. Since the two modes need to be properly matched at the via positions, the modal decomposition technique presented in [15] has been applied to derive a more general formulation of the models [9]. It can be demonstrated that an arbitrary number of via transitions in a single cavity, with or without traces, can be represented in terms of microwave network parameters, according to the following Y-parameter expression [10]:

$$\begin{bmatrix} \mathbf{I}_u \\ \mathbf{I}_l \end{bmatrix} = \begin{bmatrix} \mathbf{Y}_{vu} & \mathbf{0} \\ \mathbf{0} & \mathbf{Y}_{vl} \end{bmatrix} + \begin{bmatrix} +\mathbf{Y}_{pp} & -\mathbf{Y}_{pp} \\ -\mathbf{Y}_{pp} & +\mathbf{Y}_{pp} \end{bmatrix} + \begin{bmatrix} -\mathbf{k} \cdot \mathbf{Y}_d & \mathbf{0} \\ \mathbf{0} & (\mathbf{k} + \mathbf{1}) \cdot \mathbf{Y}_d \end{bmatrix} + \begin{bmatrix} (\mathbf{k}^2 + \mathbf{k}) \cdot \mathbf{Y}_d & -(\mathbf{k}^2 + \mathbf{k}) \cdot \mathbf{Y}_d \\ -(\mathbf{k}^2 + \mathbf{k}) \cdot \mathbf{Y}_d & (\mathbf{k}^2 + \mathbf{k}) \cdot \mathbf{Y}_d \end{bmatrix} \cdot \begin{bmatrix} \mathbf{V}_u \\ \mathbf{V}_l \end{bmatrix} \quad (1)$$

where the vectors $\mathbf{I}_u$, $\mathbf{I}_l$, $\mathbf{V}_u$, and $\mathbf{V}_l$ denote the currents and voltages defined at every via location, for the upper (u) and lower (l) sides of the cavity.

The first Y-matrix term in (1) stands for the via capacitances. $\mathbf{Y}_{vu}$ and $\mathbf{Y}_{vl}$ are diagonal matrices with entries $Y_{vi} = 1/Z_{vi} = j\omega C_{vi}$, accounting for the upper and lower capacitances of the i -th via. The second term corresponds to the expanded parallel-plane admittance matrix, where $\mathbf{Y}_{pp} = \mathbf{Z}_{pp}^{-1}$ is the planar parallel-plane admittance matrix. The third and fourth Y-matrix terms are result of the modal transformation and they are valid for vias connected to striplines. $\mathbf{Y}_d = \mathbf{Z}_d^{-1}$ is the planar admittance matrix of the traces inside the cavity, modeled either as a coupled or uncoupled multi-conductor transmission line system. The modal decomposition matrices are a function of the factor k , defined for the n -th via-stripline transition as $k_n = h_{ln} / (h_{ln} + h_{un})$, with h_{ln} and h_{un} the heights from the trace to the lower and upper plane inside the cavity, respectively [15]. For the calculation of k the trace thickness is neglected.

Figure 2(a) shows the model schematic representation for a single cavity bounded by a top ground plane and a bottom power plane. On the right side, two vias connected by a trace are represented, where the blocks denoted as T stand for the modal transformation matrices.

For power/ground vias, the model described in (1) is still applicable, provided that the connectivity of the vias to the planes is incorporated. As shown in Figure 2(a) left side, when a via is connected to a power plane, the via capacitance in the model is replaced with a short circuit. This simple consideration allows the modeling of structures with arbitrary power/ground via and plane configurations.

As previously illustrated in Figure 1, the interaction between the power and signal domains is modeled by means of the parallel-plane impedance. Additional elements such as decoupling capacitors can also be included into the cavity description by placing their network representation in the position corresponding to their physical location.

The models discussed so far constitute a stand-alone network block describing a single cavity. The general method to simulate multilayer structures involves the computation of each plane pair and the combination of the partial results for each cavity by ensuring current and voltage continuity at the connected ports [10], as depicted in Figure 2(b). Segmentation techniques [16] are applied here to perform this task.

III. Simulation Example and Correlation to Full-Wave Simulation

The example to be discussed in this section is detailed in Figure 3. Two differential links, each of them formed by four through-hole vias and a differential stripline, are routed on a six cavity substrate with mixed power and ground planes. The fourth plane is defined as a power plane, whereas the other six are assigned to be ground planes. Additional ground and power vias are placed in the vicinity of the signal vias, for a total of 28 vias. Ports were defined on top of the 8 signal vias (ports 1 to 8) and two additional ports were included as observation points on top of power vias (ports 9 and 10).

The simulation of the example was performed using both the presented physics-based models and a finite-element based full-wave solver [17]. The results obtained with the two techniques, some of them displayed in Figures 4 to 7, show good agreement in magnitude and phase.

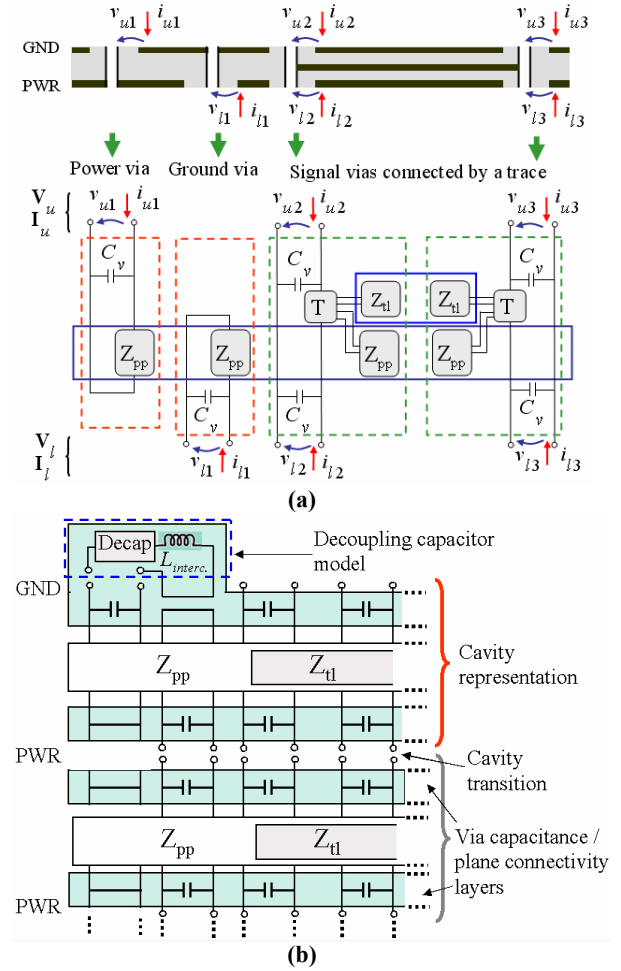


Figure 2: Schematic representation of the models. (a) Network representation of different via types in a single ground-power cavity. (b) Model concatenation for multilayer substrates.

For instance, it can be observed in Figure 4 that both the model and the full-wave analysis predict a worse differential transmission parameter for the second link (ports 3 to 6). This is due to the position of the traces at a higher level with respect to the other link. The longer via stub shifts the notch in the transmission to lower frequencies.

The configuration selected can also be used to study the interaction between signal and power nets and consequently to explore the two main mechanisms responsible for noise injection in multilayer structures: the currents being injected or supplied by the PDN to other devices such as ICs, and the crosstalk between signals routed on the substrate [18].

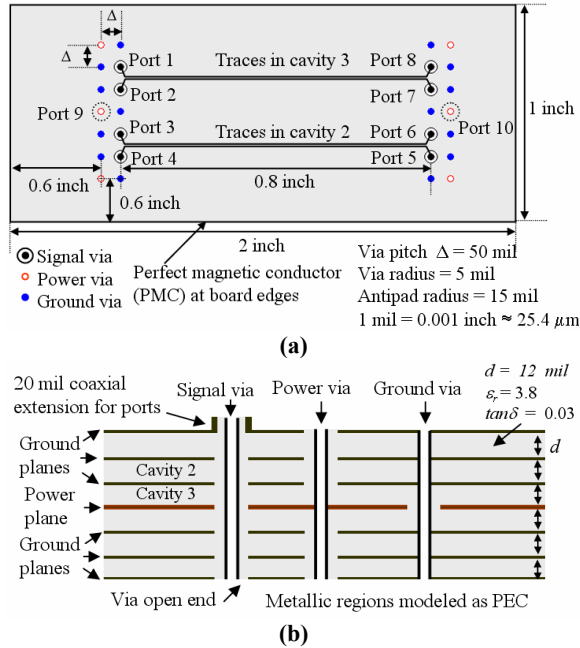


Figure 3: Multilayer example for two differential links routed on a multilayer substrate with mixed reference planes (one power plane). (a) Upper view. (b) Cross section.

Figure 5 shows the single-ended crosstalk between a power (port 9) and a signal via (port 2), and between two signal vias (ports 3 and 2). Here, the crosstalk between the power and the signal nets tends to be larger in comparison to the crosstalk between two signal nets for frequencies below 14 GHz. The transfer function between ports is influenced by several factors such as position or isolation due to ground vias [19]. The difference observed in the current example can be explained by the fact that the signal via is located farther from port 2 and the trace guides a portion of the signal to other elements, which reduce the crosstalk. However, both coupling mechanisms between vias are significant enough to degrade signals in the Gigahertz range. The results have been also translated into the time domain using an inverse Fourier transform. The impulse responses for the signal at port 2, due to a 1-V 100-ps Gaussian pulse applied at the PDN port 9 and the signal port 3, are plotted in Figure 6. The induced voltage amplitudes, up to 2 % and 0.5 % of the input pulse, may not be negligible, in particular if it is considered that in a real scenario the total noise is a result of the simultaneous interaction of many nets.

Another possibility to analyze the results is to display them in terms of generalized mixed mode S-parameters [20], in order to evaluate the impact of differential or single-ended signaling.

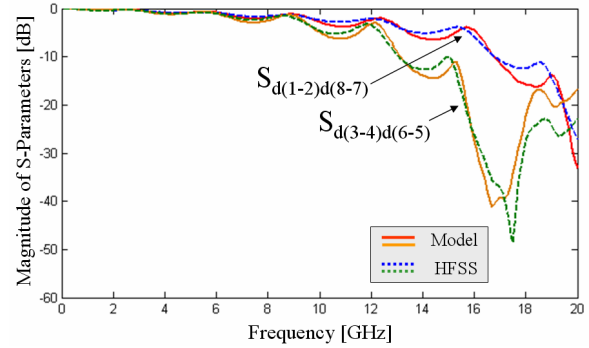


Figure 4: Simulated differential transmission for the two links of the structure shown in Figure 3, obtained with the proposed models and full-wave simulation.

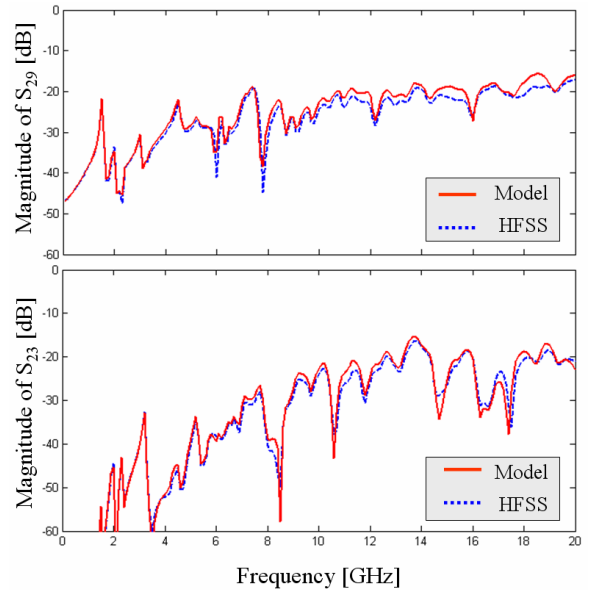


Figure 5: Single-ended crosstalk between a power and a signal via, and two signal vias, according to the port definition of Figure 3. The graphs show the results obtained with a full-wave analysis and the physics-based models.

Figure 7 shows the crosstalk and the impulse response from a power net (port 9, single-ended *se*) to a differential pair (ports 1-2, common mode *c* and differential mode *d*). The plots indicate that the differential-mode signaling can improve noticeably the immunity to noise, at least considering ideal differential sources.

The proposed method, applied to obtain the previously discussed results, shows not only good accuracy but also a very good efficiency. The simulation of the test structure took about 21 seconds for 200 frequency points in Matlab, running on a 3.0-GHz CPU with 4 GB RAM. The computation of the

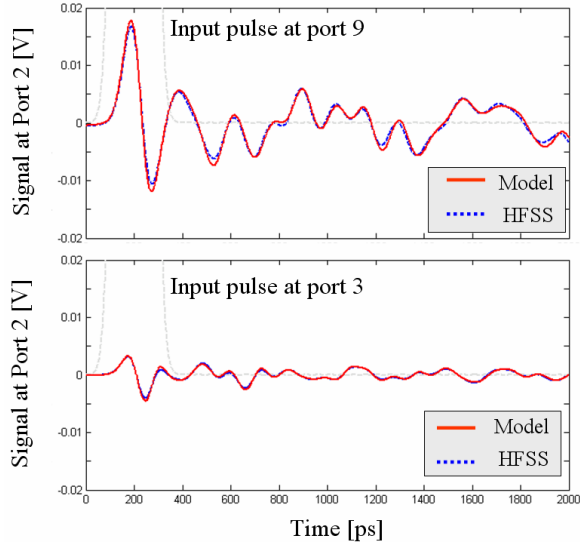


Figure 6: Impulse response at port 2 for a 1-V 100-ps full-width-half-maximum Gaussian pulse applied at port 9 and port 3, respectively. The graphs show the results obtained with a full-wave analysis and the physics-based models.

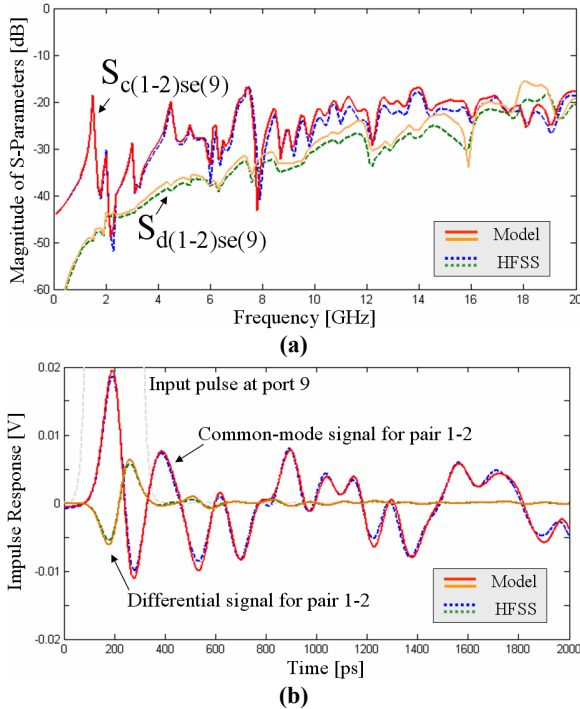


Figure 7: Differential and common-mode interaction between a signal and a power net. (a) Differential-mode and common-mode crosstalk. (b) Impulse response at pair 1-2 for a 1-V 100-ps full-width-half-maximum Gaussian pulse applied at port 9. The graphs show the results obtained with a full-wave analysis and the physics-based models.

parallel-plane impedance was done once using the cavity model with a single-sum implementation [21] and 100 iterations per impedance term. The capacitances were calculated analytically using the formulation in [14], adding a 20 fF capacitance to compensate the fringing fields at open via ends. In contrast, the elapsed time for the full-wave analysis exceeded 40 hours using 8 adaptive passes for a target convergence of 2% and 200 frequencies, running on the same computer. This represents a factor of about 6800 difference.

For the physics based method, however, if every cavity is different and a separate computation of Z_{pp} is required per layer, the simulation time can become longer. For the studied case, the analysis considering an independent computation per cavity took about 94 s. Nevertheless, this still represents an improvement of the computation speed of over three orders of magnitude.

IV. Application of the Models

The outstanding efficiency of the physics-based models makes it possible to study many different configurations in a short time. Hence, this technique is, as mentioned before, suitable for engineering studies, fast prototyping and optimization of relatively complex structures.

As an extension to the example discussed in the previous section, the power and ground via configurations are here being modified in order to quantify the impact of ground vias, according to the cases shown in Figure 8. The simulation of the new configurations took approximately 9 s, 12 s, 40 s, and 180 s for case I (16 vias), case II (20 vias), case IV (42 vias) and case V (90 vias), respectively. The port definition, geometrical and material parameters correspond to the ones defined for the previous example in Figure 3, which is now case III.

The crosstalk for different power/ground configurations is plotted in Figure 9. For cases I and II the predicted crosstalk is larger due to the small number of ground vias. In contrast, for cases III, IV and V the results show a very similar crosstalk level between the power and the signal port. A similar trend can be observed for the crosstalk between the signal nets in cases IV and V. By taking a closer look at the configurations, it can be stated that larger crosstalk variations occur when the via near environment is significantly altered (i.e. nearest neighboring vias). This suggests that vias placed further away only have a weak influence on the

response. This experiment shows that adding many power/ground vias will not always lead to a noticeable improvement on the response and that it is important to select carefully the position and number of such vias.

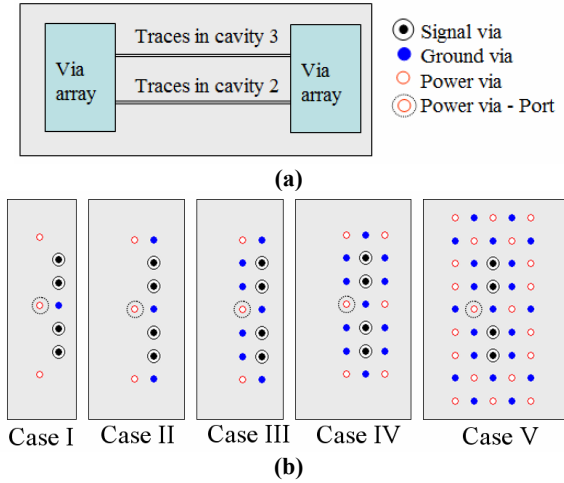


Figure 8: Alternative configurations to the reference case in Figure 3 (case III). (a) Link definition. (b) Via array configurations (same array used at both link sides).

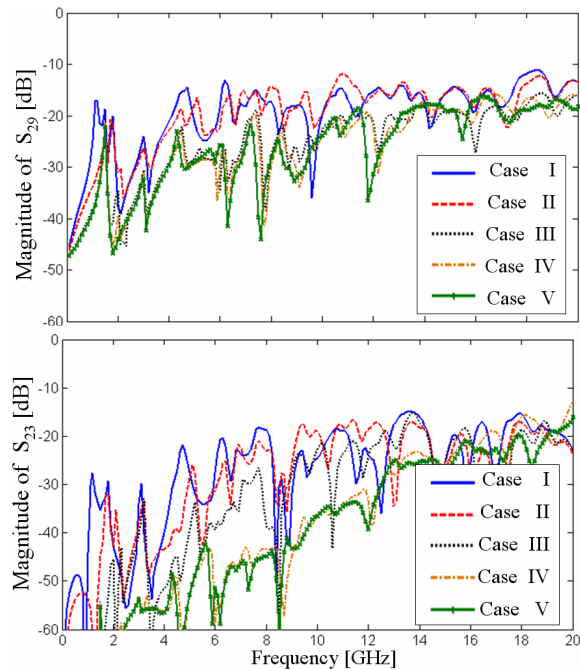


Figure 9: Crosstalk between a power and a signal port and two signal ports, for the power via configurations indicated in Figure 8 and estimated with the proposed models.

Another alternative to reduce the coupling between vias through the power planes involves the utilization of surface decoupling capacitors. These capacitances can be incorporated into the simulation method as additional network elements connected on top of the power vias (Figure 2(b)).

For the current set of examples, decoupling capacitors were connected on top of all power vias, with exception of the observation ports 9 and 10. These elements were modeled as a RLC network to represent the capacitor equivalent series resistance (ESR), the equivalent series inductance (ESL), and the inductance of external interconnects required to place the capacitor on top of the vias ($L_{interc.}$) [22]. It was assumed that all the capacitors have the same value ($ESR = 100 \text{ m}\Omega$, $ESL + L_{interc.} = 2 \text{ nH}$, $C = 10 \text{ nF}$).

The decoupling effect is more often visualized in terms of Z-parameters. Note that the impedance reduction due to decaps can be related to a crosstalk reduction between signal and power vias as well. Figure 10 shows the transfer impedance between two power vias with 4 decaps in case III, 10 in case IV, and 38 in case V. For the studied cases, the effect of the capacitors is observable mainly at frequencies below 1 GHz. The cavity resonant frequencies are located at relatively high frequencies because of the board size in this example, which leads to a poor decoupling. A stronger decoupling is also difficult to achieve due to the small cavity thickness. Nonetheless, the results indicate that more capacitors help to increase the equivalent capacitance and to reduce the equivalent inductance, increasing the maximum frequency where the decoupling may be effective. The resonance located below the first plane resonance, arising when decaps are placed, is a result of the introduced parasitic inductances.

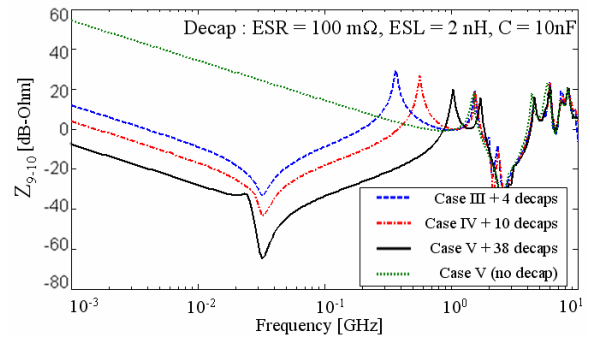


Figure 10: Effect of decoupling capacitors on the transfer impedance between two power vias, for different configurations of Figure 8 and a different number of decoupling capacitors.

In Figure 11 is shown the effect of the parasitics associated with decoupling capacitors for the case V in discussion. Different positions of the power plane are simulated, with and without considering ESR, ESL and $L_{interc.}$. The graph shows that pure capacitances connected to the second power plane can provide the largest reduction of the plane impedance at higher frequencies. The decoupling effect is reduced when the power plane is changed to a deeper layer. When the ESR, ESL and $L_{interc.}$ are added, the decoupling effect tends to further diminish. The distance to the plane and the parasitic elements associated with surface capacitors make effective decoupling in multilayer environments difficult [23].

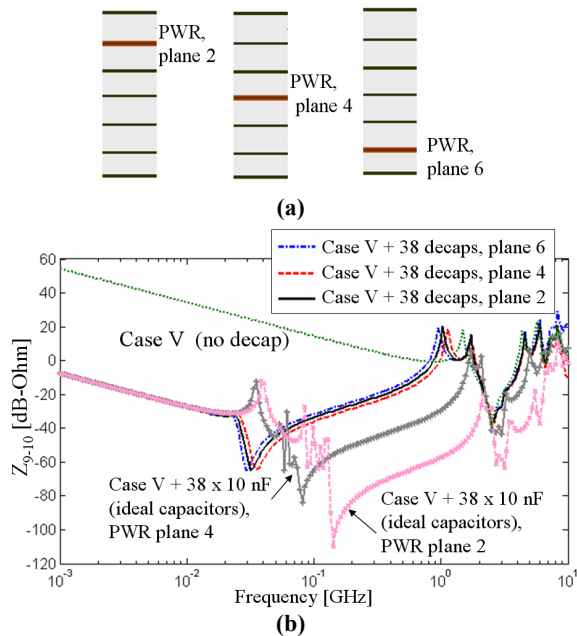


Figure 11: Effect of parasitic elements associated with decoupling capacitors. (a) Power plane configurations tested. (b) Transfer impedance between two power vias for different power plane positions and capacitor values. The decap was modeled as an RLC network with $ESR = 100$ m Ω , $ESL + L_{interc.} = 2$ nH and $C = 10$ nF. The two impedance lines with markers consider ideal capacitors (no ESR/ESL/ $L_{interc.}$)

Figure 12 shows the time-domain impulse response at port 2 for an input applied to the power via at port 9 and the signal via at port 3, for cases I, III, and V. An amplitude reduction of the output signal can be seen as the number of ground vias is increased, in particular between cases I and V. In

addition, the response for case V with 38 decaps was included on the graph; however, the decoupling in the studied case for a 1-V 100-ps pulse propagating to a signal via is not very effective, mainly due to the parasitics associated with the capacitor and their connection, which should be considered to model a realistic scenario.

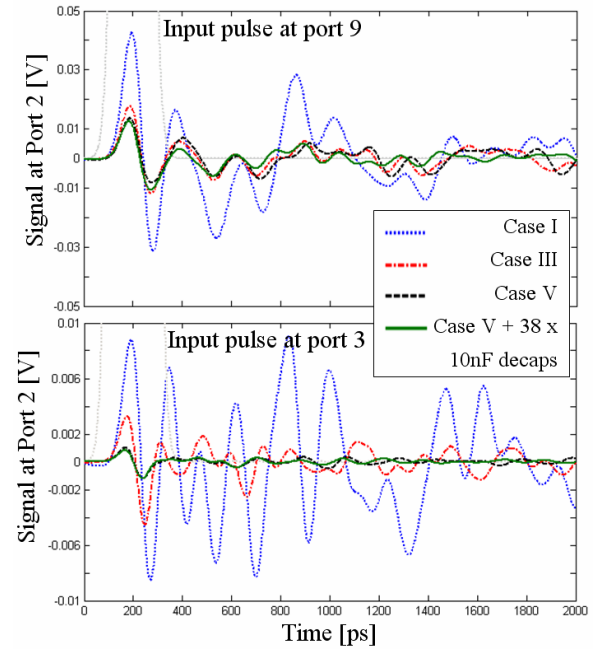


Figure 12: Impulse responses for different power/ground via configurations of Figure 8, and one decoupling capacitor scheme ($ESR = 100$ m Ω , $ESL + L_{interc.} = 2$ nH). A 1-V 100-ps full-width-half-maximum Gaussian pulse was used as input signal.

V. Conclusion

Efficient physics-based via and trace models have been presented for simulation of multilayer substrate interconnects. Good agreement for the results was observed with respect to full-wave simulations, with a drastic improvement of the computation speed of over three orders of magnitude. It has been shown in several examples that the method is suitable for co-simulation of the power and signal integrity domains in a comprehensive and efficient manner. Future work will have to explore the model limitations for board discontinuities, such as split planes, or very dense arrays, and the application of the method for cases having a very large number of elements.

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