

Full-Wave Electromagnetic Characterization and Measurement of Wirebond Transitions on High Temperature Co-fired Ceramics (HTCC) and Low Temperature Co-fired Ceramic (LTCC) Substrates For Broadband Package Designs

Jerry Aguirre, Marcos Vargas, Jason Bast, David O'Neill,
Steve Hira, Chen Wang

Kyocera America Inc., 8611 Balboa Avenue San Diego CA 92123
Phone: 858.576-2691; Fax: 858.573-0159; Email: jerry.aguirre@kyocera.com

Abstract:

This paper presents the full-wave electromagnetic characterization and measurement validation up to 50 GHz for single and double wire bond transitions on laminated multilayer ceramic substrates. Microstrips and grounded coplanar waveguides (CPWG) are fabricated on one low temperature co-fired ceramic (LTCC) substrate, having nominal dielectric constants of 6, and on one high temperature co-fired ceramic (HTCC) substrate, having a dielectric constant of 8.8. The transmission lines are designed to have a characteristic impedance of 50 Ohms and have varying gap distances between the two probe-fed ends. The gaps range from 4 mils to 100 mils and are connected by a wire bond. The wire bond shape is found to have a significant impact on RF performance at the higher frequencies. Correlation between measured performance and model simulation is also impacted by wire bond shape. The increased improvement in RF performance for a two-wire bond transition is simulated, measured, quantified and finally extended by simulation for the three-wire bond case. Results demonstrate improvements in performance are rapidly approached after two wire bonds. We extend the simulation models for chip-to-substrate wire bond transitions to quantify maximum package speed based on wire bond length, chip pad size, chip material, and return path configuration. The simulation models include silicon as the chip material, and two different return path configurations: microstrip and differential.

Introduction

The bandwidth requirements for the electronic package continues to increase seemingly unabated. This trend is driven by the constantly increasing on-chip computational speed, which places demanding broadband performance on each component in the high-

speed channels. To improve the performance, the components along the entire electrical interconnect must first be characterized and understood.

For multi-Gb/s transceiver systems, the key constraint on the overall performance is identified as the package [1]. The key high-speed bottle necks in the performance of the package are the PWB-to-package transition and the package substrate-to-die transition. Because of the high inductance and high impedance associated with the wire bond package-to-die transition, it is usually the critical bottleneck in the overall package electrical performance. The package substrate itself could have very broadband performance, but the high frequency effects of the wire bond assembly will eventually dominate and degrade the signal integrity of the package, and hence, the overall system. Since wirebonding is still the most common assembly method for chips in packages, it is important to first understand the limitations imposed by this die assembly method.

There are some conceptually straightforward and simple methods for mitigating the effects of the wire bond, either by adjusting the length to compensate for the chip input capacitance [2], or by adding capacitive features at the bond pads on the chip and package to compensate for the inductance of the wire bond [3]. However, these approaches to improve package performance only help at the lower frequencies of the signal spectrum. By implementing improved design methodologies using impedance compensating discontinuities for the signal and return path currents, existing wire bond capabilities can be implemented for 40 Gb/s and possibly higher speed applications [2].

Once the key factors contributing to the bottle necks are identified, new processes and/or materials can be developed for optimum performance. However, before relying on, or considering the development of

new processes, or assembly methods, the full characterization of the wire bond transition must be undertaken. Other work has considered similar wire bond characterization [4,5,6] to understand the limits of this first-level wire bond interconnect. In this work two test substrates, using two different ceramic technologies, were fabricated to establish correlation between a commercial full-wave electromagnetic analysis tools (HFSS) and our assumptions on wire bond assembly process. Both microstrip and CPWG traces were printed with gaps varying from 4 mils to 100 mils. Standard design guidelines were implemented for all via sizes, via pitches, and trace widths and spacings. The gaps were wirebonded by both one and two wirebonds.

For the test substrates two bonding methods are available: wedge-to-wedge bonding and ball bonding as shown in Figure 1. The basic steps of wire bonding include the first bond (usually on the chip), the wire loop (formed by bonding machine), and the second bond (usually on the substrate). Ball bonds are formed by bonding a spherical ball to the die / substrate pad using thermal and ultrasonic energy. Wedge bonds are formed using a combination of ultrasonic action and pressure from the bonding head to the die / substrate surface. Ball bonding is faster, more accurate, and also more repeatable in controlling loop shape than wedge bonding, but wedge bonding can achieve the lowest loop height. Due to the wedge bond shape and low loop height this method is preferred in high frequency applications and therefore used as the bonding method for this paper.

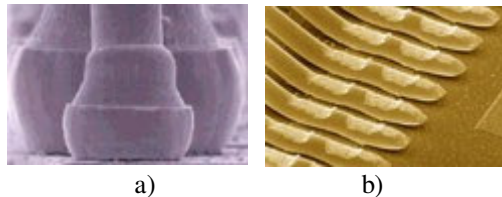


Figure 1 a) Ball bond, b) wedge bond

Once the wire bond assembly process is well characterized, generalizations and decision tables for wire bond length vs. application speed can be generated by simulation. All wire bond features, from shape to loop height, to pullback of wire bond on metallization can be parameterized and simulated. In all the assumptions we consider that the second level interconnect is not the first bottle neck encountered in the overall electrical link performance and is omitted for first order assessment of package speed limitation.

Correlation Study – Measurement Vs. Full-Wave Simulation

Accurate assessment on the impact of wirebonds on package performance for an arbitrary configuration depends on first closing the gap between a measurement

and simulation of a simple model. The accuracy of today's full-wave EM solvers have been repeatedly established. Careful measurements can be regarded as the touchstone of accuracy for such full-wave tools. The real challenge is obtaining correlation between accurate measurements and full-wave simulations. Where a gap exists between these two characterizations, a means to determine the source of the error must be established. Either there are model and simulation nuances in the solvers that must be resolved, or model assumptions are incorrect because the actual wire bond shape, connecting transmission line to wire bond dimensions, material properties, or a combination of several factors are different than the simulation models.

Figure 2 shows the two substrates fabricated and included for this correlation study. Figure 2a is an Kyocera A473 alumina test substrate. The dielectric constant for this alumina is 8.8. Coplanar and microstrip structures are shown on the far right area of the substrate. Calibration thru-lines and ring resonators were also fabricated. Similarly, in Figure 2b, the same structures with minor dimensional adjustments to account for a different dielectric constant was fabricated in Ferro A6M. Figure 2c, shows the typical wire bond scheme for the various gaps between the microstrip and CPWG transmission lines: 4 mil, 25 mil, 50 mil, 75 mil and 100 mils.

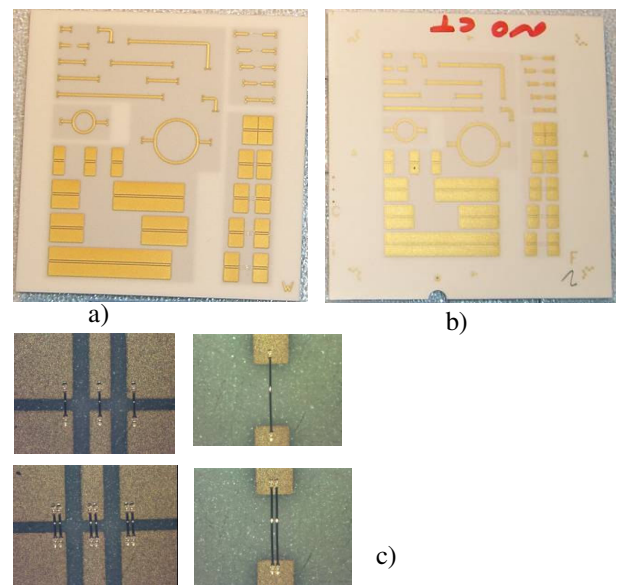


Figure 2 a) A473 test substrate, b) A6M test substrate, c) typical wire bonds

In considering the two materials for a wire bond study, the emphasis is not necessarily on the material property differences, but upon the combination of material process properties and design guidelines, i.e. conductor thickness, tape thickness, minimum trace width and spacing, tape tolerance, permittivity variation, and other particular attributes of the material technology. Considering all of the tradeoffs between the number of degrees of variation for each material and

each type of transition is beyond the scope of this paper, and left as future work. Variation and material properties are considered second order factors to assembly, however they may warrant further investigation for higher frequencies and finer correlation between simulation and measurements.

The first step is to develop a finer understanding of the material and assembly variations as they might relate to electrical performance. For example, consider the two ceramics discussed in this paper. We assume that the wire bond assembly variations are the same for all substrates. For alumina A473, a discrete range of tape thicknesses are available for constructing multilayer structures. For Ferro A6M, an LTCC material technology has two standard available tape thicknesses to construct multilayer structures. Table 1 shows a comparison of dielectric constant along with tape thickness available for fabricating 50 Ohm lines.

Table 1

Material	Dielectric constant	Substrate Height	CPWG 50 Ohm Width and spacing	MS 50 Ohm Width (mil)	available tape thickness (mil)
A473	8.8	12mil	9, 5.5	15	5, 6, 8, 10
A6M	6	14.8mil	13, 4	25.75	3.7, 7.4

Figure 3 shows the solid models used to correlate with measurements. It is expected that CPWG will outperform MS transitions since the high impedance associated with the wire bond transition is lower for the CPWG case as two adjacent wirebonds are connected to ground.

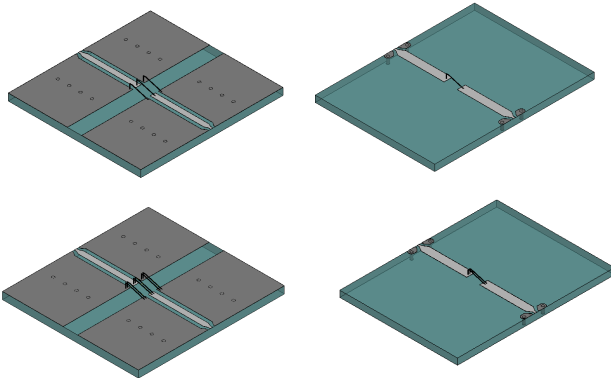


Figure 3 CPWG and microstrip models for parametric analysis.

Figure 4 and 5 shows the return loss and insertion loss for the A473 CPWG single wire bond measurement at all the gaps. As can be noted the correlation in return loss is fair to good depending on the dimension of the gap. As the gap dimension increases the correlation between simulation and measurement improves. This trend is also shown in the comparisons for the insertion loss. However, it is also clear that the correlation takes a marked turn for the worse just past 10 GHz. For the 4 mil gap a field plot as shown in Figure 6, it is clear that the wire bond transition is setting up a slot mode in the CPWG structure. In the full-wave model,

this mode is being absorbed by the problem space boundary conditions whereas in the actual substrate measurement, the energy meets a finite ground plane/ceramic interface. Hence nearby structures become a strong factor in the measurement and correlation to simulation is not good past 10 GHz. The result of this measurement identifies a potential pitfall in models for full-wave simulation and also highlights a limitation of CPWG transitions. The authors are aware that better grounding schemes can potentially remove this limitation, however it is highlighted as a potential pitfall in CPWG wirebond transition designs.

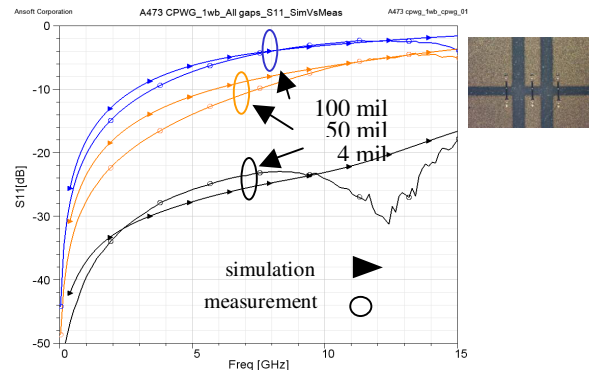


Figure 4 Return Loss for 4, 50, and 100 mil single wirebond transition on CPWG in A473

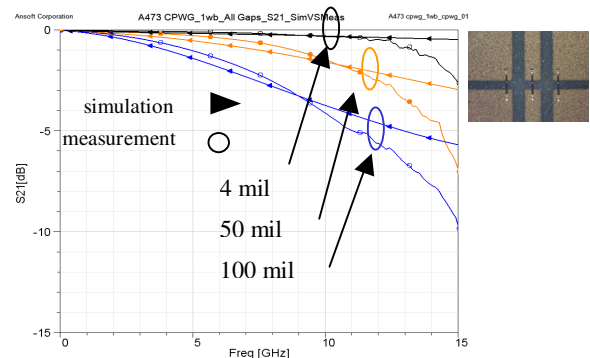


Figure 5 Insertion Loss for for 4, 50, and 100 mil single wirebond transition on CPWG in A473

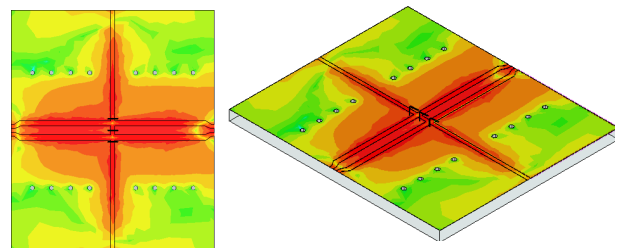


Figure 6 Field plot showing excitation of slot modes

Figures 7 and 8 shows the comparison between measurement and simulation for a microstrip line with a single wire bond connected across the gaps. The return loss correlation again shows improved correlation

between simulation and measurement for the wider gap cases. The correlation between measurement and simulation for the insertion loss shows very good correlation out to approximately 40 GHz. Beyond 40 GHz, to 50 GHz, the correlation is still good except for the 4 mil gap case where the simulation predicts more insertion loss.

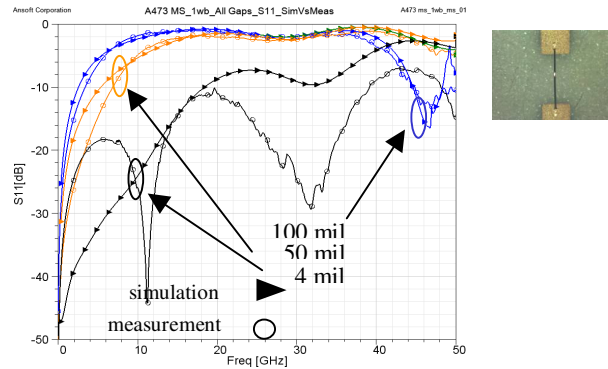


Figure 7 Return Loss for 4, 50, and 100 mil single wirebond transition on microstrip in A473

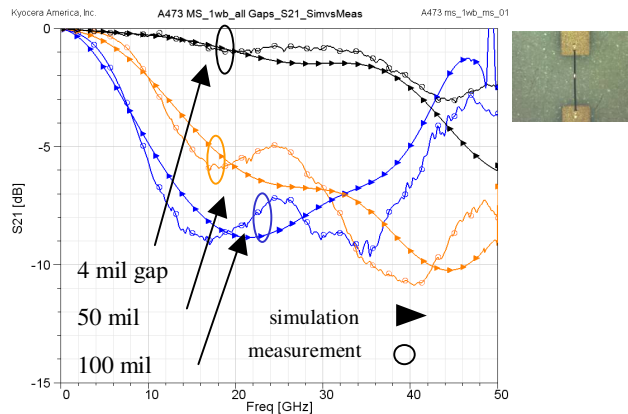
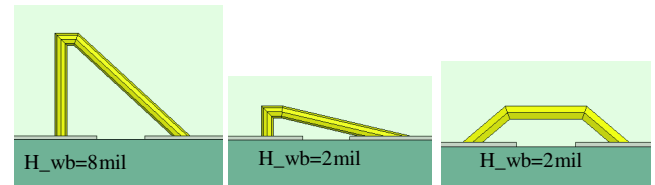


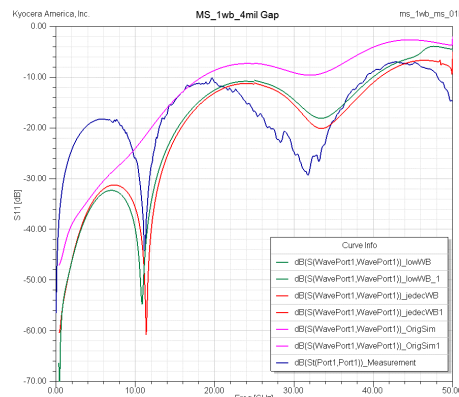
Figure 8 Insertion Loss for 4, 50, and 100 mil single wirebond transition on microstrip in A473

The wire bond shape appears to matter most for the case where the dimensional features of the discontinuity are a significant fraction of the discontinuity and the assumptions of the wire bond are off by a significant fraction of the relative dimensions of the discontinuity. To investigate the source of the discrepancy between simulation and measurement for the 4 mil gap case a series of simulations were run with different assumptions on the wire bond shape as shown in Figure 9a. The original model was a library Jedec standard wire bond model available in the simulation software. For the wedge bond we know that the loop height is on the order of 2 mils. Figure 9b shows the new simulations overlaid on measurement. The gap in level of return loss remains significant, but the characteristic shape and depth of resonance at 10 GHz is revealed as the wire bond shape

approaches a minimum wire bond height. It is left as future extension of this work to develop cross-sections to determine exact wire bond shape and loop height. For the wider gap cases, we also know that the wirebond loop height increases, and hence the correlation between simulation and measurement improves as the loop height becomes higher and our models are a closer match to actual part measured.



a)



b)

Figure 9 a) three wire bond models and b) corresponding return loss simulations compared to measurement.

Figure 10 shows the return loss for the A6M substrate test wire bonds. Again very good correlation for the wider gap is shown. Also, the drop out in correlation at around 19 GHz for the CPWG case is again shown in the insertion loss curves shown in Figure 11.

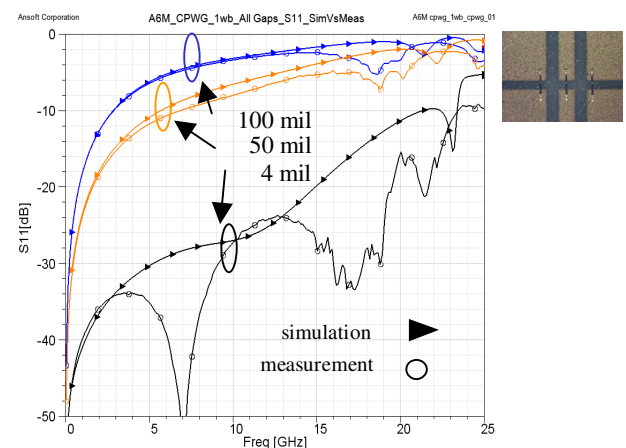


Figure 10 Return Loss for 4, 50, and 100 mil single wirebond transition on CPWG in A6M

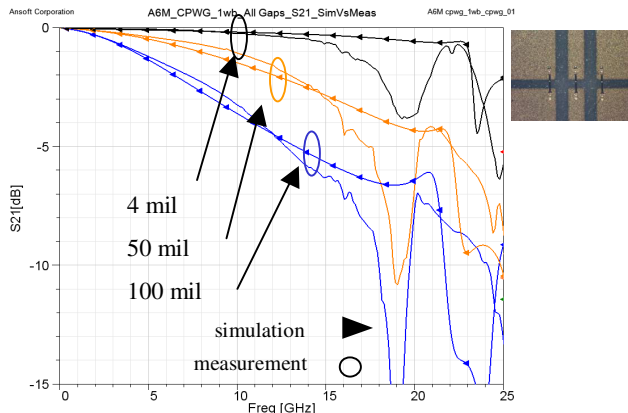


Figure 11 Insertion for 4, 50, and 100 mil single wirebond transition on CPWG in A6M.

Figures 12 and 13 show measurement and simulations for the A6M substrate from 0 to 50 GHz for the single wire bond case. Correlation for the longer wire bonds is excellent out to 50 GHz. Again, the 4 mil gap shows the greatest discrepancy, but as before we believe it is due to the wire bond height in the models.

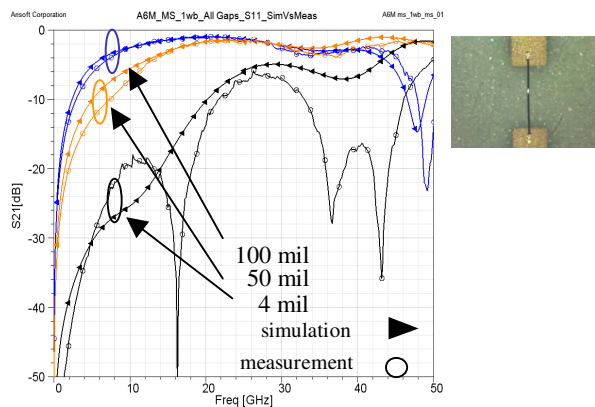


Figure 12 Return loss for 4, 50, and 100 mil single wirebond transition on microstrip in A6M

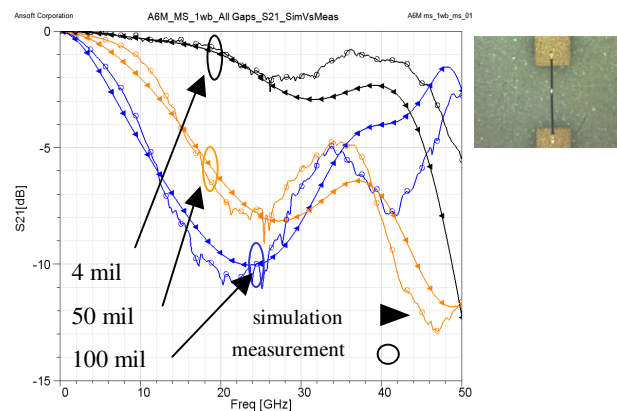


Figure 13 Insertion Loss for 4, 50, and 100 mil single wirebond transition on microstrip in A6M

Characterization of Typical Die-Package Wire bond Transitions

Once the correlation of measurement and full-wave simulation of wire bond transitions is established and used to understand the sensitive parameters and geometries of the wire bond, the task of determining the relationship between the speed of a package and wire bond length can begin systematically by full-wave simulation alone. Ideally, a set of curves and or tables can be generated that relate an upper frequency for a specific performance tied to a specific wire bond length. However, as is well understood, the return path currents and any discontinuity compensation become significant and important inputs into determining this upper frequency bound. Nonetheless, because of material technology standards and assembly requirements it is possible to constrain the number of variables to those typically found in packaging structures.

To illustrate this approach, and without loss of generality, A6M is considered as the material to illustrate this goal. Figure 14 shows the oblique and side view of the wire bond transition models to compare two transmission lines: a differential pair and microstrip. The die is GaAs ($\epsilon_r=12.9$) and 8mil thick. The substrate is Ferro A6M ($\epsilon_r=6$ and $\tan\delta=0.0013$) with a thickness of 14.8mil. A PEC pedestal is used to elevate the die and keep its top surface flush with the substrate top surface. The substrate was chosen to be two 7.4mil tape layers to correspond with the substrate model used for the correlation phase. The thicker substrate allows for a wider trace, thus, enabling double or triple wire bonding schemes. The die conductors are perfect electric conductors representing a lossless load. The substrate conductors are Ferro Gold with a $\sigma=1.31 \times 10^7$ S/m.

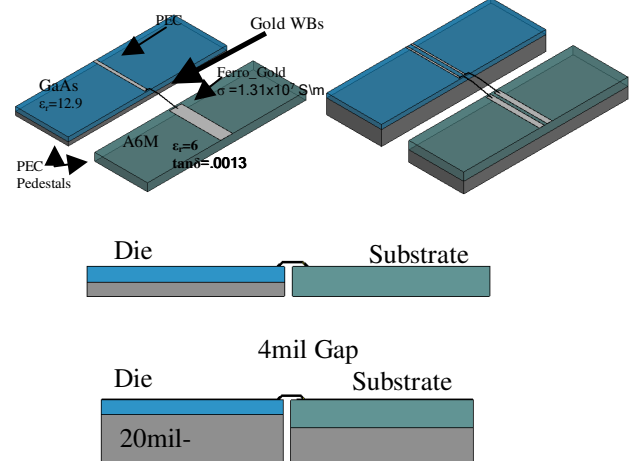


Figure 14 Single ended and differential pair models

The model for the microstrip-wire bond-microstrip transition has trace widths of 5mil and 21mil for GaAs and A6M, respectively, for 50 Ohm conductors. A single 1-mil diameter gold wire bond spans the gap. Absorbing boundary conditions are used around the air box enclosing the air box. The bottom of the air box has a PEC boundary representing the ground plane and return path in the package. For a differential impedance of 100 Ohms, the die differential pair uses 3mil wide conductors with a 6.5mil spacing and the substrate differential pair uses 9 mil wide conductors with a 5.25mil spacing. A single 1-mil diameter gold wire bond connects the traces across the gap.

The simulations consisted of (1) varying the gap between the die and substrate and (2) varying the height of the pedestals for both the die and substrates, while maintaining the top surfaces flush. Two gaps, 4mil and 50mil, and two pedestal heights were simulated. Increasing the gap increases the wire bond height, length, and shape producing a high impedance discontinuity. Increasing the pedestal height increases the return path, which similarly increases the impedance of the discontinuity. The 4mil and 50mil gaps have 15.7mil and 62.9mil wire bond lengths, respectively. From the correlation work, it was determined that the 4mil gap had a 2mil wire bond height and the 100mil gap had a wire bond height of 10mil. Thus, for the three remaining gaps (25mil, 50mil, and 75mil), a 2mil step in wire bond height was applied resulting in 4mil, 6mil, and 8mil wire bond heights for the corresponding increasing gaps. Both the microstrip and differential pair models were simulated from 0.1 to 25GHz using an interpolative sweep in HFSS.

Typical Transition Simulation Results

Insertion loss results are used to compare the performance for the two transitions: differential and microstrip. Figure 15 shows the comparison of the insertion loss for the microstrip and differential pair for a 4 mil gap and two pedestal heights. As expected the differential pair exhibits superior performance across the entire band. The differential pair also shows little dependence on the proximity of the ground plane return path. However, the dependence of the performance of the microstrip shows a strong dependence of proximity of the wire bond to the ground plane. This is as expected.

Figure 16 shows the comparison of the insertion loss for two pedestal heights of 0 mil and 20 mils. However in this case the transition gap is 50 mils. As expected the insertion loss increases significantly for both cases, but as can be seen the dependence on the ground plane remains weak for the differential pair case. For the microstrip case the influence of the pedestal height is significant. These results are as expected and merely illustrate how, in a systematic fashion, the speed of a package can be obtained by trading off wire bond

length, transmission line type, and pedestal height. As one introduces manufacturing tolerances, a matrix of such results can quickly provide a down select process for wire bond length and return path configuration.

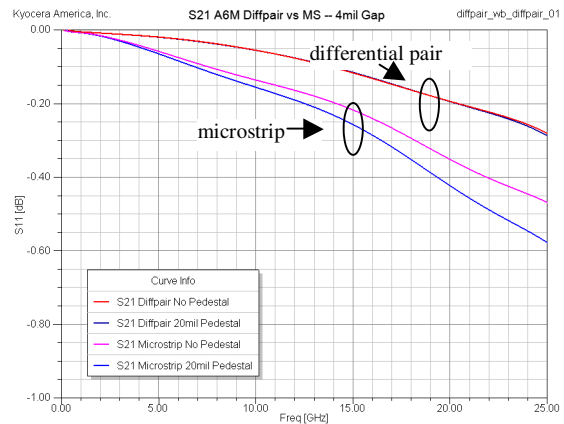


Figure 15 Insertion Loss for microstrip and differential pair transition on A6M.

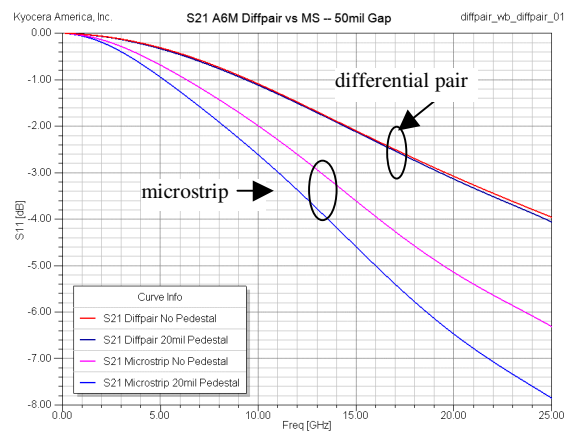


Figure 16 Return Loss for microstrip and differential pair in A6M

1 vs. 2 vs. 3 wire bonds

As a final section we consider an oft-posed question regarding the using multiple wire bonds to improve broad band performance of a transition. As a general principle this is correct, however, with full-wave solvers it becomes feasible to determine how many wire bonds are really necessary.

Figure 17 shows 5 possible wire bond configurations spanning a 75 mil gap between two 25 mil wide microstrip lines: a single wire bond, a double wire bond at a tight pitch, three wire bonds at a tight pitch, two wire bonds as far apart on the trace as possible, and finally, three evenly spaced wire bonds. Clearly the addition of each additional wire bond should improve the insertion loss, since we are reducing the effective inductance (lowering the impedance of the discontinuity) of the wire bond transition. However, direct simulation provides valuable comparisons and potential means to reducing the number of wire bonds

by judicious placement of the minimum number of wire bonds for a given performance specification. Simulations for all 5 possible wire bond configurations are shown in Figure 18. It is clear that two widely spaced wire bonds can provide the same insertion loss performance as three tightly pitched wire bonds. The result might be expected as we reduce the mutual coupling between the two wire bonds by placing them far apart, but the key point is that full-wave simulation can not only provide the analysis of each and every structure, but can also be used to systematically generate guidelines for wire bond transitions to be used to trade off against other packaging considerations.

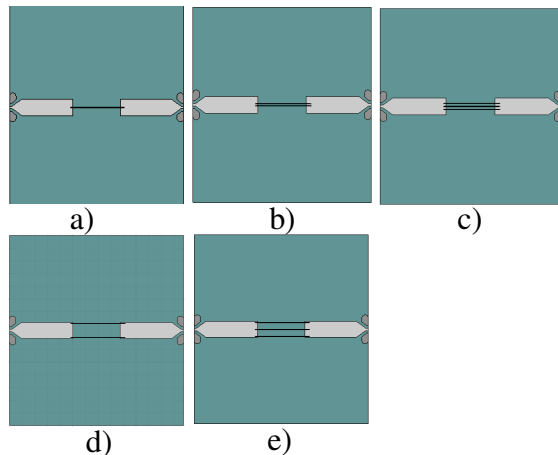


Figure 17 A 75 mil gap between microstrip lines: a) 1 wire bond, b) 2 wire bonds, c) three wire bonds, d) 2 widely spaced wire bonds, e) 3 evenly spaced wire bonds

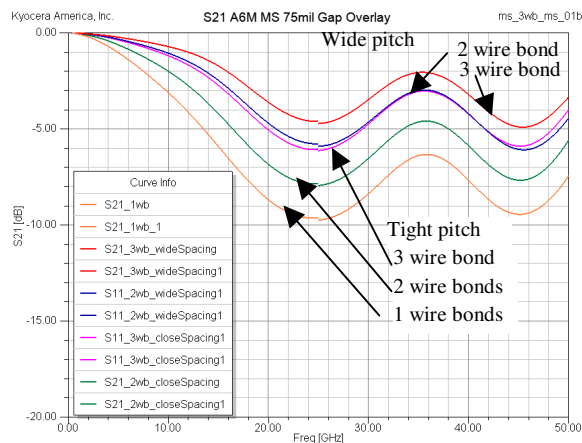


Figure 18 Insertion Loss for wirebonded microstrip line on A6M with 75 mil gap

Summary and Conclusions

This paper presents the correlation of measurement and simulation for wire bond transitions ranging from 4 mils to 100 mils. Excellent agreement is found for the longer wire bonds. For the short gap transitions, we find that the wire bond shape is significantly more sensitive to assumed wire bond shape dimensions. As an extension of the correlation, this paper moves toward

generating general guidelines for the performance of typical wire bond transitions as might be found in a typical package first level interconnect.

Microstrip and differential pairs are compared and simulated to establish influence and magnitude of influence on the return path specifics influencing the performance of the first level interconnect. General behavior is as expected: differential pairs have superior performance to single ended microstrip transmission lines and are least sensitive to the external return path configuration given the virtual ground plane between the signal pair. A key factor in consideration of wire bond length is that it is not length alone that determines speed of the package, but the return path as well, especially in single-ended transmission lines. For differential pairs, the wire bond length can be considered the dominant determining factor for speed of a package.

Future work allows for extending the well understood use of full-wave tool nuances with accurate wire bond shapes to establish rules of thumb, and/or decision curves to guide the required first interconnect transition criteria for a particular high speed application.

References:

- [1] M. Megahed, P. Zilaro, M. Khaw, "Design and analysis of low cost IC package solution for 10-gbit/s applications, IEEE MTT-S Int. Microw. Symp. Dig., pp. 1899-1902, 2001.
- [2] D. G. Kam, J. Kim, "40-Gb/s Package Design Using Wire-Bonded Plastic Ball Grid Array," IEEE Transactions on Advanced Packaging, Vol. 31, No. 2, pp. 258-266, May 2008.
- [3] J.-Y. Chyan and J. Andrew Yeh, "Return Loss Reduction of Molded Bonding Wires by Comb Capacitors," IEEE Transactions on Advanced Packaging, Vol. 29, No. 1, pp. 98-101, February 2006.
- [4] J. Lim, D. Kwon, J. Rieh, S. Kim, and S. Hwang, "RF Characterization and Modeling of Various Wire Bond Transitions," IEEE Transactions On Advanced Packaging, Vol. 28, No. 4, pp. 772-778, November 2005.
- [5] X. Qi, C. P. Yue, T. Arnborg, H. T. Soh, H. Sakai, Z. Yu, R. W. Dutton, "A Fast 3-D Modeling Approach to Electrical Parameters Extraction of Bonding Wires for RF Circuits," IEEE Transactions on Advanced Packaging, Vol. 23, No. 3, pp. 480-488, August 2000.
- [6] A. Sutono, N. G. Cafaro, J. Laskar, and M. M. Tentzeris, "Experimental Modeling, Repeatability Investigation and Optimization of Microwave Bond Wire Interconnects," IEEE Transactions On Advanced Packaging, Vol. 24, No. 4, pp. 595-603, November 2001.