Near Chip Scale Package for High Power, Big Chip LEDs

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Abstract

High power LEDs are rapidly evolving into devices that progressively bear less and less resemblance to the LEDs that we used to know. Today's LEDs feature higher brightness levels, higher operating power levels, larger die/emitter sizes, a shift from edge emission to surface emission, enhanced extraction and collimation of light, and increased efficacies. These changes are enabling applications that until now have been dominated by mercury-arc, high intensity discharge, halogen, incandescent and fluorescent bulbs, and previously were beyond the capability of LEDs. Now that LEDs can compete in many high brightness applications previously occupied by more traditional forms of lighting, new innovative forms of LED packaging are required. Handling high-density thermal dissipation, high optical power levels, tight mechanical tolerances and high current electrical interconnects now require packaging approaches that were previously unconventional, even unheard of, for LEDs. In order to address these new LED package requirements, a near-chip-scale package has been developed which is a drastic departure from traditional LED packages. This new packaging platform has borrowed from, and built on, a mix of packaging technologies more commonly associated with laminate array style BGA, CSP, and flip-chip devices. This paper presents the challenges encountered, and solutions implemented during design of the package and the associated process development. The package structural, thermal, optical and electrical design inputs are presented as well as the subsequent design approaches, including materials selection, risk prioritization, and designing for manufacturability and reliability. The resultant package is a revolutionary, very compact, surface mount device which features a junction-to-case thermal resistance of <0.6 degrees C/W for a 12 mm^2 LED die, zero optical loss (100% transmission), close proximity optical interfacing due to elimination of wirebonds and their associated loop heights, excellent compatibility with state-of-the-art assembly manufacturing lines, and design flexibility including potential for MCM and SiP integration.

Key words: LED, CSP, SMD, BGA, flip-chip

I. INTRODUCTION

Large area LED chips have now begun replacing mercury arc lamps in applications such as fiber coupling systems used in endoscopes/microscopes, and in DMD projection systems ranging from large home theater systems to very compact, high brightness pocket projectors. As these systems continue to evolve, key package attributes have been identified as critical to even further improve the performance of the LED. For these types of etendue sensitive applications, it is advantageous to use an LED which offers surface emission from a large, uniform and uninterrupted light emitting area. PhlatLight LEDs with this structure enable efficient coupling of as much as 3000 plus green lumens of light from a single 12mm^2 chip into the collection optics. The LED package is a critical means of interfacing such an LED to the system; optically, electrically, thermally, and mechanically. However, while the package enables this needed connectivity, at the same time it also impedes such connectivity. For example, wirebond loop heights and a protective glass window limit the proximity of the collection optics, the electrical connector has a certain amount of contact resistance, and although high thermal performance packaging exists in the industry, the package nevertheless has an

associated thermal resistance and this is a continuous area of focus for improvement. Furthermore, all of these attributes contribute to package size. In response to these points, a new wirebondless, windowless package has been developed, allowing the collection optics to be brought to as close as 50um from the die surface. In addition to optical performance, high power dissipation of up to 1KW/cm^2, high current, low resistance electrical interconnects, and form factor reduction have all been addressed and improved over previously available LED packages.

II. DESIGN INPUTS

A list of key package characteristics was compiled and targets were set for desired performance enhancements. These performance attributes were then specified according to thermal performance, optical performance, mechanical features/form-factor, electrical interconnect, and cost, while maintaining reliability and flexibility with respect to both design and manufacturing.

A. Thermal Performance Requirements

The electrical drive conditions required to deliver thousands of lumens per chip result in a high heat flux density which needs to be properly managed. Power densities for PhlatLight devices typically range from 200W/cm^2 to 800W/cm^2, and in some applications can be driven to approximately 1KW/cm^2. These power density levels are higher than most microprocessors, and are not just limited to hot-spots as in microprocessors, but in PhlatLight chips the power density is continuous over the entire surface area of the chip (typically ranging from 4mm^2 up to 12mm^2 or even higher, for a single chip).

In order to achieve higher brightness at a given maximum junction temperature (Tj), the thermal resistance of the packaged device needs to be lowered. A target was set for 20% reduction in thermal resistance from junction to heat sink - Rth(j-hs) - compared to the existing chip-on-board package.

B. Optical Performance Requirements

Two areas affecting optical loss were identified as opportunities to focus on; transmission losses in the protective glass window, and collection losses from stray photons escaping at high angles.

At high optical power levels, absorption and reflection of the glass window can produce losses. The glass window can be exposed to more than 10W of radiometric flux, which is reflected back, absorbed in, or transmitted through.

A very close proximity optics interface is also desired to optimize collection of all photons. The larger the distance from emitter to collection optics, the more light will be lost. Even though PhlatLight devices can feature collimated emission rather than lambertian, there are still a small percentage of photons that emit non-perpendicular to the surface, as shown in figure 1.

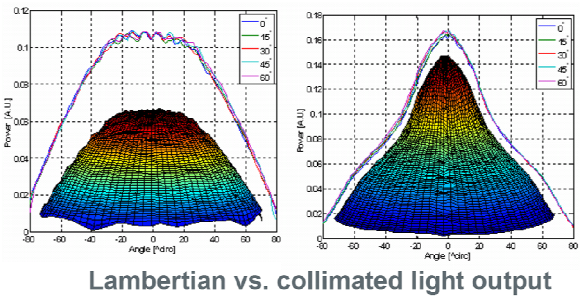


Fig. 1: Lambertian vs. collimated light

At thousands of lumens per chip, even just a few percent stray photons can add up to hundreds of lumens. For optical performance improvement goals were set to reduce or eliminate transmission losses in the glass, and to enable closer proximity optics.

C. Mechanical/Form-factor Requirements

There are several points to address with respect to form factor. To enable densification of systems, it is desirable in general to reduce the form factor as much as possible. But additionally, form factor is specifically related to, and driven by, optical interconnect requirements and electrical interconnect requirements.

In order to achieve better optical interconnect, the emitting surface of the die needs to be made more accessible to the collection optics; redesigning the mechanical structure, or form factor, will be looked at for providing better access to the emitting surface.

D. Electrical Interconnect Requirements

Large single chip LEDs for high brightness applications can be pulsed at current densities up to 2.5A/mm^2. This equates to 30A for a 12mm^2 LED. In order to reduce contact resistance of connectors, large contact areas are required for friction contacts. Connectorization has been specified as an area to work on for reduced contact resistance, reduced form factor, and ease of connectivity.

E. Cost, Flexibility, and Reliability Requirements

Cost and reliability are given requirements in any design. Flexibility for design variants and manufacturing change-overs is a sub-set of cost. As we work through the design, these items will be considered at each step. Cost and flexibility will be intrinsically addressed through DFM, and reliability will be predicted theoretically, then verified empirically.

III. PACKAGE STRUCTURE

In order to address new packaging requirements for collimated surface emitting large chips, options outside of traditional paradigms for LED packaging were considered; an open-minded approach was taken considering each spec requirement, individually and combined together, allowing for the best available packaging solutions to realize the specified targets. Also, knowing that the package adds parasitic effects and resistances, we took the approach of trying to minimize the parasitic impediments associated with each packaging element, ideally eliminating it altogether if possible. In some cases, such as with wirebond loops and window transmission losses, we were able to eliminate the package parasitics completely for those constituents.

The resultant package that was designed to meet the above mentioned requirements is a flip-chip on laminate, surface mount device of compact size, with direct solderability of exposed die backside for optimal thermal conductivity, and unimpeded light emission from the die surface for minimal loss optical coupling to the system. Figures 2a and 2b illustrate the package structure and its key features.

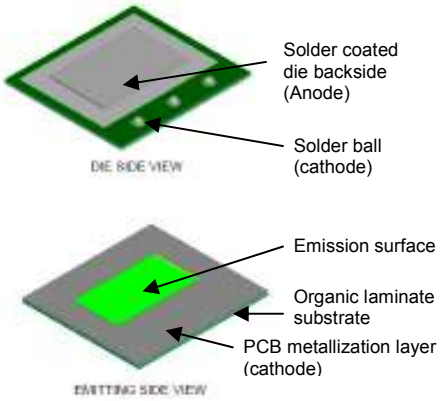


Fig. 2a: Package features

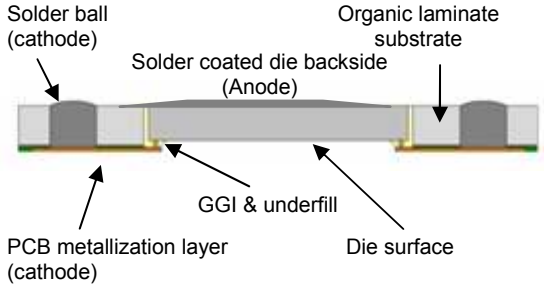


Fig. 2b: Package cross-section

Table 1 below summarizes the features and benefits of this new, near chip-scale-package structure for LED package.

Table 1: Features and Benefits

Wirebond-less	Less handling damage Close proximity
Window-less	No absorption, more light output
SMT mountable	Enable broader market
Pre-coated solder	Less voids, thermal benefit
Thin	Small form factor applications

IV. DESIGN APPROACH AND PERFORMANCE VERIFICATION

A. Thermal Design

In order to dissipate up to 100W/chip, and maintain a junction temperature below 120 degrees C at 30 degrees C ambient, a thermal resistance of 0.9 degrees C/W is required from junction to ambient.

$$Rth_{j\text{-}a} = (Tj - Ta)/Pdiss = (120C - 30C)/100W = 0.9C/W$$

This R-theta(j-a) is divided between the package and the heatsink. The value of 0.9 C/W in the above calculation puts a challenging requirement on thermal resistance between junction to heatsink ($Rth_{j\text{-}hs}$). In the current generation chip-on-board package, the $Rth_{j\text{-}hs}$ is around 0.73 C/W. A target was set for 20% reduction in thermal resistance from junction to heat sink which gives 0.73 C/W – 20% = 0.58 C/W. This allows the system level thermal management to be a little easier when determining active cooling method.

The previous generation package uses a custom highly filled Ag epoxy to achieve the 0.73 C/W value. Calculations were run to predict that the new target of 0.56 C/W may be approached by converting to a surface mount package with a solder coated die backside. This is plotted in Fig 3 below. The calculations were based on the formula:

$$Rth = L / (K \times A)$$

where:

L = thickness of TIM1 in meters
K = effective thermal conductivity in W/mk
A = area of TIM1 in square meters

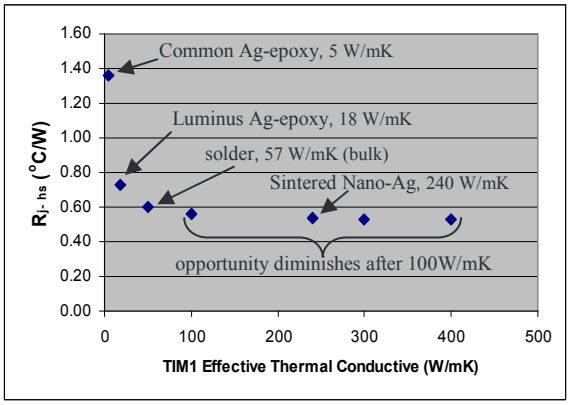


Fig. 3: Predicted thermal resistance improvement opportunity calculated for various TIM1 on 12mm^2 die

B. Optical Design

The two primary sources of optical loss - transmission losses in the glass window and stray photons not collected by the system optics - are addressed by the new package design. Eliminating the window solves both of these problems by completely eliminating transmission losses, and by allowing closer proximity optics interfacing. Since the main function of the window is to protect the wirebonds, the use of flip chip eliminates the need for a window. As seen in figure 4, by using flip-chip, we improve the proximity of the collection optics in two ways: first by eliminating the thickness of the window - typically 300um, and secondly by eliminating the loop height - typically 150um.

Fig. 4: Optics proximity comparison

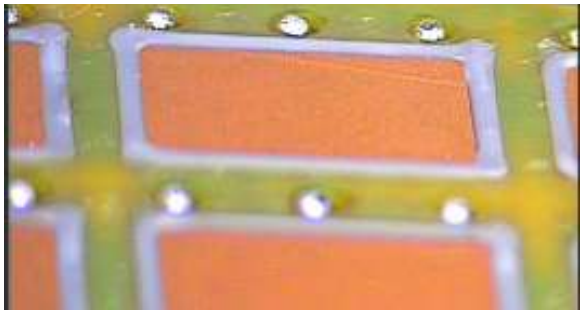
In addition to etendue-sensitive applications, this CSP can also be encapsulated or integrated with a primary optic.

C. Mechanical and Electrical Interconnect Design

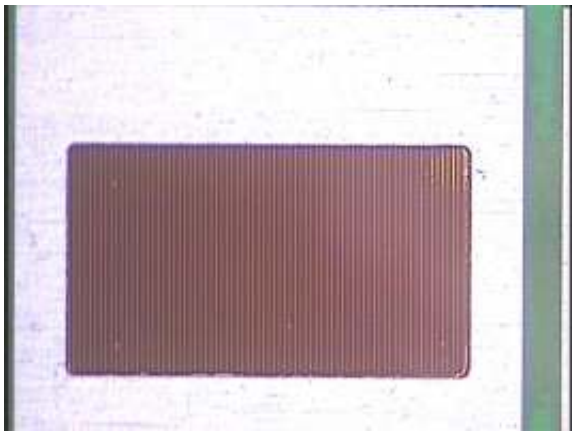
As illustrated in Figure 2, the mechanical structure begins with a metal core PCB with cut-out window. The LED die can be flip chip bumped either by solder paste or Au stud formation. The LED is then flip chip bonded to the metal core PCB frame by solder reflow or gold-to-gold interconnection (GGI) bonding. The precisely designed window allows LED surface to be exposed for complete light transmission. The metal core PCB acts as an interposer which routes the cathode of LED to the solder ball arrays. The backside of the LED is finally metalized and coated with solder for anode solder connection. The resultant package structure is a surface mountable device that provides outstanding thermal and electrical interconnection to the next level board.

D. Process and Material Development

Significant effort has been spent on the material selections and process development in order to make this a manufacturable and reliable package platform. On the material side, selection of PCB materials, their metallization, solder mask were well considered together with our vendor. Different solder materials either as the paste or BGA ball are also tested for their reflow performance and temperature hierarchy requirement. In order to prevent the solder flux from migrating from the bottom side to the surface of LED during SMT reflow, sealing the flip chip bonding gap along four sides of the frame is required. Epoxy underfill and silicone sealant material were evaluated. Figure 5 shows an example of the assembled LED package in a panel form prior to singulation. The three solder balls are cathode connection while the metalized LED backside is the anode pad. In the finished package, solder is deposited on the backside for enhanced solderability and coplanarity. The underfill/sealing material around the backside of LED is the white silicone.



(a)



(b)

Fig. 5: Near chip scale LED package in a panel form prior to singulation. (a) the backside of the LED with interconnection contacts for SMT soldering; (b) the front side of the LED.

On the process side, the development focus was primarily on the GGI bonding quality and the underfill flow control. Au stud bumping is adopted due to its' simplicity compared to solder bumping and no need for changing the under-bump metallization (UBM) structure on the chip. 10 bumps are formed using 1 mil Au wire on each side of the 12mm^2 die. The GGI bonding is then optimized through multiple runs of design of experiment (DOE) to study the key bonding parameters, PCB flatness, plasma clean of bonding surface, and stress induced during cooling from process temperature. In developing the underfill process, material viscosity, its thixotropic behavior and wetting control, and resin bleed to the die surface during curing are among the major considerations.

VI. SMT ASSEMBLY AND TEST RESULTS

After design, material, and process have been tweaked and optimized, a few hundreds of package samples were fabricated and tested. In addition to large die of 12 mm2, smaller die size were also designed and built to evaluate the feasibility for a range of LED family. Figure 6 shows the 3.9mm2 LED in this type of package style.

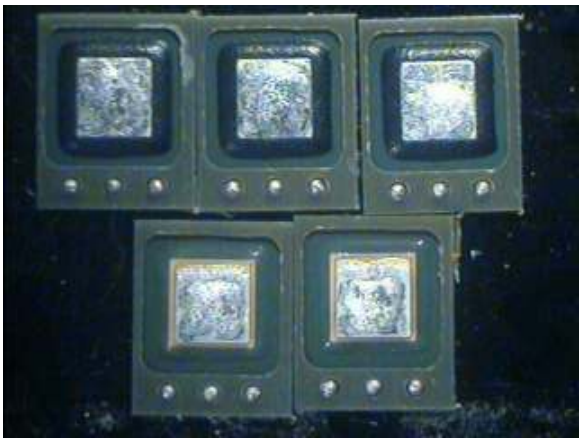


Fig. 6: Examples of singulated 3.9mm2 LED flip chip package (backside view).

The samples were tested in comparison to existing standard package and showed similar optical and electrical performance such as lumen output under the same testing conditions. Although a lumen increase was expected without the glass window, in this case these devices had frame openings slightly smaller than the die emitting area, thus blocking some light. For thermal performance and reliability tests, these parts were bonded to copper based testing substrates employing standard SMT process. Two types of testing substrate were evaluated. One is the copper core PCB with dielectric layers to isolate the cathode and anode. The other is a copper board without any dielectric layer in the heat path. Lead free solder (SAC 305) paste was used. Both convection reflow oven and conduction vacuum reflow oven were evaluated for the assembly quality. It is found that vacuum oven produces less than 5% voids while standard convection oven can result in up to 40% voids.

An empirical study was conducted to correlate solder void percentage versus thermal resistance. The results are shown in Figure 7. It is shown that the 0.58 C/W corresponds with ~25% voiding, which is considered a manufacturable process. As a result of this new lower thermal resistance, the device can now be driven at higher power, resulting in higher lumen output, or using low cost cooling solutions at system level. For applications where thermal resistance needs to be minimized, a vacuum reflow can used to achieve the best solder joint.

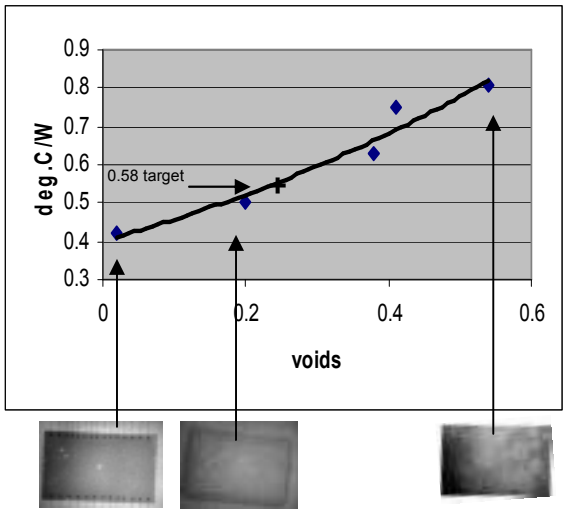


Fig. 7: Effect of solder void percentage on thermal performance

To evaluate the package robustness and screen out defective die, a rapid stress test was performed with the following conditions: 30A at 25% duty cycle or 18A at 100% duty cycle for the 12mm2 die package. All devices passed this screen test. Additionally, a uniformity test under 18A was tested to check the flip chip joint (GGI bonds) quality. Examples are shown in Figure 8.

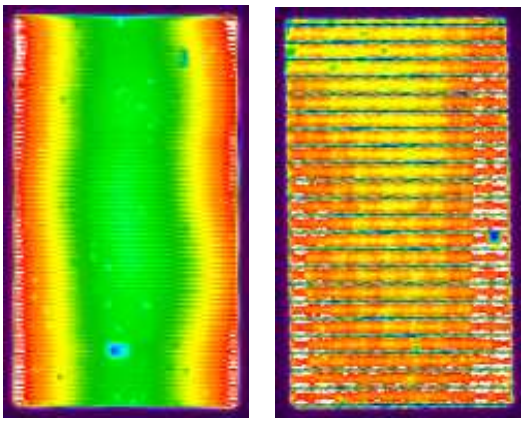


Fig. 8: Image of 12 mm2 red die (left) and blue die (right) under uniformity test at 18A of input current.

Initial reliability tests were performed on both large and small LED packages. These include thermal cycling (-40 to +125C), high temperature operating life (2A/mm2 current density, Tj of 100-150C), as well as high temperature storage (150C) and relative humidity test (85C/85%). Except for some early infant failures, the majority of the samples have passed the reliability test over 1000 hours and 300 cycles. The premature failures can be reduced and/or eliminated through packaging process optimization, quality control and rapid stress screening.

Finally, the moisture sensitivity rating of this new type of SMD LED package was tested per IPC/JEDEC J-STD-020D. It was found the package is capable to meet MSL class 1 at lead free reflow conditions.

VII. CONCLUSION

A near chip scale package has been developed according to predefined performance targets, and has been successfully demonstrated. This innovative design approach is an extension of mature IC packaging technologies to a large area monolithic LED chip package by combining flip chip technology, bump underfill, and interposer with BGA solder array interconnection. The paper described the design structure, associated processes, and demonstrated the manufacturing feasibility of such package. LED package performance and reliability have been shown to meet the design target. Continuing work will focus on the design refinement and process control to improve the manufacturing yield and package robustness.

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