

Mechanically Punched Micro Via Fabrication Process in LCP Substrate for RF-MEMS and Related Electronic Packaging Applications

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Abstract:

The objective of this paper is to present the understanding of micro via fabrication process using mechanical punching on liquid crystal polymer (LCP) substrate. LCP is attracting significant interest in electronic packaging for radio frequency (RF) and microwave applications for its multifarious advantages over the contemporary substrates used in commercial production. Various surface and subsurface features such as micro vias and cavities, at low cost are critical for the fabrication of RF-MEMS packaging. Therefore, there is a need for understanding micro features, such as via fabrication using different processing techniques. Micro mechanical punching is one of such via fabrication techniques. Depending upon the package, the size of via could range from few microns to hundreds of microns. This research has successfully demonstrated the micro mechanical punching process for fabrication of through vias of different sizes and pitch on LCP substrate along with the detailed investigation of the relationship between material structure and properties affected by the different process parameters during the via fabrication steps.

Key Words: Liquid Crystal Polymer (LCP), Electronic Substrate, Micro Mechanical Punching, RF-MEMS Packaging, Via Areal Density, Via Pitch Distribution, Z-axis Expansion of LCP

I. Introduction:

Electronic packaging weighs significant amount of challenge in research, development and commercialization of any electronic system [1]. The packaging has to provide four distinct functions: (1) providing power between chip and outer circuitry, (2) protection from outside environment and mechanical support for the die and chip carrier package, (3) facilitation of signal input/output via interconnects and (4) transporting heat generated inside the chip [2]. Packaging as a platform of structural and environmental integrity it enhances the reliability of MEMS devices in systems [3]. In 3-D flex module packaging used for foldable electronics, the reliability is a dependent on the stress concentration at different heterojunction of the packaging materials [4]. In addition to material selection, special care has to be taken for packaging of MEMS device intended to be used in harsh environment, such as oceanic environment. In this regard, glob top encapsulation is usually done on the die to put an extra environmental protection and physical stiffness of the die [5-6]. For high power electronic module packaging especially for aerospace application particular care has to be

taken to take away the excessive heat generated by the power device. Therefore, integration of thermal vias and micro heat channels into the packaging is crucial [7]. In addition of performing the heat transport micro via fabrication at wafer level and chip scale packaging has been reported for necessary electrical interconnection [8-9]. One concern about the MEMS die packaging is hermetic sealing [10]. Laser assisted bonding (LAB) has demonstrated a promising result backed by the theoretical calculation for the leak detection [11-12]. Leak detection is very crucial for traditional functionality of electronic packaging.

Apart from the traditional functionality of electronic packaging, MEMS packaging has to house the moving parts of the MEMS device, such as the cantilever or bridge structure for MEMS capacitive switch. The housing for moving parts can only be possible by fabricating a cap layer with cavities in it. MEMS devices like simple capacitive switches have 4 input/outputs (I/O's) to facilitate RF signal input, RF signal output, DC supply and grounding. However, use of capacitive switches for tunable capacitor or filter can consist of few to hundreds of

identical switches, which eventually needs different array of I/O logic combinations. These logic arrangements can only be made possible by using a network consisting of interconnections and distribution traces. Hence there is a need to study via fabrication with different array and via pitch distribution along with the choice of material for the substrate. Scale up and cost considerations are critical considerations.

Liquid crystal polymer (LCP) is a promising thermoplastic organic material [13], which has emerged as a possible candidate for its possible integration into the RF systems packaging for its lower dielectric constant of 2.9 at 10 GHz and room temperature [14]. Lower dielectric constant contributes lower loss through the medium which is very much essential for system operating at GHz range frequency. This cost effective polymeric material along with its low temperature processing (335°C) to fabricate laminated multilayered structure makes it the best suitable candidate for RF application. In addition, high temperature processing of the packaging material has an adverse effect on degradation of device properties. Moreover, the loss tangent in LCP is as low as it is in LTCC (0.002 at 10 GHz at room temperature). The minimal increase in loss tangent (from 0.002 to 0.0045 at 110 GHz) in response to the exponential increase in operating frequency makes LCP a suitable candidate for millimeter wave application [13]. Apart from the material itself, the cavity inside the LCP multilayered cap layer has to be hermitically sealed as possible penetration of moisture can cause stiction and corrosion problem of the moving parts in MEMS device. This new polymer material has very low moisture absorption of 0.04% at room temperature and 100% relative humidity for 24 hours as compared to the 2.8% in Kapton [15]. These multifarious advantages of the LCP as a substrate material makes it very suitable candidate for its integration as a new packaging material in RF MEMS application. It is important to understand and develop via and other processing abilities for LCP. A detailed discussion on via fabrication technique is presented in the following section.

II. Test Vehicle Specifications:

The intended goal of this research work was to examine the feasibility to fabricate micro vias by using traditional platform of mechanical punching on a novel LCP substrate to meet the needs of RF-MEMS device packaging. State-of-the-art RF-MEMS product has a requirement of via diameter of $90\text{ }\mu\text{m}$ with a minimum pitch of $300\text{ }\mu\text{m}$ in X-direction and

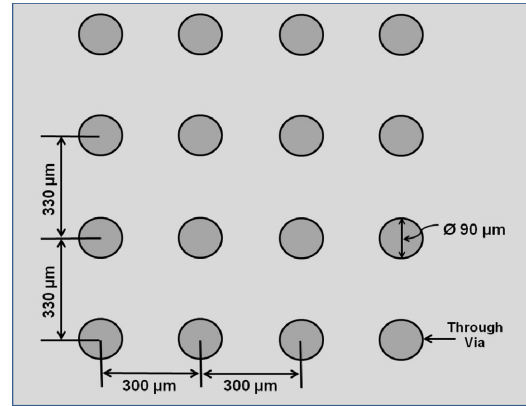


Figure – 1: Specifications of the test structure

$330\text{ }\mu\text{m}$ in Y-direction. Figure – 1 illustrates the details of the example test structure. The experiments designed in this research were focused to achieve this goal through fundamental understanding of the viability of mechanical punching process. In the experimental matrix the aggressive specifications were targeted. For example, experiments were aimed for via diameter of $50\text{ }\mu\text{m}$, half in the value of the present test structure. Also tested pitch of the via was as low as one fourth of the test structure specifications.

III. Fabrication of Micro Via on LCP Substrate by Mechanical Punching:

As discussed earlier, LCP as a material has the best merits for its better electrical performance compared to other contemporary substrate material. In this regard, the Rogers Corporation LCP brand named ULTRALAM 3850TM has very tightly stable electrical properties for highly controlled impedance matching. The surface resistivity of $1 \times 10^{10}\text{ Mohm}$, volume resistivity of $1 \times 10^{12}\text{ Mohm/cm}$, dielectric breakdown voltage of 3500V/mil allows the circuit designer to use ULTRALAM with more flexibility of using a thinner dielectric layer with possible breakdown of the dielectric layer even at higher operating voltage. In addition, the lower dielectric constant of 2.9 will give less or minimal signal distortion when the device is operational at GHz range of frequency. The ULTRALAM 3850TM is available in $25\text{ }\mu\text{m}$, $50\text{ }\mu\text{m}$, and $100\text{ }\mu\text{m}$ thickness with $\frac{1}{4}\text{ oz.}$ ($10\text{ }\mu\text{m}$) and $\frac{1}{2}\text{ oz.}$ ($20\text{ }\mu\text{m}$) copper cladded on both sides. A multilayered LCP cap is required for the RF-MEMS application where as many as 13 layers can be laminated together with the redistribution traces to fabricate the cap. $100\text{ }\mu\text{m}$ thick individual LCP film will end up a total thickness of 1.3 mm which will push the limit of the

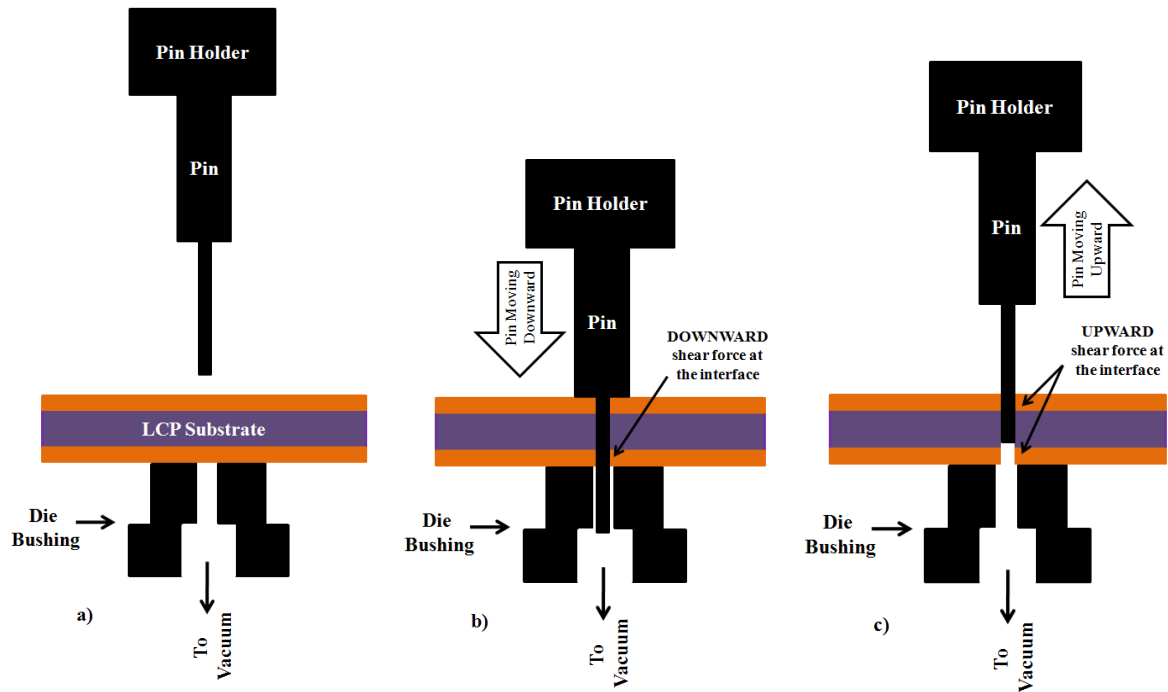


Figure – 2: a) LCP substrate placed on top of the die bushing, b) punch pin moving downwards, c) punch pin moving upwards

real state density of the packaged chip. Therefore, a thinner dielectric is required. Since LCP has a very low dielectric constant it gives the best advantage to choose a thinner film of 25 μm . However, to have more mechanical robustness of the LCP substrate during fabrication process 50 μm LCP with $\frac{1}{2}$ oz. (20 μm) copper cladding has been chosen in this experiment.

Pacific Trinetrics Corporation, CA, USA (model APS-8718) mechanical punching system was used to fabricate the micro vias. During the mechanical punching process as illustrated in figure – 2, the pin impinges the substrate and pierces through it. In the micro via fabrication process using mechanical punching, the substrate is placed on top of a die bushing which has a bigger diameter than the punch pin. As a result of smaller size die bushing as compared to the punch pin for instance, 2.5 mil (62.5 μm) die instead of 3.5 mil (87.5 μm) for 2 mil (50 μm) punching it tends to break the pin very easily. This is because of its increased chance of hitting the die edge rather than the exact center. In addition, use of smaller die, tends to leave the slug into the die, which tends to clog into the die. Clogging of the die makes it impossible to reuse it even after cleaning. Use of bigger size die eliminates the chance of clogging and makes the die reusable. Therefore, a 3.5 mil (87.5 μm) die is used for a 2 mil (50 μm) pin, 4.5 mil (112.5 μm) die is used for 3 mil

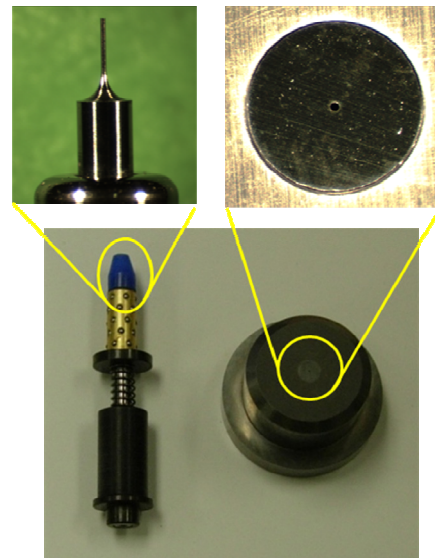


Figure – 3: top) the tungsten carbide punch pin and the die; bottom) the punch pin holder and die bushing

(75 μm) pin, and 5.5 mil (137.5 μm) die is used for 4 mil (100 μm) pin. The die was connected to a vacuum system from the bottom which sucked the clogged material ejected out from the punching process.

Punch pin and die are made of tungsten carbide supplied by MPK Special Tools GmbH, Germany. The punch pin along with the holder and die bushing are shown in figure – 3. Special tool set was used to mount the punch pin in the pin holder and the die into the bushing. Since LCP is a flexible substrate, it was expected to deliver some offset apart from the machine offset during the punching process.

IV. Cross Sectional Analysis of the Micro Mechanically Punched Via:

The Cross section of the ULTRALAM LCP film was obtained (as shown in figure - 4) by molding the punched sample into pot molding compound from Buhler. The mold was made using Epocolor™ fast cure resin and hardener mixed into a ratio of 5:1. The sample was cured over night at room temperature. Though the curing could be done at 150°C or higher temperature, the elevated temperature might alter the sample property. Hence room temperature curing was chosen in all the experiments conducted under the research. In the figure, D_1 represents thickness of the LCP film sandwiched between top copper film (of thickness D_2) and bottom copper film (of thickness D_3). During the punching process, if the LCP film is punched without a suitable supportive polymeric base, the bottom part of via was unevenly sheared. In addition, there is an inevitable chance of micro and sub-micro crack formation at the edge of the bottom copper film. Hence an additional PTFE film is used at the bottom of the LCP film. The PTFE film will give an additional mechanical support to the LCP film as well. The soft polymeric film in between two metallic contacts (between bottom copper layer and die) minimizes the energy deposition and shear force which the sample experiences. Therefore, the possible chance of crack propagation through the copper film is minimized.

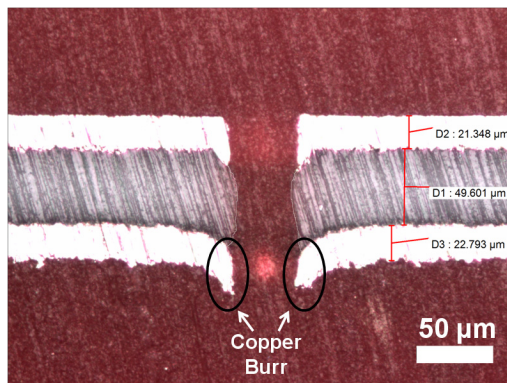


Figure – 4: Cross sectional view of the fabricated via on ULTRALAM LCP film

Copper burr formation in figure – 4 at the bottom side of the LCP sample is due to the size variation between the punch pin and die bushing. The burr is formed in downward direction because of the shear force acting from the punch pin on the LCP substrate when it is applied in downward direction during the micro mechanical punching. After punching, the pin is retracted and translated to the next punch location. This upward pull action of the pin creates an upward shear force on the entire substrate during upward sliding of the pin with intimate contact with via wall, which in turn causes an mechanical distortion (expansion) of the LCP film in Z-direction. Study of this Z- axis expansion is presented in the following section.

V. Experimental Results:

A. Pitch dependency of the film Z – Axis expansion:

In any electronic packaging pitch of the vias varies according to the requirements of the design and signal integrity of the circuit. Therefore, study of pitch dependency during via fabrication on LCP substrate was undertaken. An experimental matrix was designed to study the impact on the Z-axis expansion of the LCP film. 50 μm, 75 μm, and 100 μm vias were fabricated starting from the unit pitch with 25 μm increment. For example, 50 μm vias were fabricated with pitch of 75 μm, 100 μm, 125 μm, and 150 μm. 10x10 arrays of vias were fabricated in the designed test vehicle. The height of the Z-axis of the LCP film was measured at the central part of the via array to study average behavior. For instance - in a 10x10 array the measurement was performed on the 5th or 6th vias of the row.

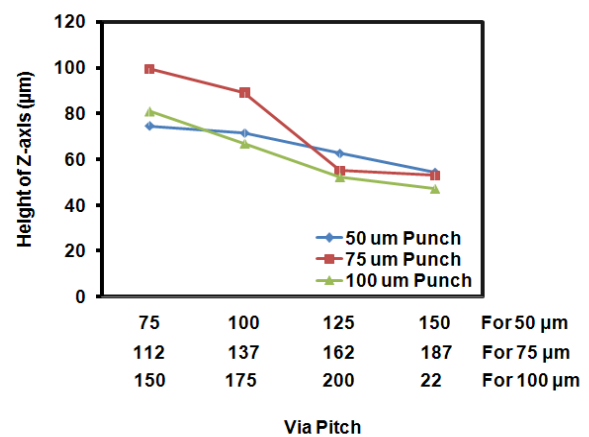


Figure – 5: Z-axis expansion of the LCP film and its dependency on the via pitch

Figure – 5 illustrates that the Z-axis expansion is highest for a pitch with unit distance and the expansion become less noticeable with longer pitch. The Z-axis expansion of the film is almost nil when there is a 100 μm increase in addition to the unit pitch, i.e., at 150 μm pitch for 50 μm punch, 187 μm pitch for 75 μm punch, and 225 μm pitch for 100 μm punch. This increase in the film expansion with lower pitch can be attributed to the closeness of the vias and the associated additive z-axis expansion of the films created by the first and second vias. It is observed that distance between two vias is inversely proportional to the cumulative Z-axis expansion of the film. This cumulative effect of the first via becomes negligible once the second via is fabricated far enough to have no impact from the first via. In addition to the pitch of the via there is a dependency of the z-axis expansion on the number of via holes in an array which is presented in the following section.

B. Via array dependency of the LCP film Z – Axis expansion:

Apart from pitch of the via, the number of vias (via density) in an array was expected have an effect on Z-axis expansion of the LCP film. 4x4, 6x6, 8x8, and 10x10 array of vias were fabricated using the above process. The fabricated vias were of 50 μm , 75 μm , and 100 μm in diameter with unit pitch. For different via diameters, higher via density was shown increased Z-axis expansion of the LCP film (figure -6). This z-axis expansion also goes with the similar explanation that more the number of via holes in an array the cumulative adding up of the individual Z-axis expansion due to the punch. Therefore, more number of vias in an array, higher the corresponding expansion of the film.

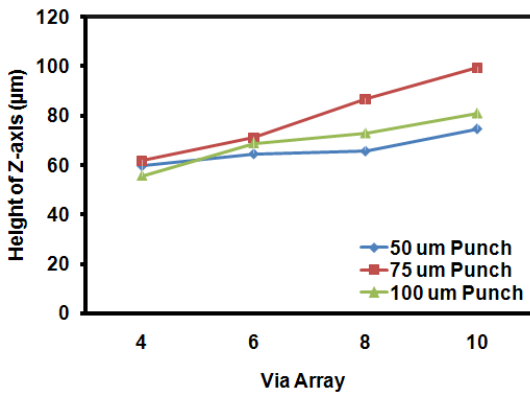


Figure – 6: Z-axis expansion of the LCP film with increase number of holes in an array

C. Radius of Warped LCP Film:

The micro mechanical punching tends to form a tomb shape warpage of the film during the micro via fabrication. This is due to the upward shear force acting on the substrate from the punch pin as shown in figure – 2 previously. It was observed from the cross sectional analysis that the warpage formation is correlated with pitch of the vias and density. Therefore, the radius of curvature of the warpage needs to be measured to find these correlations. The radius of the curvature of the circuit formed by the tomb shape warpage can be calculated by using the formula presented in the equation – 1.

$$r = \frac{d^2 + h^2}{2h}$$

When $h \approx 0$, $(r - h) \approx r$ ----- (1)

Then $\frac{(r - h)}{r} \leq 1$

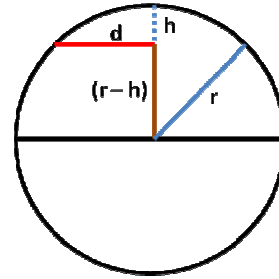


Figure – 7: Measurement of radius of curvature

Figure – 7 depicts the procedure of finding the d and h in the warpage formed in the LCP film. Where, d is the distance between the edge and center of the via array, and h is the distance between the base of the via array and tip of the tomb shape. The

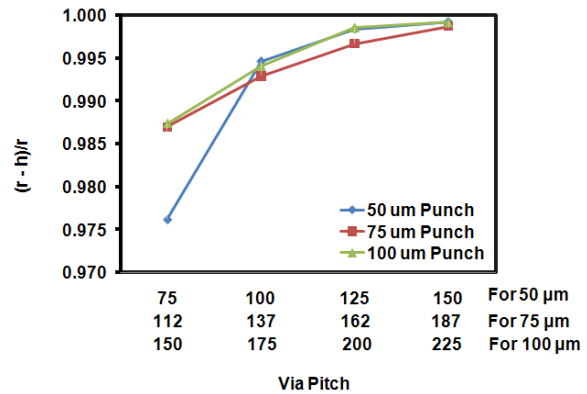


Figure –8: Decrease in radius of curvature with increase in via pitch

measurements were from the optical microscope image and using Buhler OmnimatTM software. From the equation we can see that the value of $(r - h)$ is closer to the radius of curvature if the value of $h \approx 0$. In that case the ratio between the $(r - h)$ and r is closer to 1. The more the value of $\frac{(r - h)}{r}$ closer to 1 there will be less amount of warpage formation. $\frac{(r - h)}{r} = 1$ indicates that there is negligible curvature formation during the micro mechanical punching process.

Furthermore, figure – 8 shows that the value of $\frac{(r - h)}{r}$ is closer to 1 when there is higher value of pitch in the micro via formation which in turn indicates that the value of radius of curvature decreases as via pitch increases. This implies that higher amount of pitch allowed less adding up effect of the upward bending. The closer the vias are the more bending of the film, consequently smaller the warpage diameter. The study was done on the 50 μm , 75 μm , and 100 μm via size with the different pitch starting from the unit pitch to pitch sizes with 4 equal 25 μm increments. Lower number of vias in an array will have less amount of warpage and thus less amount of associated upward bending. Hence, as seen in figure – 9, radius of curvature decreases as the number of vias in an array increases. Less amount of bending is the resultant of less number of repetitive shear forces acting on the film due to lower number of vias in the array.

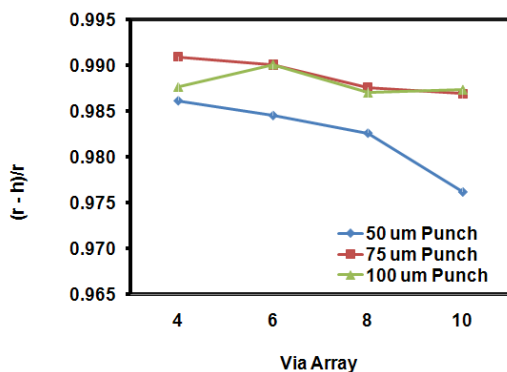


Figure – 9: Radius of curvature decreases as the number of vias increases

This study successfully demonstrates that the desired via specifications (Figure - 1) for RFMEMS application in LCP substrate could be delivered using traditional platform of micro

mechanical punching. The current infrastructure is capable of delivering large scale and cost effective manufacturing with least possibilities of defects. Future research will involve fundamental understanding of cleaning vias and their metallization for intended application.

VI. Conclusion:

In this research work successful micro via fabrication in LCP substrate is presented. Z-axis expansion of the LCP film was found to be inversely proportional to the pitch while it was directly proportional to the number of vias in an array. There was a noticeable warpage for a smaller pitch or for a higher number of vias in an array. This warpage formed a tomb shape when the radius of curvature decreased with higher values of pitch and lower number of vias in an array. We believe, the anisotropic alignment of the polymeric chain gave the LCP film a lower tensile strength in Z – direction, which lead to the expansion of the film in Z – axis during micro mechanical punching.

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