

Modeling and Analysis of a New Packaging Structure for Noise Isolation in Mixed-Signal Systems

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Abstract

The integration of heterogeneous components/sub-systems (e.g., RF, high-speed digital, MEMS...) on the same chip, package or board requires the use of efficient noise isolation/suppression structures or techniques to minimize electromagnetic interference (EMI). So far, electromagnetic band gap (EBG) structures have been considered to be the most effective means to suppress noise coupling and prevent EMI over a wide range of frequencies. However, EBGs reduce the integration density because they consist of many periodically arranged patches, vias, and at times, surface mount components (capacitors and/or inductors) which consume much of the board space. EBGs also cause return-path discontinuity (RPD) problems for signal lines routed above/below one of their patterned layers, thus resulting in signal integrity (SI) issues. Therefore, in this paper, we propose a new packaging structure for noise isolation – the interconnected patch ring (IPR) structure. It is just as effective as EBGs in noise suppression/isolation, but overcomes most of the limitations of EBGs and other conventional noise isolation structures. To illustrate some of its advantages, we modeled and simulated the IPR structure to suppress the propagation of noise from 700 MHz to 2.5 GHz – the frequency range used by many wireless communication standards (e.g., GSM 900/1800, Bluetooth, UMTS and 2.4 GHz WLAN). Test samples of the IPR were designed, fabricated and measured. The measurement results showed good isolation throughout the required frequency range (Proof of Concept). Furthermore, a very good correlation was obtained between measurement and simulation, thus experimentally validating the simulation results.

Keywords: Noise isolation/suppression, decoupling capacitor, split-planes, electromagnetic bandgap (EBG), interconnected patch ring (IPR), signal integrity (SI), electromagnetic interference (EMI).

1. Introduction

To meet the continuous demands for miniaturized electronic components and systems, the integration density is steadily increased. This is mostly achieved using either the System-on-Chip (SoC), System-in-Package (SiP) or System-on-Package (SoP) approach, whereby heterogeneous components/sub-systems (e.g., RF, high-speed digital, MEMS...) are integrated in close proximity to each other on the same chip, package or board. Such high-density mixed-signal integration requires the use of efficient noise isolation/suppression structures or techniques, especially if the different components/sub-systems share the same power distribution network (PDN). This is mainly because at higher operating frequencies (>1 GHz), noise generated by components/sub-systems on one part of the chip/package/board may couple to other parts, causing electromagnetic interference (EMI). This may then lead to detuning of sensitive

RF/analogue circuits, false switching of digital circuits or even system failure.

In this contribution, a novel planar noise isolation/suppression structure, the interconnected patch ring (IPR) structure, is proposed, modeled and analyzed. To experimentally validate the IPR concept as well as the simulation results, test samples were designed, fabricated and measured. The measurement results show good isolation throughout the required frequency range. Furthermore, a very good correlation was obtained between the measurement and simulation results.

The rest of this paper is structured as follows: An overview of the state-of-the-art structures/techniques used to prevent/minimize the generation and propagation of noise in electronic packages and boards is first presented in section two. This is followed in section three by a brief illustration of some of the limitations of these conventional

techniques using the EBG as an example. In section four, modeling and analysis of the novel noise isolation structure, the IPR, is presented. Furthermore, the advantages of the IPR over conventional noise isolation techniques as well as the proof of concept are also presented in this section.

2. State-of-the-Art Structures/Techniques: An Overview

Over the decades, a variety of structures/techniques have been developed and applied to prevent/minimize the generation and propagation of noise in electronic circuits at the chip, package and board levels. Three approaches that have received much attention within recent years are decoupling capacitors, split planes and electromagnetic band gap (EBG) structures.

The main goal of decoupling capacitors, as used for example in [1]-[3], is to prevent/minimize the generation of switching noise, i.e., simultaneous switching noise (SSN). By delivering charges to switching ICs, they minimize the voltage drop across the PDN which normally results in the generation of SSN, and its coupling in power-ground cavities. However, due to the parasitic inductance of the capacitors as well as the inductance of the interconnects used to mount the capacitors, they are usually effective only up to about 1-2 GHz.

The concept of split-planes, as used for example in [4], is based on the fact that the impedance of slots/slits is very high at lower frequencies, therefore noise cannot propagate between sub-systems/components mounted on the same board and separated by a slot/slit. However, as shown in [5], this method becomes ineffective at higher frequencies (>1.5 GHz) because the impedance of the slit/slot becomes very small. Furthermore, the split-planes approach is not cost-effective, because multiple power supplies may be needed to maintain the same DC level at different parts of the board, if required.

To overcome the limitations above, EBGs, based on Svienpipper's work on high impedance surfaces [6], have been applied. Due to their efficiency in suppressing the propagation of noise within a pre-defined range of frequencies, different configurations of EBGs have been developed and extensively studied within the last decade. These configurations can be broadly classified into three main categories namely; mushroom-type, (e.g., [7]-[9]), planar (e.g., [10]-[12]) and hybrid (e.g., [13], [14]) EBGs. Since EBGs are periodic structures, one of the metal (reference) layers is always

periodically segmented. The capacitances and inductances of the periodically arranged patches, the metal strips which interconnect the patches and/or vias (in the case of mushroom-type EBGs) are used to achieve the stopband characteristics within the desired frequency range. In some cases (e.g., in hybrid EBGs), surface-mount capacitors and inductors are also used, in addition to the patches and vias. However, since these surface-mount components as well as the periodic patches, interconnecting metal strips and vias (needed for noise suppression) consume much of the board space, very little space is left for the placement and routing of the "actual" components needed for system functionality. EBGs therefore, reduce the integration density of electronic packages and boards. Furthermore, due to the periodicity of the patches, transmission lines referenced to the patterned layers of EBGs suffer from return-path discontinuity (RPD) problems, which severely degrade their electrical performance.

In the next section, some of the limitations associated with the state-of-the art noise isolation structures/techniques will be briefly illustrated.

3. Illustrating Some of the Limitations of State-of-the-Art Structures/Techniques using a Planar EBG as an Example

Since EBGs are currently considered to be the most effective means to suppress noise coupling, we'll use them as an example in this section. Two of the main limitations addressed are 1) the RPD issue caused by EBGs as a result of the discontinuity of the reference planes and 2) lack of board "space" for placement and routing of system components. In order to illustrate these limitations, a planar EBG for ultra-wideband (UWB), WLAN, Bluetooth and UMTS applications was designed and fabricated on an FR4 substrate ($\epsilon_r=4.2$ and $\tan \delta=0.02$). The EBG consists of 2 metal layers and a dielectric layer (200 μm thick) in-between.

Figure 1 shows its top view. The top metal layer consists of a 3*3 array of patches. The patches are separated by a distance of 0.5mm and are interconnected by a metal strip having a length of 6mm and width of 0.25 mm. The bottom metal layer is continuous.

For the EBG design, Ansoft HFSS (a 3D full-wave EM field solver which employs the finite element method to solve Maxwell's equations in the frequency domain) was used. A continuous power-ground plane pair, having the same dimensions as the planar EBG (dielectric thickness = 0.2mm, width=length=38.5mm) was used as the reference. It was also simulated with the same software using

same boundary and excitation conditions within the same frequency range, as the EBG.

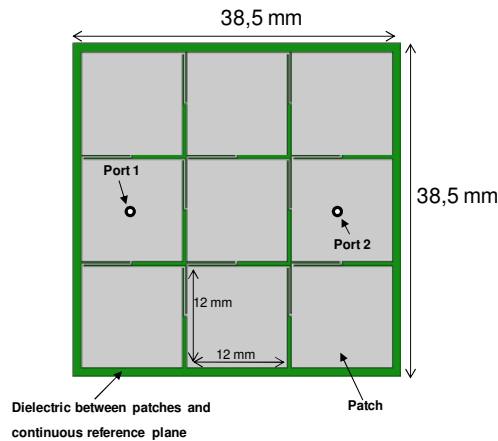


Figure 1: Top view of planar EBG.

The EBG and the reference plane were fabricated and measured. The measurement was performed using a vector network analyzer (VNA) in a frequency range of 100 MHz to 12 GHz. The measurement result is shown in Figure 2. It can be seen in this figure that the proposed EBG structure prevents EMI over the complete range of frequencies, where the RF/analogue circuits for WLAN, Bluetooth, UWB and UMTS operate, as expected. Approximately 10 GHz stopband bandwidth (considering the -50 dB bandwidth) was achieved, thus blocking the propagation of noise within the required band, as predicted.

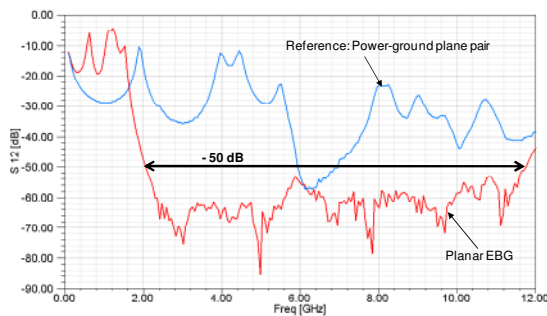


Figure 2: Planar EBG suppresses noise propagation within the entire UWB range.

A. The Return-Path Discontinuity (RPD) Problem

To quantify the impact of the RPD problem caused by EBGs on microstrip lines, a 3 layered board, whose cross-sectional view is shown in Figure 3, was designed. As illustrated in this figure, the

microstrip line (width= 180 μm , thickness= 17 μm , length=30 mm) is routed on the first metal layer with its return-current flowing through the patterned layer of the EBG. The 30 mm long line runs across two EBG cells. For the purpose of comparison, a standard microstrip line routed above a continuous power-ground plane pair with no slots or patches and having the same dimensions as the line routed over the EBG, was also analyzed.

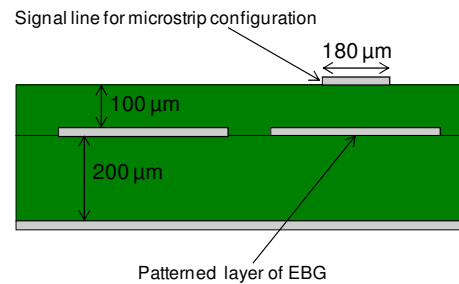


Figure 3: Cross-sectional view of board showing microstrip line routed over EBG.

The insertion losses of both microstrip lines were computed using HFSS and a comparison of the S-parameters obtained is shown in Figure 4.

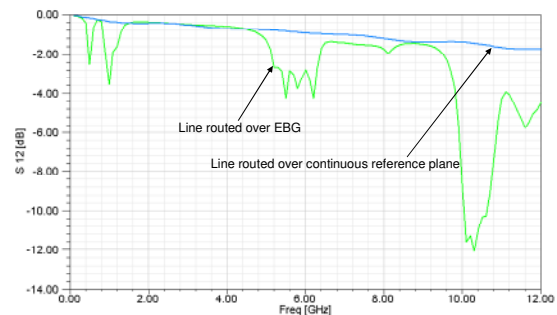


Figure 4: Impact of EBG on the transmission coefficient of a 30mm long microstrip line.

As seen in this figure, the insertion loss of the transmission line routed over the continuous power-ground plane pair is free of resonances. However, in the case where the transmission line is routed over the EBG, there are dips on the insertion loss. The frequencies at which these dips occur correspond to resonance modes of the parallel-plates which form the EBG. The presence of these dips can be explained as follows: The return-current of the microstrip line flows partly as conduction current on the metal strips which interconnect the patches of the EBG, and partly as displacement current between the gaps. This excites the parallel-plate modes. At/around the resonance frequencies of the parallel-plates, strong coupling occurs between the microstrip line and the parallel-plates.

Consequently, much of the power to be transported along the microstrip line is coupled through the slots/slits between the patches of the EBG to the cavity. Part of this power is lost in the cavity and part is radiated at the edges of the plates. For example, at about 5.6 GHz, approximately 60% of power is lost from the microstrip line. At 10.2 GHz, at least 80% of the power is coupled away from the microstrip line and lost. This may lead to system failure.

B. The “Space” Problem

Another issue facing EBGs is that much, if not all, of the board space is used for achieving the required filtering characteristics. This is done using patches, vias, interconnecting metal stripes and at times even surface mount components (capacitors and inductors). Consequently very little space is left for the placement and routing of the system components. The problem of lack of space is illustrated in Figure 5 using some examples of

conventional planar, mushroom and hybrid EBGs published in the open literature.

4. Progress beyond State-of-the-Art: A New Packaging Structure for Noise Isolation – the IPR

The structure and concept of the IPR-structure is presented in section A. In section B, its function as a noise isolation structure are discussed and in section C, the main advantages of this novel structure over conventional noise isolation structures are outlined. It will also be shown in this section how the IPR can be used to minimize EMR problems. Finally in section D, the proof of concept is presented.

A. Structure and Concept of IPR-Structure

The top and cross-sectional views of the IPR structure are presented in Figure 6 and Figure 7, respectively.

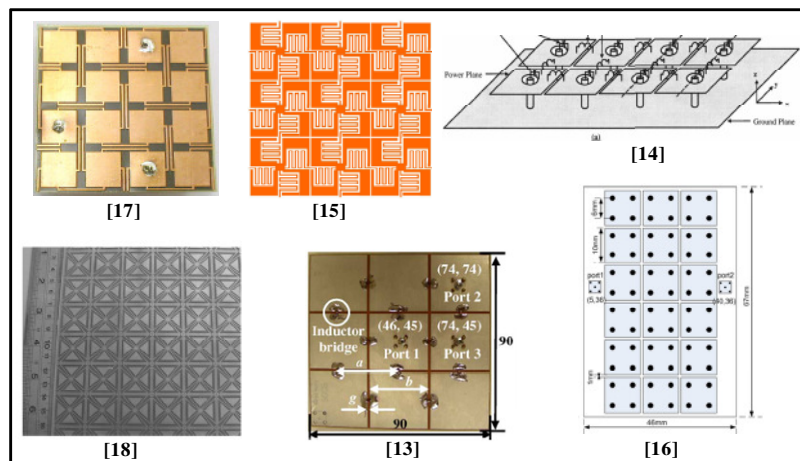


Figure 5: Top views of some conventional EBGs used to illustrate “space” problem.

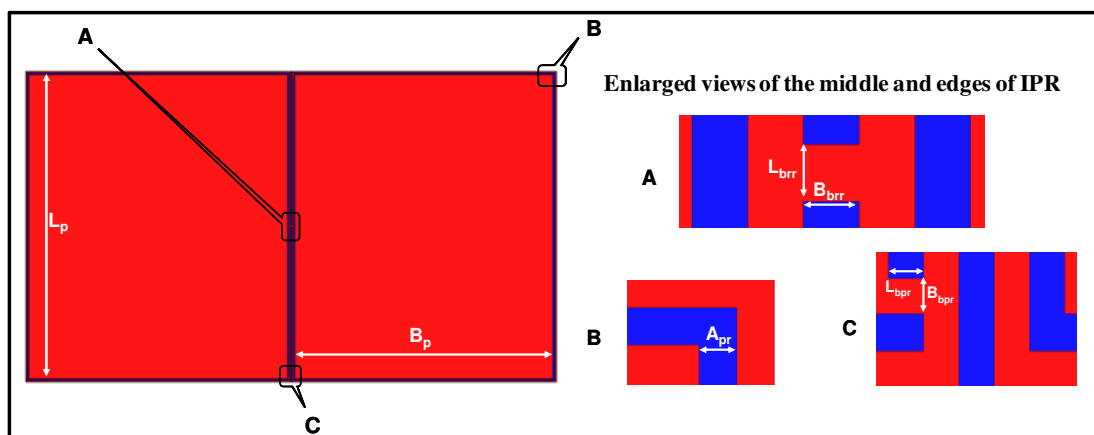


Figure 6: Top view of a new packaging structure for noise isolation – the IPR (left) and enlarged views of middle and edges of the IPR (right).

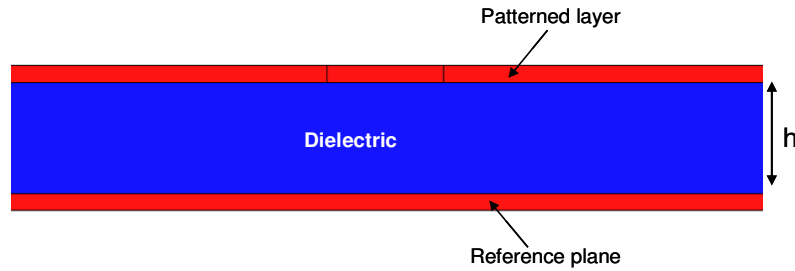


Figure 7: Cross-sectional view of IPR.

It consists of two metal layers and a dielectric layer in-between. Considering the configuration discussed in this paper, one of the metal layers is patterned while the other one is continuous. However, unlike the EBG which consists of numerous periodic patches arranged in an array format, the IPR structure consists of only two large patches, each having a length and width of L_p and B_p , respectively. These patches contribute the majority of capacitance needed to achieve the desired stopband characteristics. However, since the inductance of such large patches is very small, a different means had to be devised to generate large inductances, so as to ensure high isolation and large stopband bandwidths. For this purpose, a metal strip, in the form of a ring, was used around each patch. Since inductance is inversely proportional to the area of the metal strip, a very thin metal strip is required at the edges of the patches to achieve a large inductance. Hence, unlike for EBGs whereby the required inductance is obtained from periodic metal bridges that interconnect each patch, numerous vias and surface mount inductors distributed everywhere on the EBG, the inductance needed for the IPR is obtained from the ring which occupies very little space at the edges of the board. Consequently, much space is left for the placement and routing of components needed for system functionality. By varying the dimensions of the metal strip of the ring, the inductance and hence, stopband characteristics of the IPR can be tuned. Each ring is interconnected with its patch by a metal strip of length L_{bpr} and width B_{bpr} . Another metal strip having a length and width of L_{brr} and width B_{brr} , respectively, interconnects both rings. By ensuring that all the components are interconnected, only one power supply is needed to maintain the same DC level at various parts of the package/board, if required.

B. Noise Isolation using the IPR Structure

In order to illustrate the effectiveness of the IPR-structure for noise isolation, an FR4 board was

used. The inductances and capacitances of the patches and interconnecting metal strips were computed, such that the IPR structure should suppress noise isolation over the frequency range where the GSM, Bluetooth, UMTS and 2.4 GHz WLAN standards operate. For the required bandwidth, the following dimensions were used: $L_p = 40.25$ mm, $B_p = 34.3$ mm and $L_{bpr} = B_{bpr} = L_{brr} = B_{brr} = A_{pr} = h = 0.2$ mm.

Ansoft HFSS was used for electromagnetic field simulations and extraction of S-parameters. A reference power-ground plane pair was also simulated. A comparison of the S-parameters obtained for both structures is shown in Figure 8. As seen in this figure, the IPR creates a large stopband within the desired frequency range, with isolation better than -60 dB. Hence, no noise can propagate in the power-ground cavity.

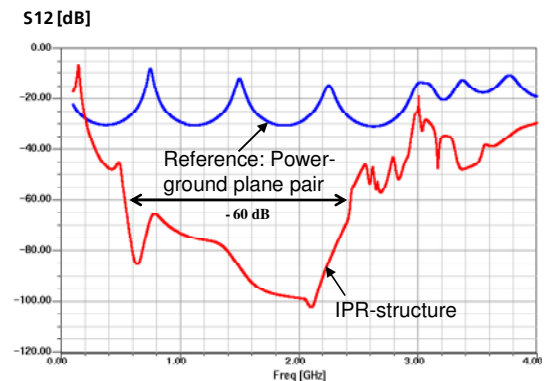


Figure 8: Illustrating the efficiency of the IPR-structure for noise isolation.

C. Some Advantages of the IPR-Structure over EBGs and other Noise Isolation Techniques

In addition to the fact that the IPR-structure is as effective as the EBG in noise isolation/suppression, it also has the following advantages over EBGs and other conventional noise isolation structures:

1) The IPR overcomes the “space” problem. It requires very little package/board space to achieve

the needed isolation. Hence, it ensures that much of the package/board space is used for placement and routing of components needed for system functionality. Hence, when IPR-structures are used, a higher integration density in electronic packages and boards can be achieved.

2) By using the IPR structure, electromagnetic reliability (EMR) problems can be minimized, because the return-currents of transmission lines referenced to the patterned layer of the IPR structure flowing through a large continuous plane. RPD problems would occur only if the lines are routed between both patches.

3) The manufacturing cost of the IPR is low, because neither vias, surface-mount components nor expensive lossy dielectrics are needed. Furthermore, the IPR is very simple in nature and consists only of two metal layers, a patch, ring and the interconnecting metal stripes. No special manufacturing processes or packaging materials are required for the fabrication. Standard techniques can be applied.

4) Large and controllable stopband bandwidth as well as high isolation: By varying the dimensions of the ring, interconnecting metal strips and the patch, the stopband characteristics of the IPR structure can easily be tuned.

D. Illustrating how the IPR overcomes the “Space” and RPD Problems

The IPR overcomes the “space” problem by utilizing only a very small area at the edges of the patch to route a metal strip (in the form of a ring) which accounts for the necessary inductance. Consequently, much of the space is left for placement and routing of system components. This advantage of “space” leads directly to the advantage of reduced EMR issues. That is, since much space is available, the transmission lines are routed over a continuous reference plane such that their return-currents flow un-interrupted. Consequently, the RPD problem is prevented. This is illustrated in the following paragraph.

The microstrip line used for this illustration has the same dimensions as the one used in section 3. In Figure 9, the top view of the microstrip line on the IPR is shown. Since the IPR structure allows enough space for placement and routing of components, the 30 mm long microstrip line was placed such that its return-current flows predominantly over the part of the patterned reference plane that is continuous. Another microstrip line was also designed, to serve as the reference. In this case, a continuous power-ground plane pair was used as the reference plane of the

microstrip line. Both microstrip lines were simulated with HFSS using the same excitation and boundary conditions.

A comparison of the insertion losses of the microstrip lines is shown in Figure 10. As seen in this figure, the insertion loss of the microstrip line routed over the IPR is free of resonances. It is the same as that of the line routed over the reference plane. These results confirm the fact that the IPR prevents the occurrence of RPD issues, which normally occurs for transmission lines routed over EBGs, as shown in Figure 4.

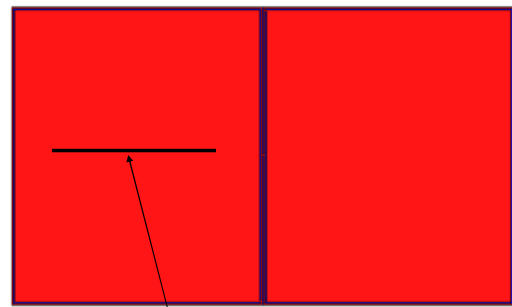


Figure 9: Illustrating how the IPR overcomes the “space” problem.

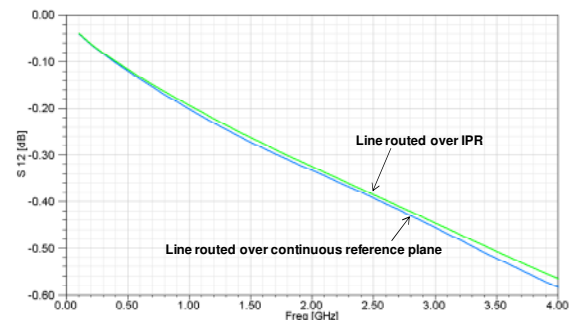


Figure 10: Illustrating how the IPR overcomes the RPD problem.

6. Experimental Validation (Proof of Concept)

In order to experimentally validate the concept of the IPR, test samples were designed, fabricated and measured. For the fabrication of the samples, FR4 substrate having a thickness of 1.5 mm, a relative dielectric constant of 4.2 and loss tangent of 0.02 was used. Each IPR patch has a length of 48 mm and width of 43 mm. All the other dimensions are the same as those used in the simulation in section 4B. The measurement was also performed with the same VNA as the EBG and the result obtained is shown in Figure 11. As can be seen, a good isolation of -36 dB was obtained from approximately 780 MHz to 2.6 GHz. That implies,

when 2 components are mounted on the IPR not more than 0.03% of noise can couple between them. This measurement result validates the concept of the IPR for noise suppression.

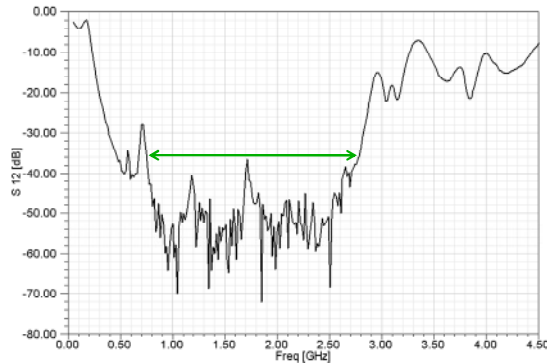


Figure 11: Measurement results of IPR showing good isolation within required frequency range.

For experimental validation of the electromagnetic field simulations, the simulation and measurement results were compared (see Figure 12). As can be seen, a good correlation was also obtained. The very slight discrepancy is as a result of the process tolerances that occurred during the fabrication of the IPR.

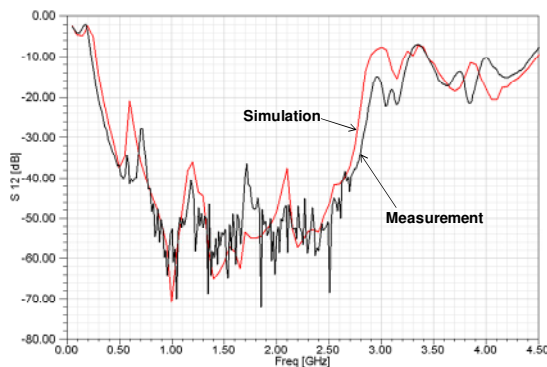


Figure 12: Comparison of measurement and simulation results of the IPR.

6. Summary

The state-of-the-art structures/techniques in preventing the generation and propagation of noise in electronic packages and boards are presented. Using a planar EBG as an example, some of the limitations of these techniques are illustrated. To overcome these limitations, a novel noise isolation/suppression structure, the IPR is proposed, modeled and analyzed. Test samples are then fabricated and measured. The measurement results

show good isolation throughout the required frequency range, thus experimentally validating the concept of the IPR for noise isolation (Proof of Concept). To validate the numerical simulations, a comparison was also made between measurement and simulation results. A very good correlation was obtained.

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