

High Density Hearing Aid Chip Packaging

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Abstract

There has been enormous worldwide effort to increase the volumetric efficiency of electronic packaging. Much of this effort has been driven by the telecommunications industry that has succeeded in reducing cell phone size while simultaneously increasing functionality. The hearing aid business has always had the need to use extremely small electronic packaging because hearing aids pack electronics into the ear canal. Today's hearing aids such as Starkey's S-Series product have extensive computing power and run sophisticated hearing algorithms that have tremendous impact on a patient's quality of life. The industry trend is to put more memory, more signal processing capability and more wireless capability into hearing aids to increase functionality and to improve performance. In order to achieve higher performance, the hearing business has had to develop and execute 3D packaging well ahead of other industries. This paper will examine the history of ceramic packaging at Starkey. The challenges and drivers for each technology step will be addressed. Various issues will be examined including: available ASIC technologies, impact of chip metallization, solder interconnect temperature hierarchy, overcoming routing design limits, use of embedded passives, mixed wire bonded and flip chip attached die, and materials limitations. The following technology changes will be examined along with their impact on thick film ceramic device packaging: move from analog to digital devices, benefits realized utilizing flip chip attach, chip stacking, use of conductive epoxy instead of solder, migration to stacked thick film ceramic interconnect layers using vertical interconnect channels, and the incorporation of RF devices.

Key words: Thick Film, Chip-on-flip-chip (COFC), Vertical Interconnect (VIC), Multi-chip module (MCM) and System in a Package (SIP).

Introduction

There has been a voracious drive to put more electronics into smaller and smaller spaces. For many years high end mainframe computers dominated this push. In the 1980's two dimensional thinking dominated improvements, but was rapidly reaching the limits of how many devices could be placed on a planar circuit board. IBM's Thermal Conduction Module (TCM) was widely considered as the crowning achievement of what could be done. [1]

By the 1990's consumer products were starting to drive low cost progress in putting more processing power in less space. The laptop computer, cell phones, hand held video cameras and digital photography were just a few of the technology drivers. There is a never ending desire to put more capability into consumer products and a passion to make everything wireless. Portability of everything is now a real possibility. For example, in 1984 a single CPU unit mainframe computer the size of a refrigerator plus the support system of air and/or water cooling units ran at 25 million instructions per second (25 Mips). Today a dual core processor laptop exceeds that by more than four times.

By the late 1990's and early 2000's electronics was powerful enough and small enough to make putting significant computing systems inside people a real possibility. The hearing aid business has always had the need to use extremely small electronic packaging because hearing aids pack electronics into the ear canal. [2,3] Today's hearing aids such as Starkey's Zon product have extensive computing power and run sophisticated hearing algorithms that have tremendous impact on a patient's quality of life. One example is automatic feedback cancellation. This technology is a marriage of hardware digital signal processing and high performance software that instantly and completely

eliminates all audible feedback. In order to achieve this kind of performance, the hearing business has had to develop and execute 3D packaging well ahead of other industries. The hearing business has been an early adopter of technologies such as flip chip, multi-chip modules, chip stacking, embedded components, 3D multi-level ceramic hybrid circuits, and much more. Power consumption must be kept to a minimum since hearing aids are powered by low voltage 1.3 V DC zinc air batteries; therefore, heat and power dissipation are generally not design constraints.

This paper will examine some of the key electronic packaging technologies used in many hearing applications from 1995 until 2008. Discussion will include production and developmental hardware features, decision drivers, technology enablers, technical challenges and real world solutions.

Results

First Flip Chip hybrid

The first 3D packaging solution featured a single flip chip thick film ceramic hybrid with embedded capacitors and was introduced to mass production in 1995 to meet the huge customer demand for new, tiny, custom hearing aids called CICs (completely in the canal). The heart of this single chip package (Figure 1) was a custom ASIC that boasted state-of-the-art compression and automatic gain adjustment which provided the user with rapid (milliseconds) output level response to ever changing acoustic environments.

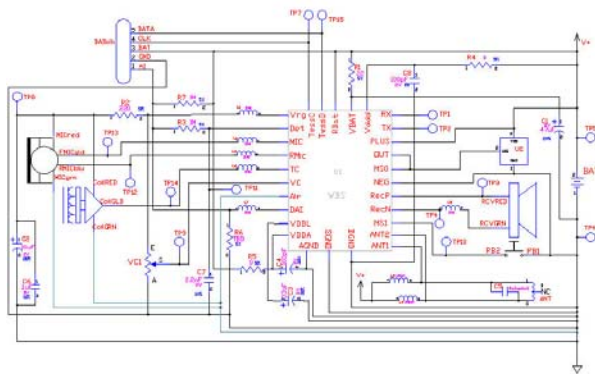


Figure 1. The hybrid includes most of the electronics in a hearing aid circuit. See schematic.

The finished package outline dimensions were 6.5 mm x 3.0 mm x 1.25 mm (25.6 mm³). The flip chip was a custom, 2.18 mm x 4.29 mm, analog ASIC with 23 100 μm x 100 μm gold bump pads.

The capacitors were standard value 0402 ceramic multilayer components.

Several challenges had to be overcome during the development process. First, the IC was unavailable with solder bumped pads. Lack of solder bumps drove the decision to seek alternative flip chip attachment techniques. Second, the flip chip attachment process demanded IC placement accuracy beyond the current manufacturing capability of the time. And third, our relative inexperience with flip chip technology led to a surprise discovery late in the development cycle that the hybrid was adversely affected by IR radiation – a real problem for hearing aids which are frequently exposed to sunlight during normal use.

To address the first challenge, isotropic conductive adhesive was selected for the flip chip attachment method. The material we chose was a silver filled, screen printable, single part epoxy with adequate adhesive strength. Several key characteristics of this epoxy were 90 $\mu\Omega\text{-cm}$ volume resistivity, 60,000 cPs viscosity, and 24 MPa die shear strength for a 227 μm x 227 μm IC. Advantages of this method were: smallest possible hybrid package, lower processing temperature (compared to high temperature gold compatible solder), screen printing competency, and relative cost. Disadvantages included tight flip chip placement accuracy requirements (+/- 37.5 μm), more stringent control of substrate cleanliness, longer processing time, and the circuits were now not reworkable.

The selection of conductive epoxy flip chip attachment necessitated the procurement of a highly accurate piece of flip chip placement equipment; we chose the Universal GSM pick and place machine. We quickly adapted our 76.2 mm x 76.2 mm printed thick film ceramic substrates to maximize the placement fiducial recognition of the GSM's unique camera and lighting system. Steps were added to the assembly process to assure that substrates were extremely clean prior to conductive epoxy printing. A special daisy chain flip chip IC and test substrate were designed and used for incoming inspection of each lot of conductive epoxy.

During hybrid qualification testing we discovered that the circuit's analog output signal became distorted when the circuit was exposed to a powerful light source. We had been aware that most IC's handled in production were light sensitive during assembly, but in the past our packaging solutions involved wire bonding the die to the substrate (active side up) followed by application of an opaque glob top encapsulant which provided sufficient light blocking.

We soon realized that the flip chip configuration placed the active side of the IC directly atop a thin ($375\text{ }\mu\text{m}$), white ceramic substrate, which readily allows light to penetrate from all exposed surfaces. Research at the time revealed that the IC was specifically sensitive to electromagnetic radiation in the IR band. Sunlight and typical artificial light sources emit broadband radiation including ample energy in the IR band to impact the IC. Our first solution was to switch to black alumina substrates, but while light sensitivity was eliminated, we discovered that the adhesion strength of external thick film solder pads was much lower compared to the normal white, 96% alumina substrates we utilized; therefore, black alumina was an unacceptable alternative. We turned to our thick film ink supplier who developed a special blend of opaque dielectric ink. This ink was fired onto the external surface of the ceramic substrate during the normal thick film printing process instead of the old, more translucent dielectric. This solution proved effective against light penetration and remains in use today.

First 3D Thick Film Multichip Module

Responding to a growing market demand for easier to use, programmable ITE hearing instruments, Starkey next developed its first 3D multichip module package in 1997. This package featured the previously mentioned custom ASIC amplifier combined with a programmable IC. See Figure 2. Along with unique hearing aid fitting software, the dispenser was now able to select from a set of discrete values for a given acoustic characteristic (such as compression ratio and gain) to tailor the hearing aid for the patient. The hearing aid became both smaller and simpler because discrete, user-adjustable potentiometers were eliminated. This provided benefit for both dispenser and patient since successful fittings became easier to achieve.

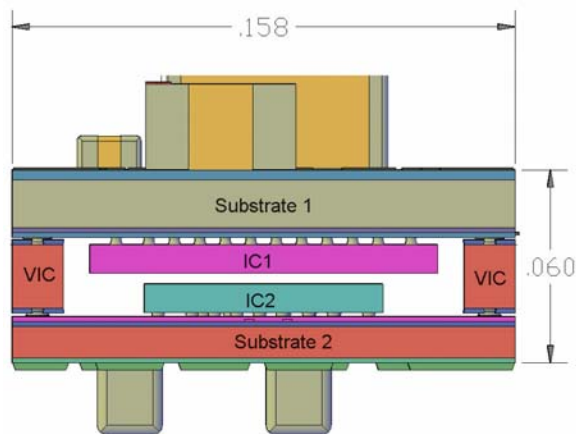


Figure 2. Side view of 1st 3D package. Dimensions are in inches.

The programmable IC was an off-the-shelf die featuring four memories, six programmable resistors, and two programmable switches developed specifically for the hearing aid industry. The IC was $2.07\text{ mm} \times 2.47\text{ mm} \times 0.25\text{ mm}$ thick, with $114\text{ }\mu\text{m} \times 114\text{ }\mu\text{m}$ gold bump pads, at $380\text{ }\mu\text{m}$ pitch. The IC was flip chip attached with conductive epoxy.

The design team was now faced with a new challenge: how to accommodate a second die along with three more required I/O pads (18 total) and one more 0402 chip capacitor in a form factor that could not be grown in the X-Y ($3.05\text{ mm} \times 6.60\text{ mm}$) plane. The solution was a novel invention called the vertical interconnects (VIC). [4] The VIC allowed the package to grow in the Z-axis while maintaining a slim $2.79\text{ mm} \times 5.56\text{ mm}$ in the X-Y plane. The VIC was a piece 96% alumina containing a linear array of $200\text{ }\mu\text{m}$ diameter laser drilled through holes at a pitch of $450\text{ }\mu\text{m}$. The holes were filled with conventional thick film conductive paste with high silver content and low Z-axis shrinkage. Additionally, each VIC array contained two fiducial for placement camera visual recognition and an orientation mark.

Manufacturing was faced with three primary challenges: silver epoxy printing registration, VIC placement accuracy, and surface cleanliness. We knew from our previously described first flip chip package how to maintain consistent silver epoxy registration in the screen print process when the substrate was a flat 76.2 mm by 76.2 mm ceramic substrate. The challenge now was to print silver epoxy atop the VICs which behaved as speed bumps to the screen printer's squeegee. The solution was a carefully designed, stainless steel, lasered stencil, and extensive operator training. The dimensional consistency of the package's Z-axis was improved by lapping the ceramic VIC substrate from $625\text{ }\mu\text{m}$ to $825\text{ }\mu\text{m}$. Another benefit of lapping was then discovered; VIC placement accuracy was enhanced by creation of a very well defined fiducial. A laser drilled through hole that was subsequently filled and lapped, proved to be the most dependable fiducial.

Surface cleanliness became paramount. Thin oxide or epoxy resin films on bond pads proved to be the most troublesome because these films were typically invisible to operators working under 10-30X stereo microscopes. The symptoms of thin film contamination in a conductive epoxy system are unstable electrical performance often exasperated by thermal cycling. The average series resistance of a good VIC connection (includes through hole material plus both conductive epoxy connections on each end) was $35\text{ m}\Omega$. Defective connections exhibited resistances ten times or more than the good connections and often were unstable. In the failure analysis lab we found that it was not unusual for a

defective, high resistance connection to heal during the process of curve tracing with application of test voltages as low as 0.5 to 1.0 volts. A good quality precision resistance meter equipped with 4 lead sensing and a dry circuit test feature proved to be essential for characterizing conductive epoxy connection integrity.

One specific source of contamination was traced to the VIC dicing saw process. Thin film residue discovered on packaged VIC's prior to placement into the 3D module was traced to the saw mount material with the help of FTIR analysis. A new mounting material with a lower volatile organic compound (VOC) concentration and ionic content was qualified and curing ventilation was improved to remedy this issue.

Care also had to be taken to avoid introducing contamination during special processing and handling. For example, if the silver epoxy registration on a particular panel was unacceptable, the panel required rework. It is important to state that the assembly environment was a HEPA filtered class 100,000 clean room.

1st 3D Hybrid with 3 Flip Chip Die

The success of our first VIC-based 3D package was leveraged by extending the concept to a BGA style package containing a third quad op-amp flip chip IC in addition to the two flip chip die described in the previous section. Customer desire for high power performance with the flexibility of programmability was the driver for this BTE application. The BGA outline dimensions are shown below. The quad op-amp IC was 1.525 mm x 1.375 mm, lapped to 250 μ m thick with ten 100 μ m x 100 μ m gold bumped I/O pads at 250 μ m pitch. This 1999 package was loaded with passive components: 19 chip components (nine 0402, eight 0302, two 0603), five thick film resistors (laser trimmed embedded components to be discussed shortly), and two larger VICs with 18 through holes. See Figure 3. All three die were flipped chip attached with conductive epoxy to a common BGA substrate (the downstairs subassembly). The upstairs assembly contained 19 passive components with the two 18 hole VICs serving as the walls and providing electrical connectivity between the upstairs and downstairs subassemblies.

The challenges mentioned previously applied to this complex package, with the added constraint that the package had to survive solder reflow attachment to a PCB assembly. During initial solder reflow reliability testing a fascinating discovery was made: a thin inorganic contamination film was causing erratic electrical performance of the SMD assembly. Determining root cause of this

problem proved to be very challenging given the package complexity. Circuit's exhibiting this adverse behavior frequently healed during the trouble shooting process and behaved normally thereafter. Eventually the problem was isolated to a thin film of contamination which covered some of the flip chip pads prior to printing silver epoxy. This film could not be seen with conventional stereomicroscopes. The only detection method in-house was a high power metallurgic microscope equipped with differential interference contrast (DIC) lighting.

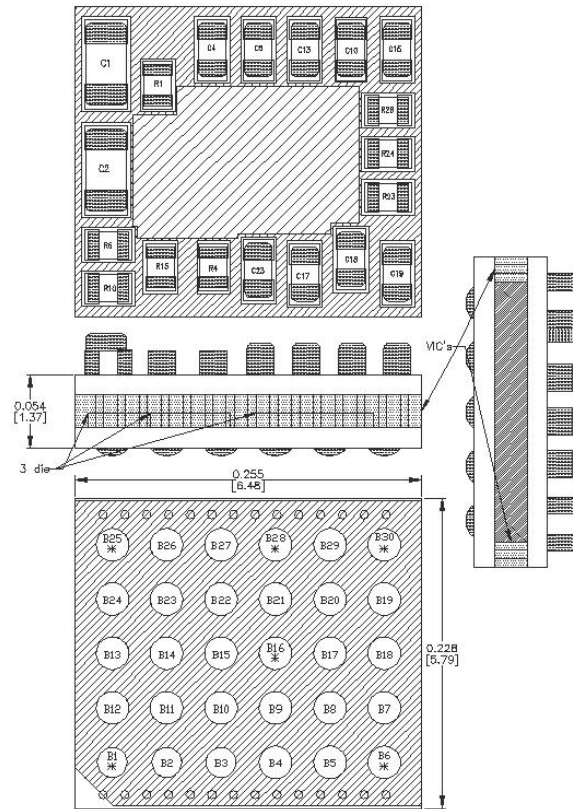


Figure 3. 3D thick film hybrid with VIC, top surface passives and 3 die on the top of the bottom substrate surface. Dimensions are in inches.

The prism was adjusted to obtain just the right amount of surface light reflection to make the film appear as a faint rainbow at 100-200X.

We learned that the epoxy flip chip connections contaminated with the film behaved either as an open or intermittently open circuit for applied curve tracer voltages from 0 volts up to about 1 volt DC. The connection would then heal and conduct normally after slowly increasing the voltage from about 1 to 1.5 volts DC. SEM/EDX analysis revealed the film was dielectric material (glass) which had redeposited onto the substrate around the thick film resistors where the laser cuts were made.

See Figure 4. This phenomenon was dubiously nicknamed post laser drip (PLD). Since each thick film printed resistor has a unique laser trim pattern, the amount and location of PLD varied on every circuit. At first, methods to prevent the PLD from depositing on the substrates were pursued; later it seemed that a more practical solution was to remove the PLD after trimming using a burnish and wash method. Burnishing is a light mechanical abrasion of the substrate surface; washing was accomplished with acetone. This burnish-and-wash operation proved to be effective provided process indicators were consistently monitored. See Figure 5.

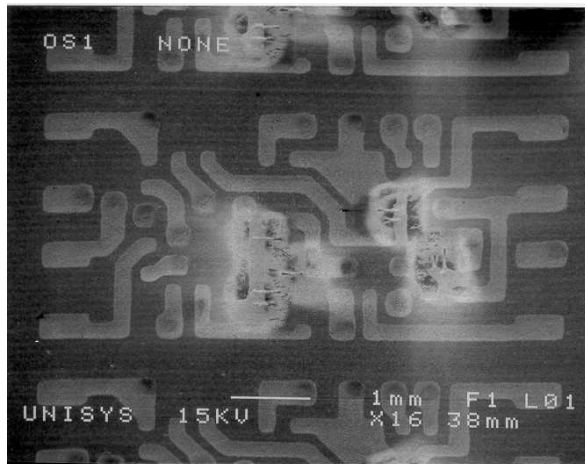


Figure 4. SEM image of thick film substrate before laser trim. White clouds are PLD regions around laser trimmed resistors.

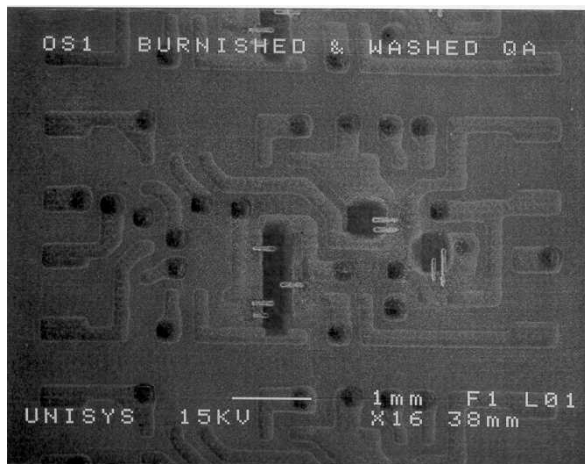


Figure 5. Thick film substrate after burnish & wash. PLD was successfully removed.

1st Digital Thick Film Module

The drive for digital performance in high power BTE hearing instruments led to the creation of yet another 3 chip package; in 2001 a MCM package

with a module-on-flip-chip arrangement was developed and shown in Figure 6. This time the hearing application was a truly digital BTE product – not just an analog product with limited programmable modes. The physical constraint imposed by the surface area of three die demanded a stacked, vertical approach as shown in the cross-sectional view above. Fortunately there was some available room to grow the package vertically within the BTE.

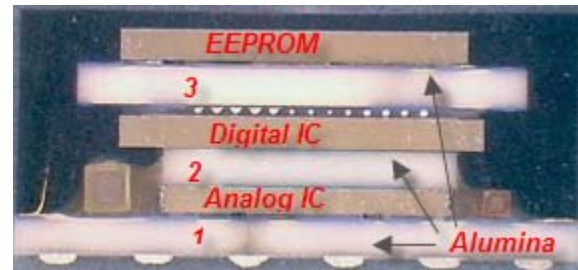


Figure 6. 3 chip stack with thick film ceramic interposer and spacer.

The analog IC, digital IC, and EEPROM die were each mounted in flip chip fashion and connected by means of solder; this was the first time solder was used for flip chip attachment in high volume production. First, the analog IC with gold bumped I/O pads was solder reflow attached to an alumina substrate (1) along with two embedded chip capacitors, and then underfilled. An alumina spacer (2) was then added atop the analog IC. In a separate operation, the digital and EEPROM ICs bumped with 4 mil 63/37 eutectic Sn/Pb solder bumps were reflow attached to a different alumina substrate (3), underfilled, diced into individual modules, and placed atop the analog IC's spacer. Connections from the top (3) were made to the base substrate (1) via 25 μ m gold wire bonds. The finished package outline dimensions are shown in Figure 7.

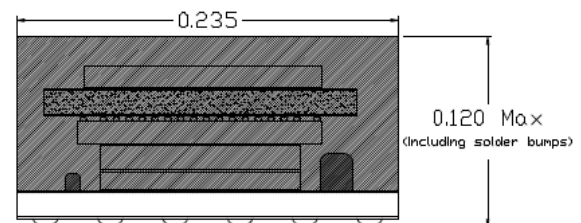


Figure 7. Hybrid dimensions in inches for 3 chip stack. Dimensions are in inches.

Several technical advancements at the time enabled this design: better underfill, availability of 63/37 Pb/Sn solder bumped digital die, and wire bonding improvements. The primary challenge faced with this package was making it robust enough to survive 3X convection solder reflow cycles. Initial

samples exhibited solder shorting between the analog IC's flip chip joints. Failure analysis revealed underfill voids (Figure 8) under the analog chip as the cause of the flip chip shorts. This was remedied by modifications to the underfill dispense pattern and technique.

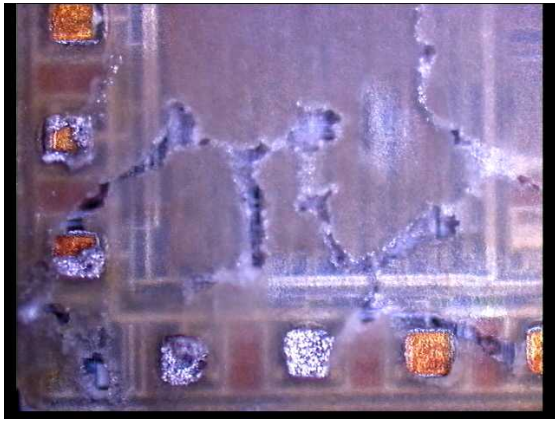


Figure 8. Underfill voids visible after analog IC was removed.

Solder shorts under the embedded capacitors (Figure 9) was the second problem faced. This proved more difficult to remedy, possibly because of physical variations in the solder joint from part to part. We found that switching to a higher temperature lead indium solder, optimizing the reflow profile, and modifying the underfill dispense technique substantially reduced the occurrence of solder shorts.



Figure 9. Chip capacitor was removed to show solder shorts beneath the capacitor.

Improved Digital Thick Film Module

Hearing aid users were benefiting from the digital advantage and continued to demand greater performance. This drove IC development to merge the

separate analog and digital functions described in the previous package into one silicon DSP chip. This 2003 innovation enabled creation of a powerful DSP hybrid comprised of one DSP chip (3.78 mm x 2.35 mm x 0.33 mm thick) and one memory IC (1.77 mm x 3.08 mm). The approach was a chip on flip chip (COFC) package which contained 8 passive chip components and 14 I/O pads. See Figure 10.

First, the DSP IC was flip chip mounted and reflowed via its 50, 85 μ m diameter, 63/37 Pb/Sn solder bumps. Next, the EEPROM IC was mounted, with its 75 μ m x 75 μ m aluminum wire bond pads face up, atop the DSP die. The EEPROM was then wire bond attached to the substrate using conventional thermosonic gold ball bonding. Next came underfill, encapsulation, back side population, reflow, test, and dicing. This device was the simplest DSP hybrid yet to manufacture and proved to be very robust; it recorded a 1st time pass through quality and reliability testing.

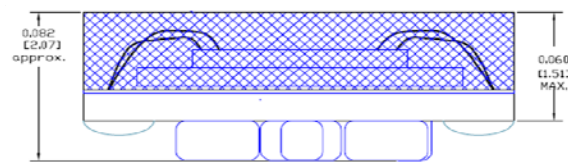


Figure 10. Sketch of a digital COFC hybrid. U1 is a DSP die with dimensions in inches.

Thick Film Hybrid with 3 Stacked Die

Another 2003 three chip solution was necessary to accommodate demand for greater digital functionality in the largest, full shell ITE instruments. The design of this hybrid was similar to the previously described COFC package, but with a third die added atop the second die. Referring to Figure 11, first a solder bumped die (FC1) was attached flip chip style and reflowed onto the alumina substrate. The next die (WB1) was mounted, wire bond pad side up, atop FC1. Finally, the last die (WB2) was populated atop WB1 also with its wire bond pads facing up. In one operation, WB1 and WB2 were wire bonded to the substrate. See Figures 12.

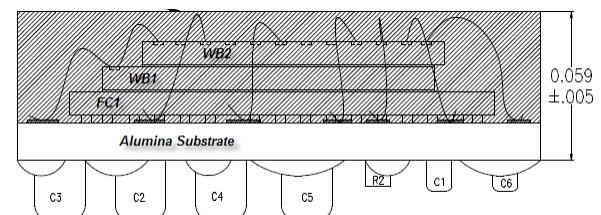


Figure 11. Chip-on-chip on flip-chip package. Dimensions are in inches.

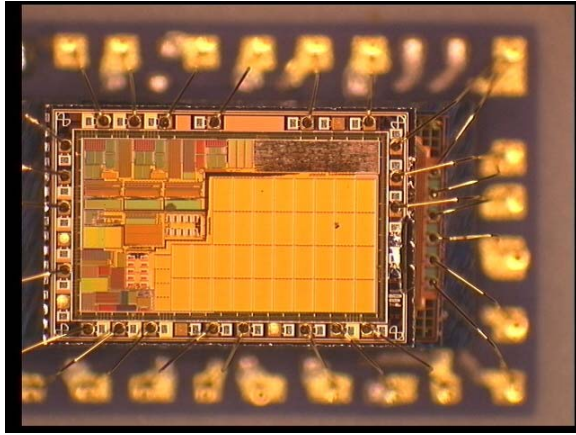


Figure 12. Photograph showing hybrid circuit with 3 stacked die before encapsulation. Top two die are resting atop a flip chip die.

The device was then underfilled, encapsulated, and completed the remaining processing steps. The die were custom designed for this application which enabled us to optimize the wire bond pad locations of WB1 and WB2 for thermosonic gold ball bonding using a Hughes/Palomar 2460-III machine. Even so, wire bonding proved to be a challenge for manufacturing due primarily to variation in the stack height and X-Y position of the top two die (WB1 & WB2). A 2nd challenge was placing WB2 atop WB1 without damaging WB1's active area in the process. Wire bonding improvements were achieved by tightening the placement accuracy of the WB1 IC after it was learned that adequate clearance was needed between the wire bonder's capillary and the edge of WB1. The WB1 positional accuracy was incrementally improved by optimizing the dispense pattern and amount of die attach epoxy used secure WB1 to the flip chip. Increased care was needed with the selection and maintenance of the pick and place nozzle used for populating WB1 and WB2 in order to reduce damage to WB1's active surface.

Also, dirty die left tiny, silicon particles embedded in the pick tool which contributed to IC damage. That led to tighter scrutiny of incoming die; they were examined closely for the presence of chips or random silicon particles collected around the die edge. Preventive maintenance on the wire bonder was increased; pick tools were checked and replaced more frequently.

Wireless Hearing Aid Hybrid

Hearing aid packaging of electronic systems eventually needed to include wireless technology. Wireless technology enables increased functionality for patients and improved patient experience during visits with audiologists. Any wireless technology

needed to include at least a radio transceiver, antenna, passive components and glue logic to mate with system memory and digital signal processor. Once again the challenge of putting more components into the ear canal for CIC applications drove innovation. A thick film ceramic hybrid 3D package was selected. The final part size was 6.025 mm x 3.950 mm x 3.350 mm (l/w/h). Thick film ceramic vertical interconnect components were used to support a second thick film ceramic circuit board to add wireless components. The package included 25 passive components (six 0402, fifteen 0201, one 0603, one crystal oscillator & two VICs), three die (DSP, EEPROM & Radio), three thick film resistors (thick film passive components were limited because they consume too much space), and twenty input/output pads. All die were connected using flip chip solder attach. The top of the hybrid structure is shown in Figure 13.

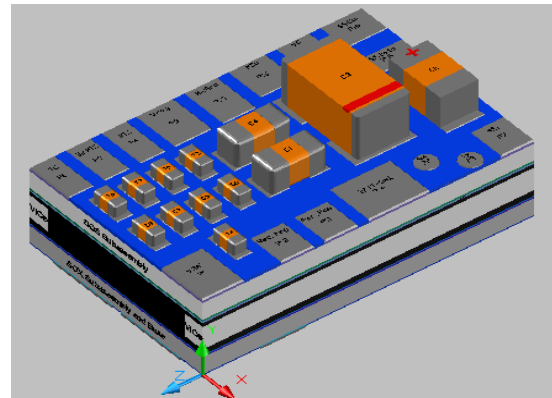


Figure 13. Structure of the bottom surface of the hybrid.

The hybrid MCM had 85% of available route channels filled and 100% of the surfaces filled; apparent vacant space is required for performance reasons. Two major challenges that needed to be overcome included: escaping from the DSP and radio chips and increasing routing density of the thick film ceramic substrates.

The DSP had 39 I/O, the radio chip had 35 I/O and the EEPROM had 8 I/O. All of the vertical interconnect channels were used; each VIC contained 16 surface-to-surface connections. The VIC ceramics also act as stand-offs that hold the top and bottom ceramic substrates apart by 500 μ m. See Figure 14. All die are underfilled and the space between the ceramic substrates is encapsulated. Finite element analysis was used to explore the margins of the design space and was the subject of a previous paper. [5]

The thick film ceramic technology route density was insufficient to support this design and

required a major improvement. The final design used 87.5 μm lines and spaces with 100 μm vias and 125 μm via capture pads. DuPont FodelTM was used to enable this MCM and was the topic of a previous paper. [6]

There was insufficient space on the ceramic substrates to incorporate an antenna so two pads on the top surface lead to an antenna on the hearing aid faceplate. The DSP was an ultra low power processor operating at 5.12 MHz and consuming only 950 μA . The DSP had both a main 16-bit processor unit and a coprocessor. A 512K EEPROM was used to support the DSP.

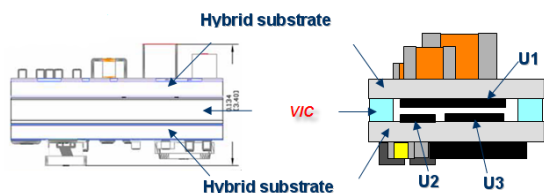


Figure 14. Cross-section of the ceramic hybrid.

Future Products

Every generation of hearing instrument has been more complex than the previous. Each successive product evolution has improved the quality of life of hearing aid customers. Today the horizon is rich with potential technical improvements. [7,8] Hearing aid algorithms are becoming more sophisticated and demanding more I/O, higher processing speed and greater performance. Typical BTE hearing aids are becoming smaller and more style conscious; ITE hearing aids remain size constrained due to the ear canal. Increasing use of wireless technology is enabling breakthrough performance such as highly focused sound fields. Each successive generation has demanded more capability in a smaller space and there is no reason to believe this pattern will not continue; there is every reason to believe technology evolution will accelerate.

Conclusion

The history of hearing aid microelectronics from 1995 to present was examined. Technical solutions to increasing density requirements were explored as well as the key drivers, technology enablers, execution challenges, and real-world solutions. Technical solutions included flip chip die attach, multi-chip modules, chip stacking, 3-dimensional multi-chip modules, digital electronics, integrated passive components, DuPont FodelTM, vertical ceramic interconnect structures, and underfilling of components. The drive to put more electronics into hearing instruments continues as software algorithms demand more memory and faster

processors, and more wireless functionality is required by a technology conscious customer base.

Acknowledgments

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