

## Design and Process of 3D MEMS Packaging

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### ABSTRACT

The design and assembly process of 10 different 3D MEMS packages will be presented and discussed in this study. These 3D MEMS packages integrate the MEMS devices from the MEMS wafer (with either wirebonding pads, or solder-bumped TSV (through silicon via) substrate, or solder-bumped flip chip without TSV), the ASIC chips from the ASIC wafer (with either TSV or without), and the cavity package cap from the cap wafer (with either TSV or without). The assembly process consists of release (etching), singulation, wire bonding, flip chip, TSV, cavity etching, chip-to-wafer (C2W) bonding and wafer-to-wafer (W2W) bonding. It can be shown that these packages lead to small packaging foot-print, high electrical performance, and potentially low cost.

**Key Words:** MEMS, TSV, SiP, 3D IC integration, Low-temperature bonding, Wafer-level packaging

### Introduction

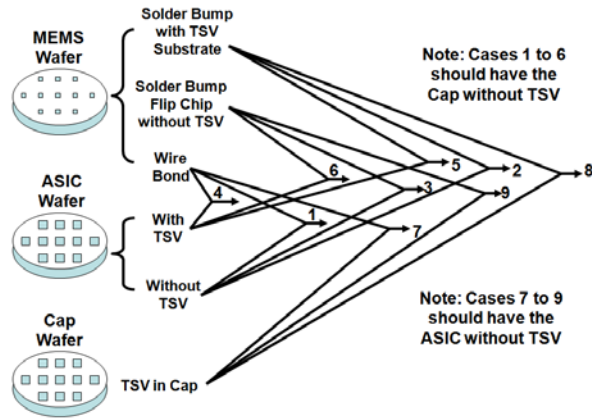
MEMS stand for *microelectromechanical* systems, which are the integration of mechanical elements such as sensors and actuators and electronics on a common silicon substrate through the use of microfabrication technology [1-4]. The same basic technology and process steps such as the etching, patterning, doping, and connecting employed for making conventional electronic integrated circuits (ICs) such as complementary metal-oxide-semiconductors (CMOS) can be used to fabricate (micromachining) micromechanical elements by selectively etching away parts of a silicon wafer or adding new structural layers to form MEMS devices. However, there is a fundamental difference between MEMS and ICs devices - namely; MEMS devices must remain physically movable. MEMS devices use electronics to move their mechanical elements (parts)!

Unlike electronics IC packaging [21-29] MEMS packaging [5-20] is not trivial, is expensive (60 to 80 percent of the product total cost), and is custom-built. Electronics IC packaging is a well-developed technology (e.g., wire bonding, tape automated bonding, and the flip chip). However, MEMS packaging is a specially designed packaging process that is difficult owing to moving structural elements, and it is the most expensive process in micromachining.

Unlike electronics IC packaging [21-29] MEMS packaging [5-20] needs a cap. In order for the moving elements of a MEMS device to move effectively (e.g.,

with minimum damping and stiction) in a well-controlled atmosphere, hermetic sealing of the MEMS device in a cap is necessary. For some MEMS devices (e.g., resonators, infrared bolometers, and gyroscopes), vacuum packaging is even required. Usually, the cap is processed at the wafer level, and thus MEMS packaging is truly a wafer-level packaging.

Just like electronics IC devices [21-29] MEMS devices [5-20] are not isolated islands. They must communicate with other IC chips in a circuit through an input/output (I/O) system of interconnects. Furthermore, the MEMS device needs to be powered up, and its embedded circuitry and moving elements are delicate, requiring the package to both carry and protect the device. Consequently, the major functions of MEMS packaging are (1) to provide a path for the electrical current that powers the circuit and moves the moving elements, (2) to distribute the signals onto and off the MEMS device, (3) to remove the heat generated by the circuit, and (4) to support and protect the MEMS device from hostile environments. In this study, the design of 10 different configurations of 3D MEMS packaging which meet these requirements are presented. Also, these packages are supposed to yield low-cost, high-performance, and small footprints. Furthermore, the packaging assembly processes of these 3D packages are provided and discussed. Emphases are placed on the low-temperature bonding, MEMS chip to ASIC wafer bonding and ASIC wafer to cap wafer bonding.

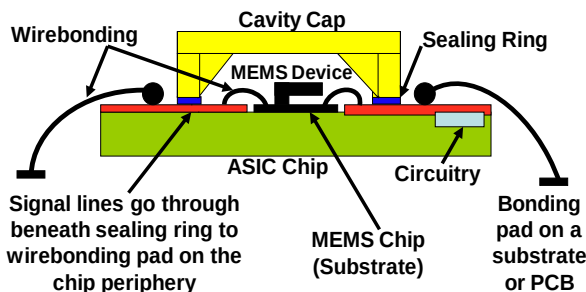


**Figure 1** Nine different designs of 3D MEMS packaging from the MEMS, ASIC, and cavity-cap wafers

### Design of 3D MEMS Packaging

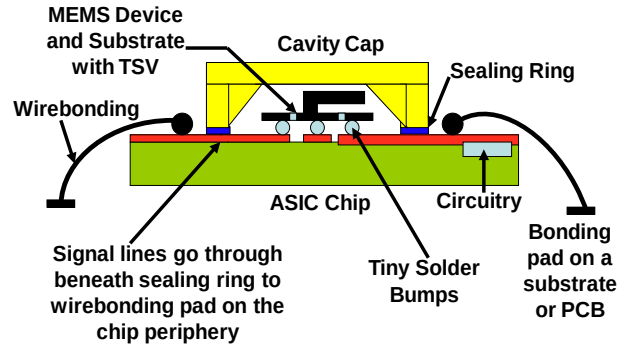
Advanced 3D MEMS packaging usually involves 3 wafers, namely the MEMS device wafer, the ASIC wafer, and the cavity cap wafer. Figure 1 shows nine different combinations (designs) of 3D MEMS packaging from the MEMS wafer (with either wire bonding pads, solder-bumped TSV substrate, or solder-bumped flip-chip without TSV), the ASIC wafer (with or without TSV), and the cavity-cap wafer (with or without TSV).

**Case 1:** The MEMS device is die attached and then wire bonded on the ASIC chip or wafer. The cavity-cap chip/wafer is attached to the ASIC chip/wafer with a sealing ring, as shown in Figure 2. The signal lines go through beneath the sealing ring to the wirebonding pad on the ASIC chip periphery. Another set of wirebonding pads connects the MEMS/ASIC 3D stack to either a substrate in a package or on a PCB.



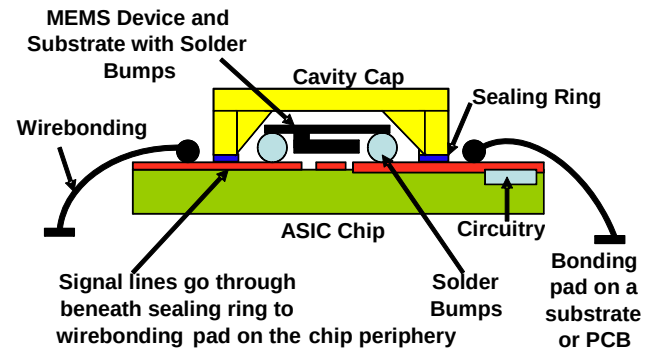
**Figure 2** Wire-bonding 3D MEMS packaging with lateral electrical feed-through

**Case 2:** The micro-solder-bumped MEMS device with a TSV substrate is first attached to the ASIC, as shown in Figure 3. The rest is the same as in case 1.



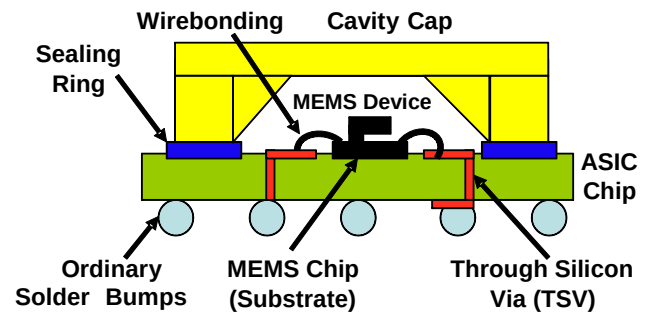
**Figure 3** Solder-bumped MEMS device with TSV substrate on an ASIC chip with lateral electrical feed-through

**Case 3:** The solder-bumped flip-chip MEMS device is first attached on the ASIC, as shown in Figure 4. The rest is the same as in case 1.



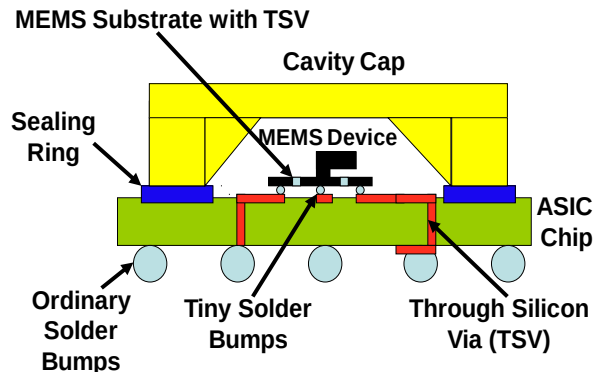
**Figure 4** Solder-bumped flip-chip MEMS device on an ASIC with lateral electrical feed-through

**Case 4:** The MEMS device is die attached and wire bonded on the ASIC chip with TSV and ordinary solder bumps, as shown in Figure 5. A cavity cap is attached on the ASIC with a sealing ring. The MEMS/ASIC 3D stack is then attached (solder reflowed) to a substrate in a package or on a PCB.



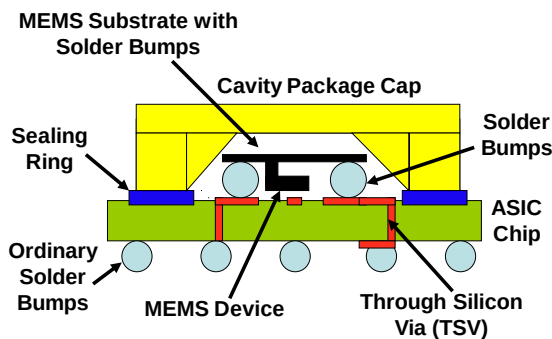
**Figure 5** MEMS device wire bonded on an ASIC with vertical electrical feed-through TSV

**Case 5:** The micro-solder-bumped MEMS device with a TSV substrate is first attached to the ASIC chip/wafer with TSV and ordinary solder bumps, as shown in Figure 6. The rest is the same as in case 4.



**Figure 6** TSV MEMS device solder bonded on an ASIC with vertical electrical feed-through TSV

**Case 6:** The solder-bumped MEMS device is first attached to the TSV ASIC with ordinary solder bumps, as shown in Figure 7. The rest is the same as in case 5.

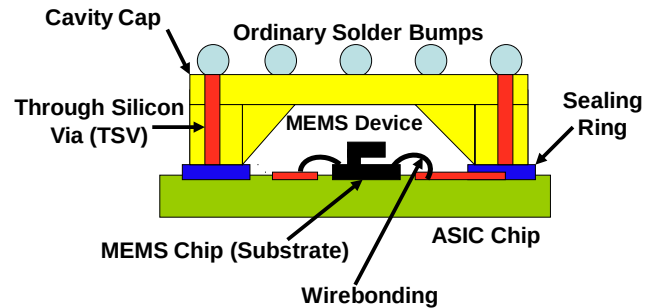


**Figure 7** Solder bumped MEMS device flip-chip on an ASIC with vertical electrical feed-through TSV

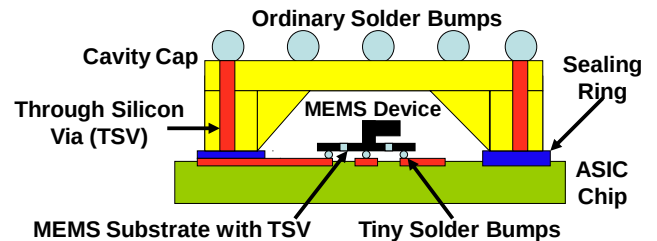
**Case 7:** The MEMS device is die attached and then wire bonded on the ASIC chip/wafer. The cavity cap with TSV and ordinary solder bumps is attached to the ASIC with a sealing ring, as shown in Figure 8. Then the whole 3D carrier is attached (solder reflowed) to a substrate in a package or on a PCB.

**Case 8:** The micro-solder-bumped MEMS device with TSV substrate is first attached to the ASIC as shown in Figure 9. The rest is the same as in case 7.

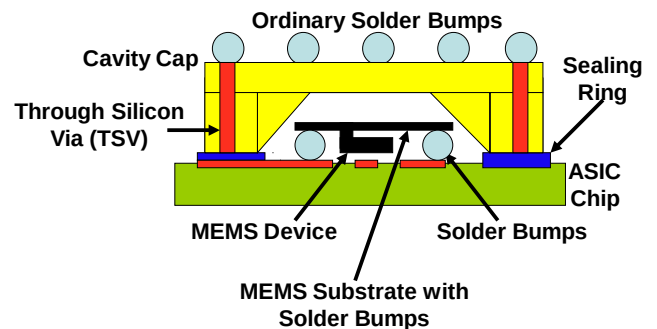
**Case 9:** The solder-bumped MEMS device is first attached to the ASIC as shown in Figure 10. The rest is the same as in case 7.



**Figure 8** MEMS device wire bonded on an ASIC (electrical feed-through TSV is in the package cap)

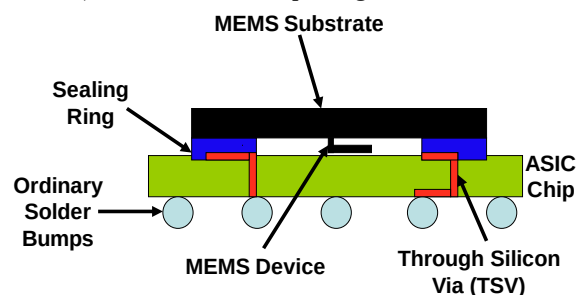


**Figure 9** TSV MEMS device solder bonded on an ASIC (electrical feed-through TSV is in the cap)



**Figure 10** Solder bonded MEMS device flip-chip on an ASIC (electrical feed-through TSV is in the cap)

**Case 10:** The MEMS device is attached to the solder bumped TSV ASIC with a sealing ring, as shown in Figure 11. Then the whole 3D stack is attached (solder reflowed) to a substrate in a package or on a PCB.



**Figure 11** MEMS device is bonded (with a sealing ring) on an ASIC with electrical feed-through TSV

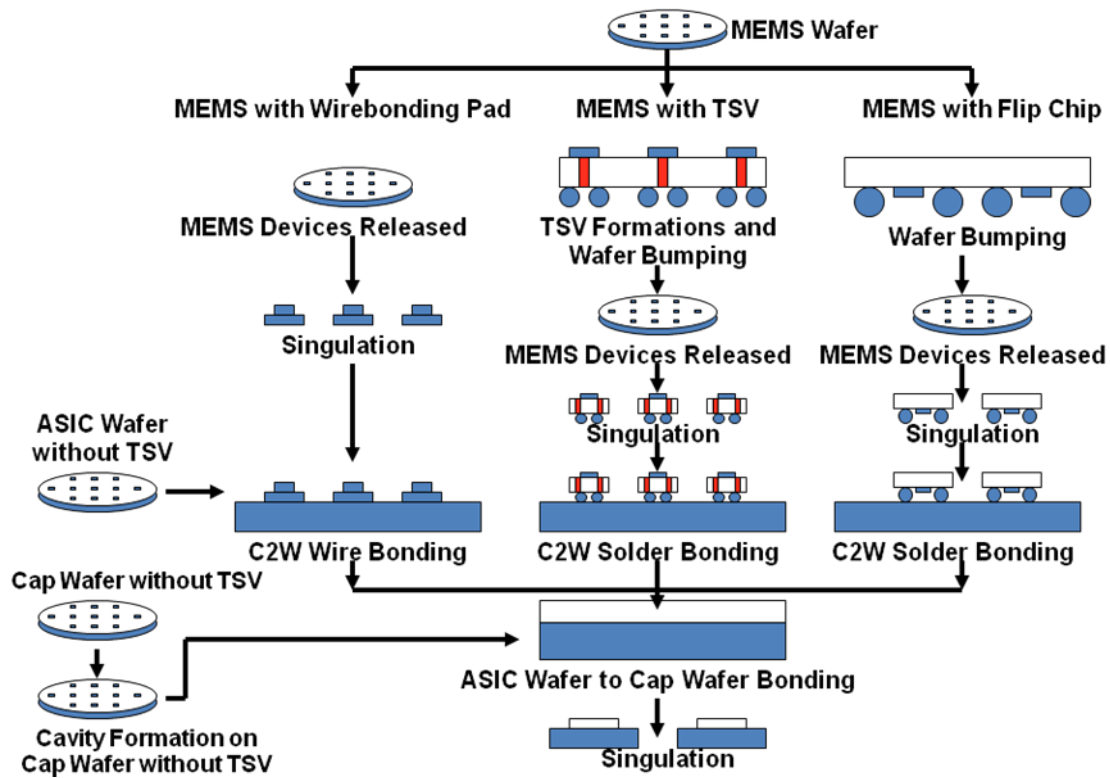


Figure 12 Assembly process for 3D MEMS packaging with lateral electrical feed-through

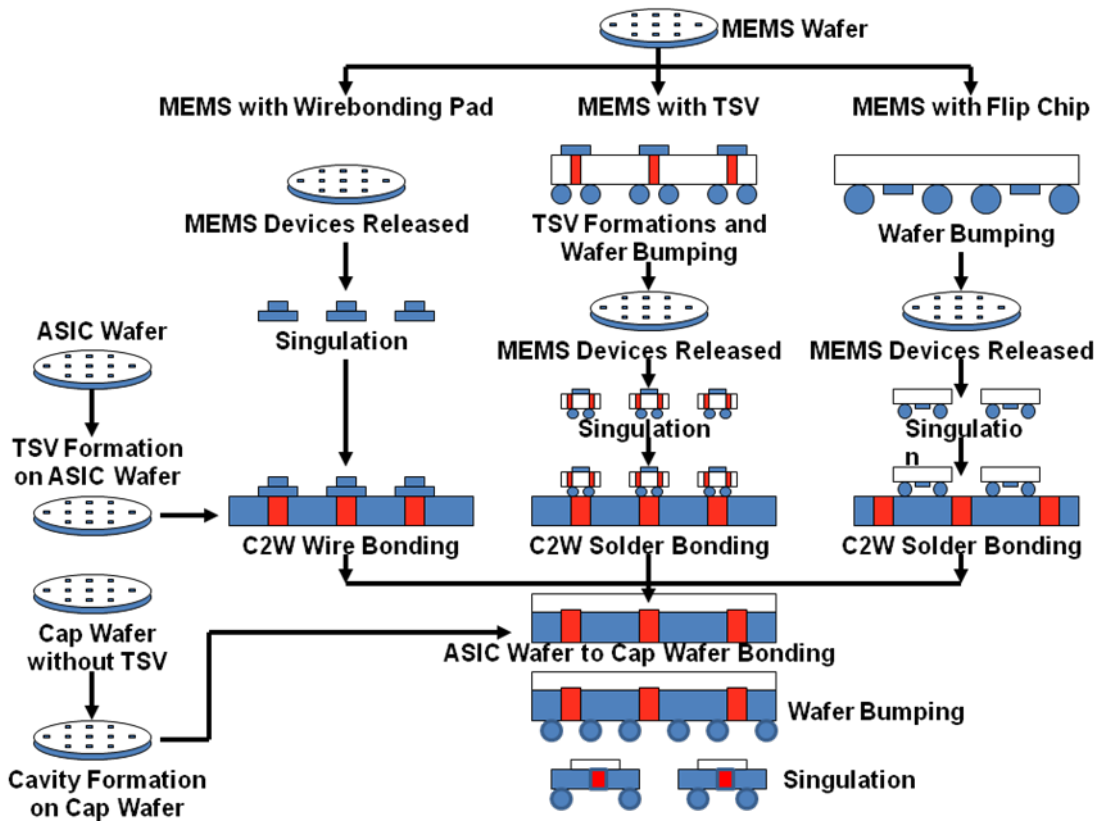


Figure 13 Assembly process for 3D MEMS packaging with vertical electrical feed-through the TSV ASIC

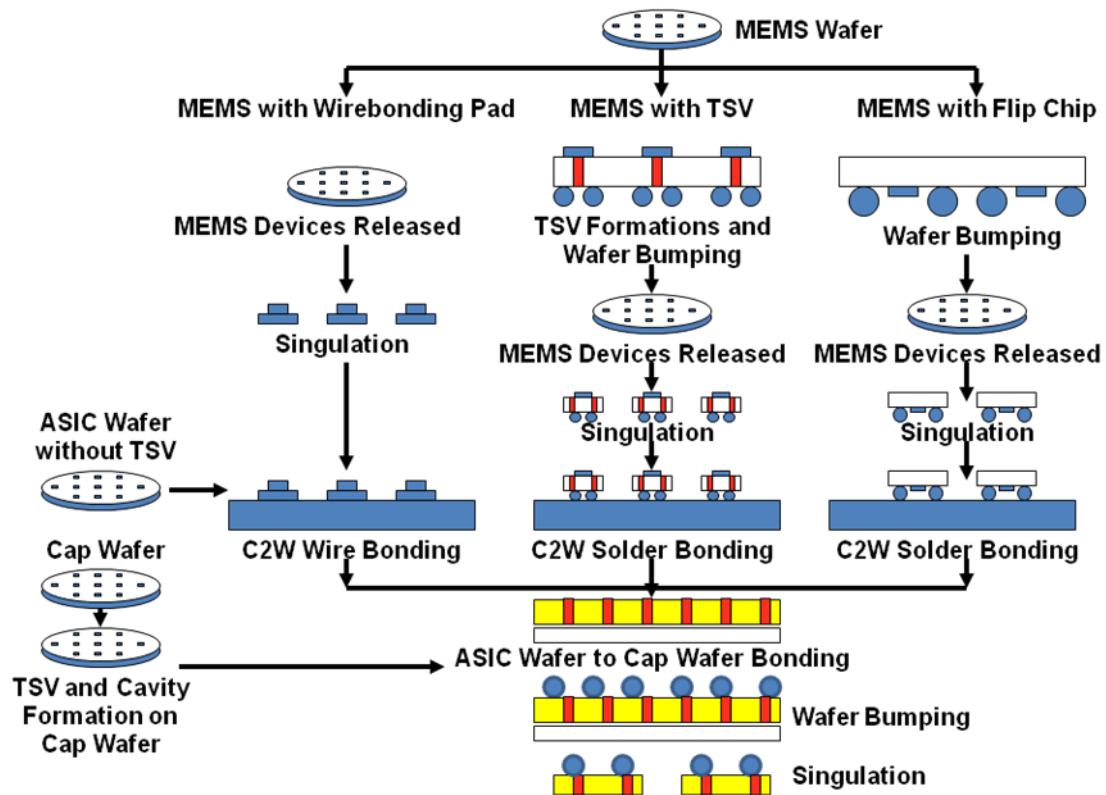


Figure 14 Assembly process for 3D MEMS packaging with vertical electrical feed-through the TSV cap

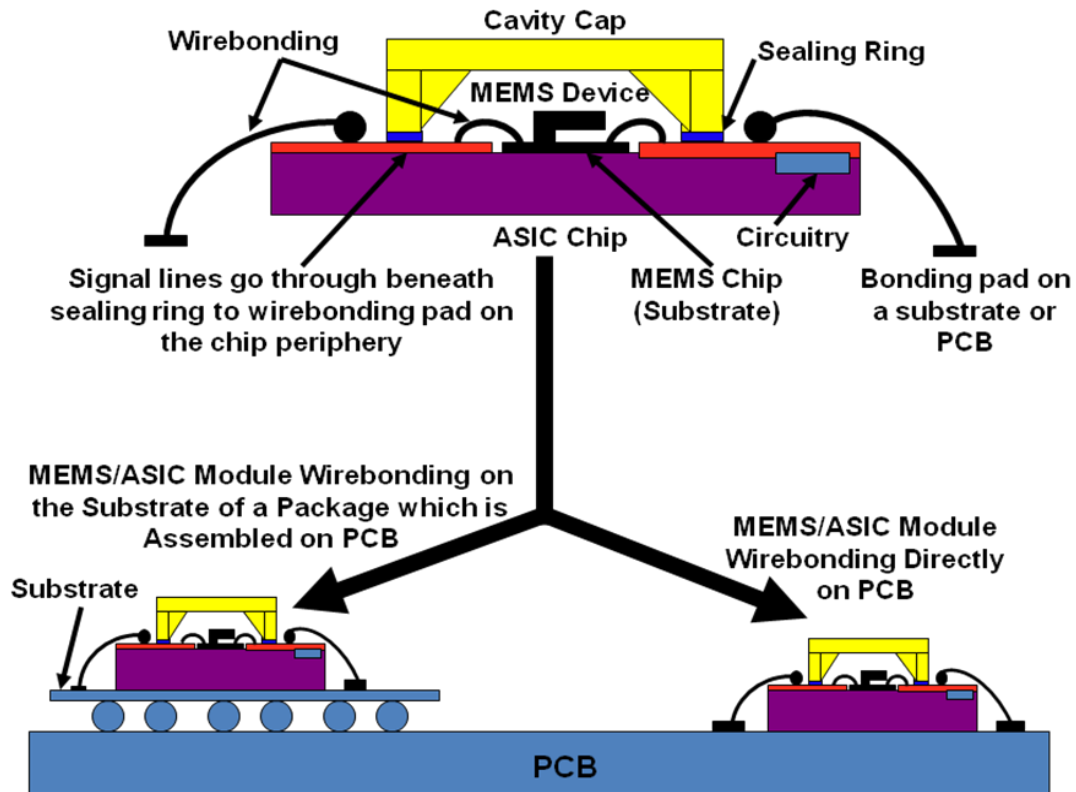


Figure 15 3D MEMS packaging with lateral electrical feed-through (encapsulants are recommended)

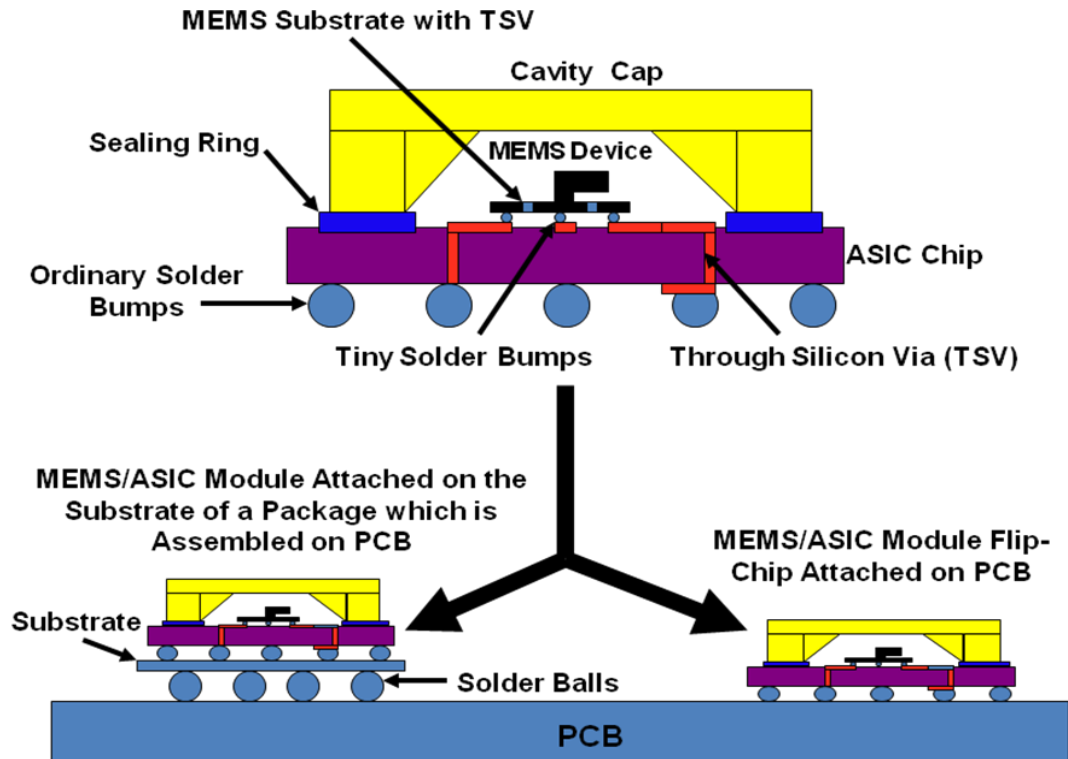


Figure 16 3D MEMS packaging with vertical electrical feed-through in TSV ASIC (underfills are recommended for the solder bumps)

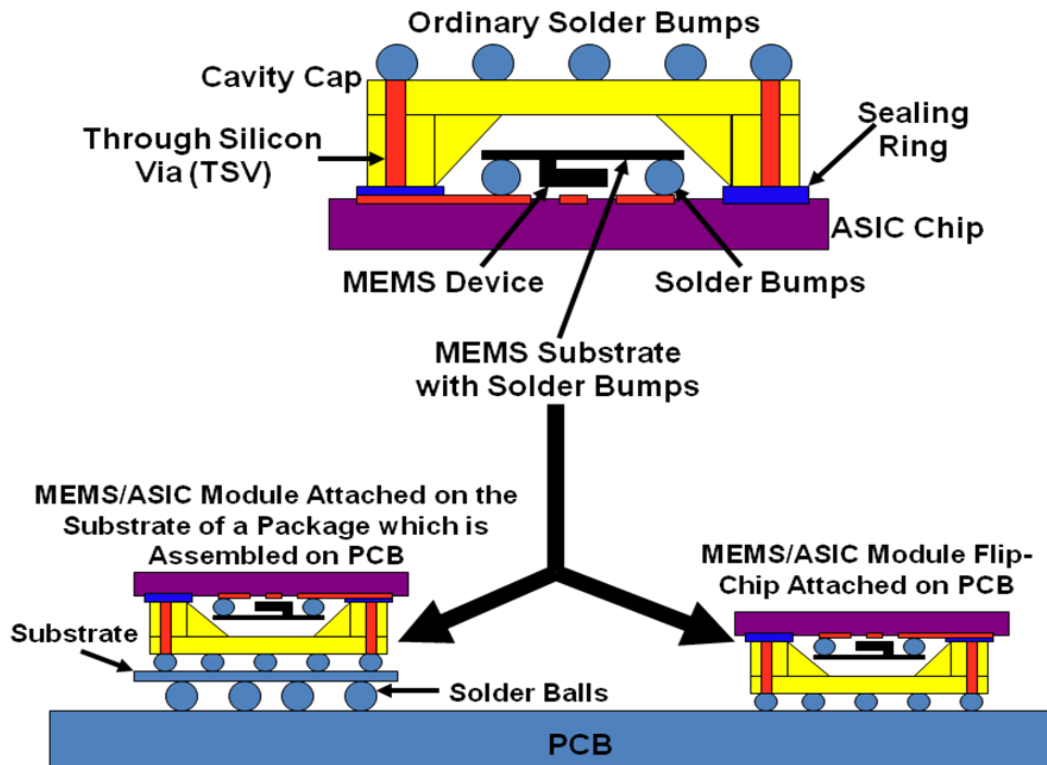


Figure 17 3D MEMS packaging with vertical electrical feed-through TSV cap (underfills are recommended for the solder bumps)

### Assembly Process of 3D MEMS Packaging

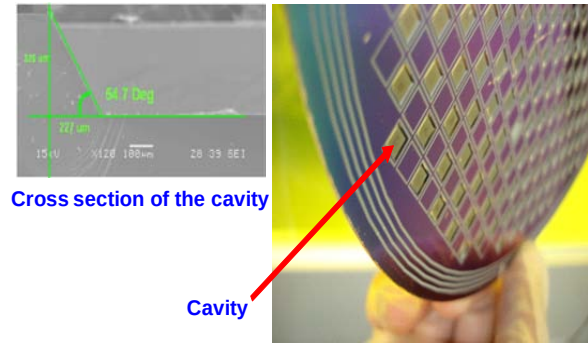
There are many different processes to assemble these 10 MEMS SiPs. For example, the assembly process shown in Figure 12 can be applied to cases 1 through 3; Figure 13, to cases 4 to 6; and Figure 14, to cases 7 to 9. Case 10 will be discussed later. As mentioned earlier, the MEMS wafer can be fabricated either with wire-bonding pads or TSV and solder bumps or a solder-bumped flip-chip, as shown in Figures 12 through 14. These are followed by releasing (etching) the MEMS wafer and singulation. MEMS wafer to ASIC wafer bonding is not recommended because of chip yields and size differences.

For 3D MEMS packaging with lateral electrical feed-through (cases 1, 2, and 3), there is no TSV in both the ASIC and cap wafers (see Figure 12). In these cases, cavities should be formed in the cap wafer by either KOH etching (Figure 18) or use of a laser (Figure 19). Then one performs the bonding of the MEMS device (chip) to the ASIC wafer (C2W). This will be followed by bonding of the cavity-cap wafer to the ASIC wafer (W2W). Finally, the bonded wafers are singulated into individual units, which are ready to be wire bonded on the substrate of a package or on a PCB, as shown in Figure 15. For both cases, encapsulant is recommended.

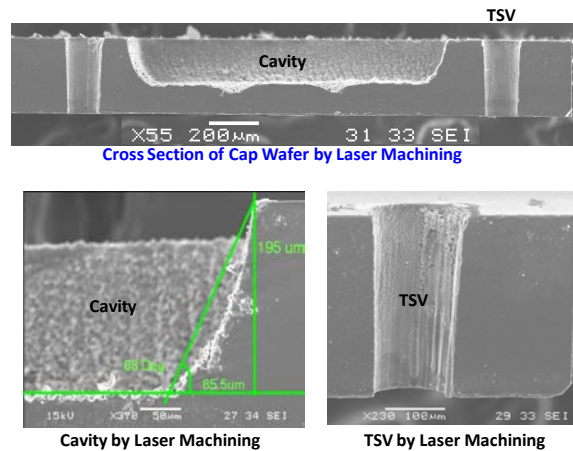
For 3D MEMS packaging with vertical electrical feed-through in the ASIC (cases 4, 5, and 6), the TSV must be fabricated on the ASIC wafer before the MEMS chip to ASIC wafer (C2W) bonding, as shown in Figure 13. After the W2W (cap-to-ASIC) bonding, wafer bumping should be performed on the bottom side of the ASIC wafer. After singulations, the individual units can be soldered on either the substrate of a package or a PCB, as shown in Figure 16. For the PCB case, underfill is necessary for the reliability of the solder joints. For the solder-bumped flip-chip in-package case, use of underfill depends on the substrate material. If it is made of ceramic, then underfill is optional. However, if it is an organic substrate, then underfill is a must.

For 3D MEMS packaging with vertical electrical feed-through in the package cap (cases 7, 8, and 9), the TSV and cavity must be fabricated on the cap wafer before W2W bonding, as shown in Figure 14. After C2W bonding and W2W bonding, wafer bumping should be performed on the bottom side of the cap wafer. The rest is the same as in cases 4 through 6, and Figure 17 shows an example of the complete 3D MEMS packaging with vertical electrical feed-through in the package cap.

As mentioned earlier there are many ways to assemble the 3D MEMS packages. Another way is to attach the MEMS device to the cap wafer first and then perform the cap wafer to ASIC wafer bonding. In this case, however the alignment accuracy requirements



**Figure 18 MEMS cap wafer with cavities fabricated by KOH wet etching**



**Figure 19 MEMS cap wafer with cavity and TSV fabricated by laser machining**

for wafer to wafer bonding are tougher.

### Low-Temperature Bonding with Solders

Most current C2W and W2W bonding methods use temperatures higher than 300°C. During bonding, however, the MEMS devices are already released (there are free-standing microstructures, e.g., membranes, beams, and cantilevers), and low-temperature bonding is desired to reduce damage to the microstructure owing to the thermal-expansion mismatch of the bonding structure (less bow). Fusion (e.g., Cu-to-Cu) bonding at RT works, however the bonding surfaces must be very flat and clean, which do not permit high-volume production. On the other hand, with proper designs of bonding pads and under bump metallurgy (UBM) and selections of solder materials, 180°C or lower bonding temperatures are possible [7, 9-20]. During/after bonding, the solders will be reacted within themselves and the UBM and become an intermetallic compound (IMC) with a melting point much higher than that of the solders.

This feature is welcome by 3D MEMS packaging. For example, after the bonding of a MEMS device with an ASIC wafer with a low melting solder, all the bonding

(solder-interconnect) areas become the IMC with a very high remelting temperature. When a cap wafer is bonded (with a low-temperature solder) to the ASIC wafer (already bonded with the MEMS device), the interconnect between the ASIC and the MEMS devices will not be reflowed. Furthermore, when the whole 3D MEMS package is attached to the PCB with surface-mount technology (SMT) lead-free soldering (260°C), the solder interconnects between the ASIC and MEMS, and cap and ASIC will not be reflowed.

#### **Cavity in Cap Wafer and TSV in MEMS, ASIC, and Cap Wafers**

Figure 18 shows an 8-in cap wafer with cavities fabricated by the KOH (potassium hydroxide) wet etch process and its typical cross section. It can be seen that KOH etch yields a straight wall condition. The cavity can also be made by laser machining and is shown in Figure 19. Even its quality is not as good as that by KOH etching, however, it is adequate for most of applications. The surface conditions of the TSV made by laser machining are very rough and these may affect the electrical performance. Thus, in general, the TSVs for the cap wafer, ASIC wafer, and the MEMS wafer are made by DRIE (deep reactive-ion etching) process [30-32].

#### **A Note on Case 10: 3D MEMS Packaging**

In the food chain of electronic products, packaging is a downstream process (i.e., the packaging people cannot be or are not in a proactive position and cannot say too much), and the packaging people just package whatever is given them by the semiconductor people (i.e., our job starts from the wafers). Case 10 (see Fig. 11) is a very low-cost, high-performance 3D MEMS package. However, in order to make it, the MEMS device (chip) must be much larger (to make space for the sealing ring) than that packages in cases 1 through 9 with a cavity cap. Thus, from a semiconductor points of view, this is a very “bad idea” because many fewer MEMS devices can be produced on the same size MEMS wafer.

#### **Summary and Recommendations**

By integrating the MEMS device from the MEMS wafer (with either wirebonding pads, or solder-bumped TSV substrate, or solder-bumped flip chip without TSV), the ASIC chip from the ASIC wafer (with either TSV or without), and the cavity cap from the cap wafer (with either TSV or without) 10 different 3D packages have been presented. Their assembly processes have also been provided. Some important results and recommendations are summarized in the following.

- (1) The footprints of all these 10 3D MEMS packages are smaller than that of the corresponding 2D conventional (separate) packages.
- (2) The electrical performances of all these 10 3D MEMS packages are better than that of the

corresponding 2D conventional (separate) packages.

- (3) The costs of all these 10 3D MEMS packages are lower than that of the corresponding 2D conventional (separate) packages.
- (4) The footprints of all the vertical electrical feed-through 3D MEMS packages (Cases 4 through 10) are smaller than that of the lateral electrical feed-through 3D MEMS packages (Cases 1 through 3).
- (5) The electrical performances of all the vertical electrical feed-through 3D MEMS packages (Cases 4 through 10) are better than that of the lateral electrical feed-through 3D MEMS packages (Cases 1 through 3).
- (6) C2W bonding is recommended for the MEMS device bonding to the ASIC wafer.
- (7) W2W bonding is recommended for the cap wafer bonding to the ASIC wafer with the MEMS devices already attached.
- (8) For both C2W bonding and W2W bonding, low-temperature bonding methods with solders are recommended.

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