

Electromigration and Annealing Kinetics of Cu pillar

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Abstract

Cu pillar bump was annealed or current stressed at various current densities. Based on the results of electromigration life time test, the resistance to electromigration of Cu pillar bump was much better than conventional solder bump. Also, intermetallic compounds (IMCs) growth behaviors were investigated by in-situ scanning electron microscopy (SEM) observation. Only Cu_6Sn_5 was observed in the Cu pillar/Sn interface after reflow. However, Cu_3Sn formed and grew at Cu pillar/ Cu_6Sn_5 interface with increasing annealing and stressing time. The growth kinetics of total ($\text{Cu}_6\text{Sn}_5 + \text{Cu}_3\text{Sn}$) IMC changed when all Sn phases in Cu pillar bump were exhausted. The complete consumption time of Sn phase in electromigration condition was faster than that in annealing condition. Kirkendall voids, which would be detrimental to the reliability of Cu pillar bump, were observed at both $\text{Cu}_3\text{Sn}/\text{Cu}$ pillar and $\text{Cu}_3\text{Sn}/\text{Cu}$ under bump metallization interfaces.

Key words: Cu pillar bump, electromigration, intermetallic compound, Kirkendall voids

1. Introduction

Flip-chip packaging technology has been widely used in the electronics industry in recent years as high performance and miniaturized electronics have become more common [1]. This technology assists in the achievement of high performance and miniaturization because the chip and the substrate are directly connected to solder bumps. The solder bumps become spherical to minimize the surface energy [2]. Bump bridging is caused by the shape of solder in miniaturized electronics. It is limited to applications with a fine pitch below $100\mu\text{m}$. Therefore, a new shape for the bump structure is necessary to address this limitation.

A Cu pillar with a solder cap structure where bump bridging does not occur due to the small amount of solder used compared with conventional solder bumps was developed as a fine pitch flip-chip packaging alternative [3]. Electrical reliability issues can also be solved with this structure because Cu pillars have superior electric conductivity.

However, brittle Cu-Sn IMCs form at the joints in Cu pillar bumps because Cu atoms react to the Sn

atoms in the solder. Additionally, the high concentration of Sn in Pb-free solder induces more excessive growth of IMC than eutectic SnPb solder [4]. Extensive IMC growth and Kirkendall void formation, which results from the difference in the intrinsic diffusivities of Cu and Sn, in solder joints severely deteriorate the mechanical strength of the joints [5]. The mechanical reliability of solder joints is sensitive to the solder reaction and the microstructure of the solder [6]. Therefore, to ensure the reliability of solder joints, an understanding of the IMC growth between Cu and solder is necessary. Many researchers have studied IMC formation and the growth between Cu and solder in solder bumps and thin film structures [7]; however, there have been few studies regarding the microstructural evolution and growth of IMCs in Cu pillar bump structures. Moreover, under electric current stressing, the IMC growth is accelerated by the influence of by the electron wind force [8-10]. Because the current density of Cu pillar is high due to its small size, it is important to understand this behavior.

In this paper, the IMCs growth behaviors in Cu pillar bumps during simple annealing and under

various current stress conditions were studied systematically using in-situ SEM observations. By using in-situ method, we could observe IMCs growth behaviors in Cu pillar bumps more accurately than conventional ex-situ method which observes a few samples after test.

2. Experimental Procedure

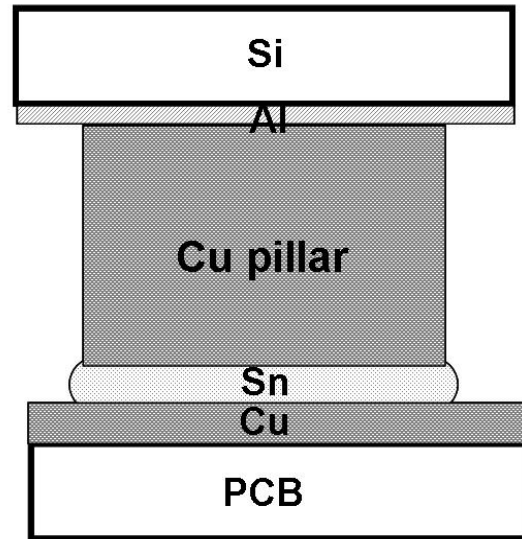
Figure 1 shows a schematic diagram and SEM image of the Cu pillar bump structure. The pad on the Si chip was electroplated with a 2 μ m thick Al film, and Cu pillars and pure Sn formed to thicknesses of 40 μ m and 3 μ m, respectively, on the Al pad through an electroplating process. The pad on the printed circuit board (PCB) was made using an electroplated 20 μ m thick Cu layer and an electroplated 3 μ m thick pure Sn.

The height and diameter of the Cu pillar bump were 65 and 80 μ m, respectively. Pure Sn solder at both the chip and substrate was directly interconnected during the bonding process. The bonding was followed by a reflow process with the peak reflow temperature fixed at 280°C. The bonding time and load were 7sec and 35 N, respectively. Just after bonding, all samples have similar Sn thicknesses between 5 to 6 μ m. The samples were cross-sectioned with sand paper after the reflow.

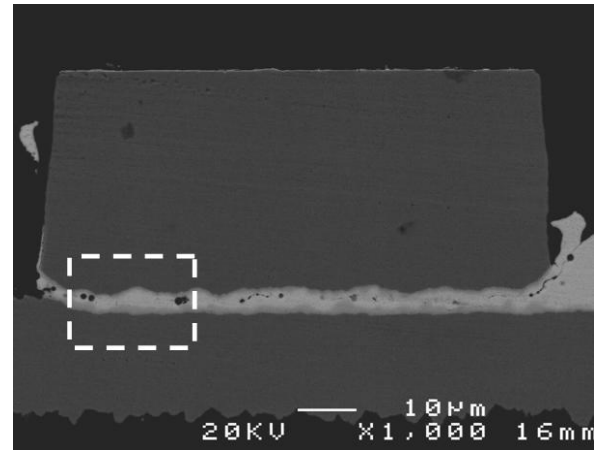
To investigate the interfacial microstructure evolution and IMC growth in Cu pillar bumps, in-situ annealing tests were performed via SEM on three samples at temperatures of 120, 150, and 180°C. The applied current densities for the annealing under current stress condition were 3.5×10^4 , 5.0×10^4 , and 7.2×10^4 A/cm². The temperature of the sample was kept at 150°C by attaching thermo-couple on Si chip. IMC growth during annealing was observed at every 20 hours. IMC growths at applying various current densities were observed by in-situ as well.

The evolution of each interfacial microstructure and the IMC growth of Cu pillar bumps were analyzed using SEM in the back-scattered electron (BSE) mode and energy dispersive x-ray spectroscopy (EDS). IMC thickness includes the IMC layers at both the chip side and substrate side. The Cu-Sn IMCs thickness was quantified with an image analyzer. The Cu-Sn IMCs thickness was defined by dividing the area of the IMC by the interface length.

The Kirkendall void area was quantified by the measurement of the total occupied area of all voids at SEM image with an image analyzer. The changes in IMC thicknesses between the samples were used to evaluate the activation energy for IMC growth.



(a)



(b)

Figure 1. (a) Schematic diagram and (b) SEM image of Cu pillar/Sn bump structure

3. Results and Discussion

A. IMC growth during annealing

To observe the evolution of the interfacial microstructure and the growth of Cu-Sn IMCs on Cu pillar bumps with annealing temperature and time, BSE images were taken of cross-sectioned Cu pillar bumps annealed at 150°C, as shown in Figure 2. The SEM and EDS results suggest that only Cu_6Sn_5 was observed at the Cu pillar/Sn interfaces, and microvoids exist in the Sn phase after reflow. The microvoids seem to originate from the flip-chip bonding process, and they arise from the defects in the samples. Cu_3Sn formed and grew at the Cu pillar/ Cu_6Sn_5 interface with increasing annealing time. It has been reported that the Cu_6Sn_5 and Cu_3Sn phases are generally formed at the Cu/Sn interface during the reaction between Cu and Sn [7,11]. Cu_3Sn layers on both interfaces have grown up with the similar thicknesses.

The Sn phase was not observed at the Cu pillar/Sn interface after 300 h at 150 and 60 h at 180°C, while the Sn phase was observed at the Cu pillar/Sn interface after 300 h at 120°C. It appears that the reaction velocity between Cu and Sn was faster at higher annealing temperatures.

Figure 3 shows the thickness of the total IMCs as a function of the square root of the annealing time at 150°C. The growth of the total IMC followed a linear relationship with the square root of the annealing time and was faster at higher annealing temperatures. This implies that the growth of the total IMC was controlled by a diffusion mechanism.

To understand the variation of total IMC growth slopes at 150 and 180°C, the IMC thicknesses of the Cu_6Sn_5 and Cu_3Sn phases as a function of the square root of the annealing time at 120, 150, and 180°C. The IMC growth of the Cu_6Sn_5 and Cu_3Sn phases at 120°C followed linear relationships with the square root of the annealing time until 300 h. The Cu_6Sn_5 and Cu_3Sn phases linearly increased together before 240 h at 150°C and 60 h at 180°C, and then the Cu_6Sn_5 phase rapidly decreased after 240 h at 150°C and 60 h at 180°C.

The Cu_3Sn growth rate was also faster than the Cu_6Sn_5 growth rate compared with the Cu-Sn reaction system of a conventional solder bump structure, which is a Cu-limited system.

This seems to arise from the Cu pillar bump structure, which is a Sn-limited system.

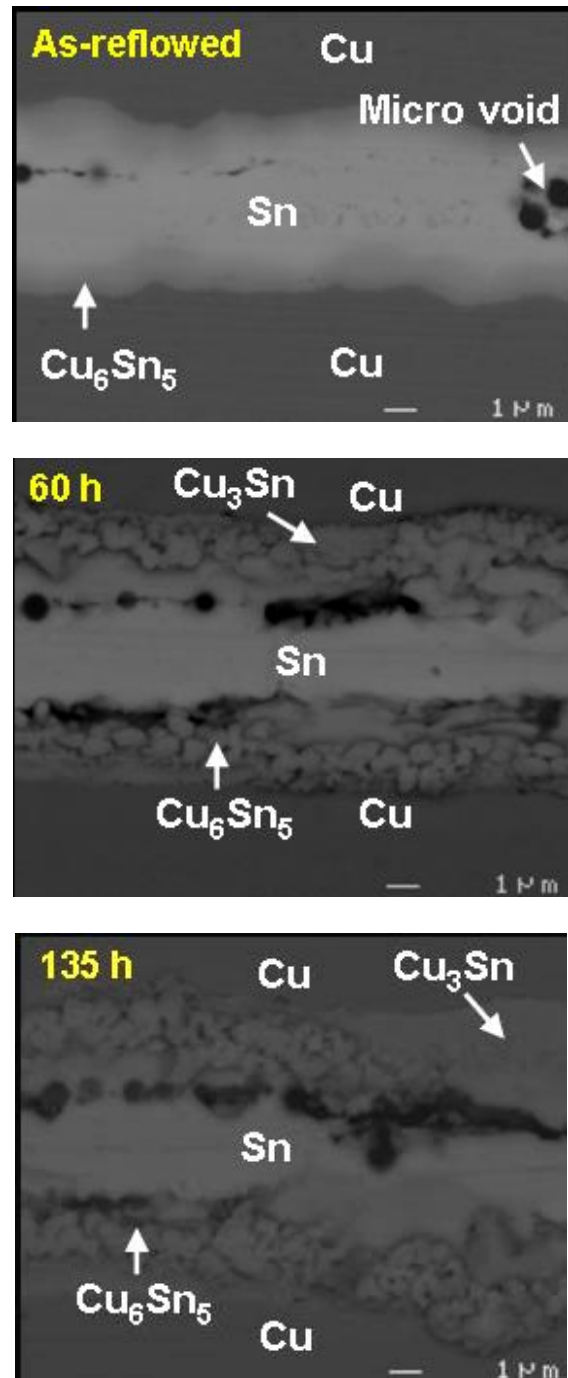


Figure 2. BSE micrographs of the enlarged cross-sectioned Cu pillar/Sn bump during annealing at 150°C

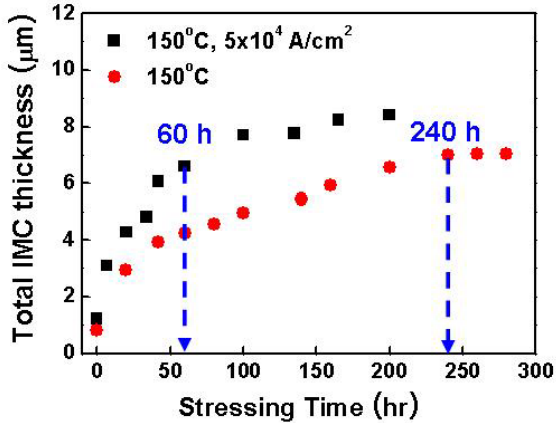


Figure 3. Total intermetallic compound layer thickness with annealing time and stressing time; 150°C and 150°C, 5×10^4 A/cm²

B. Kirkendall void growth during annealing

Kirkendall voids were observed at the Cu pillar/Cu₃Sn interface as well as within the Cu₃Sn layer at 150 and 180°C, while Kirkendall voids were not observed at the Cu pillar/Cu₃Sn interface at 120°C. It appears that the reaction velocity between Cu and Sn was faster at higher annealing temperatures.

To investigate the correlation between the Kirkendall void area and the Cu₃Sn thickness, the Kirkendall void area and Cu₃Sn thickness as a function of the square root of the annealing time at 180°C are shown in Figure 4. The Kirkendall void area also linearly increased as the Cu₃Sn IMC thickness linearly increased with annealing time.

The Cu₃Sn IMC thickness was thicker than the Cu₆Sn₅ IMC thickness with increasing annealing time due to the Cu pillar bump structure, which is a Sn-limited system. Several researchers reported that the formation of Cu₃Sn and Kirkendall voids at solder joints affect the mechanical strength [5]. Therefore, the formation of Cu₃Sn and Kirkendall voids in the Cu pillar bump structure affects the mechanical reliability. The correlation between the formation of Cu₃Sn and Kirkendall voids and the mechanical reliability in the Cu pillar bump structure should be clarified in future work.

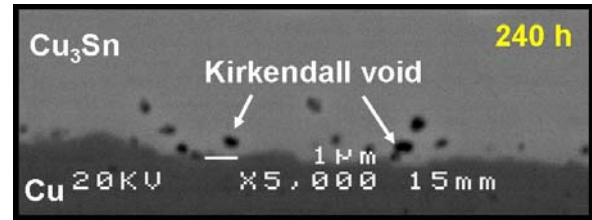


Figure 4. BSE micrographs of the Kirkendall void inside Cu₃Sn layer for annealing at 180°C

C. IMC growth during electric current stressing

IMC thickness changes applying current densities of 3.5×10^4 , 5.0×10^4 , and 7.2×10^4 A/cm². Figure 3 shows the thicknesses of total IMC, Cu₆Sn₅, and Cu₃Sn increased linearly proportional to square root of stressing time. It has been reported that IMC thickness in the conventional solder bump under current stressing condition is linearly proportional to the stressing time [8-10].

This indicates that the local joule heating is more predominant factor affecting IMCs growths than electron wind force in Cu pillar bump. Indeed, large joule heating was observed in life time test. Therefore, local joule heating is more serious than expected in Cu pillar bump.

Also, the polarity effect, which was commonly observed in the conventional solder bumps, was not observed during current stressing test. The thicknesses of IMCs at upper part of solder bump and those at lower part of solder bump were almost the same as shown in Fig. 5. Nah et al. reported that there was no polarity effect in Cu pillar bump with SnPb and the temperature effect would be much important [12]. We think that the electron wind force did not affect seriously on the IMCs formations, while the temperature increasing by local joule heating affected on the IMCs formation in Cu pillar bump.

In case of annealing with current stressing, Cu₆Sn₅ thickness decreased after the transition time, and then Cu₃Sn growth rate became larger than Cu₆Sn₅ growth rates similarly to that observed in annealing without current stressing. It was found that the IMCs growth rates increased as applied current density increased.

Since the amount of Sn in Cu pillar bump is limited to $2\mu\text{m}$ in thickness, the transition time becomes shorter as IMC growth rates increased by applying higher current densities. The transition time of IMC growth was 100, 60, and 20 hours when the applying current densities were 3.5×10^4 , 5.0×10^4 , and 7.2×10^4 A/cm², respectively.

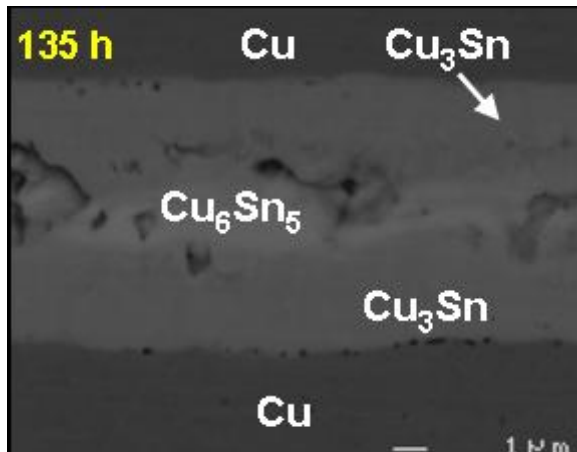
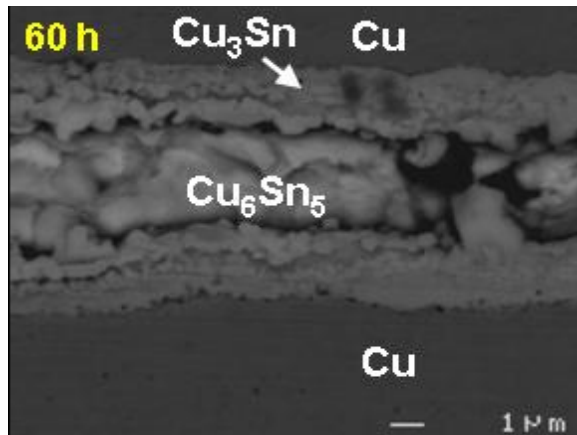
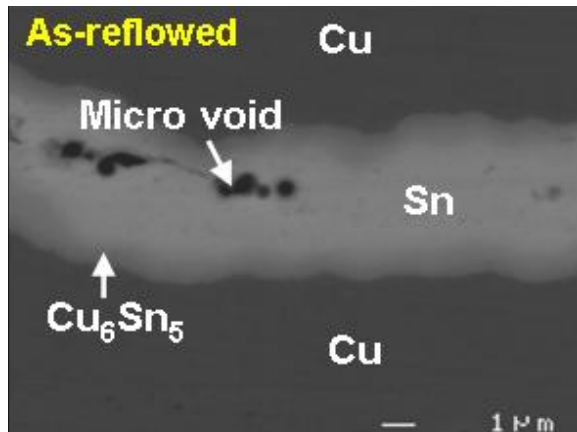


Figure 5. BSE micrographs of the cross-sectioned Cu pillar/Sn bump current stressing of 5.0×10^4 A/cm² at 150°C

Table I. The transition time of IMC growth at annealing and various current densities

Current density (10^4 A/cm ²)	3.5	5.0	7.2
Transition time of IMC (h)	100	60	20

Table I shows the transition times of IMCs growths with respect to the applied current density, showing that the transition times of IMCs growths were inverse proportional to current density. This relationship can be expressed by power law:

$$t = kj^{-n} \quad (1)$$

where t is the transition time, k is a constant, j is a current density, and n is an exponent. According to the log-log plot result, the exponent n was estimated to be 2.23. The transition times of IMC growths were enhanced by the effect of joule heating and current density. It is very important to know or predict exact transition time of Cu pillar under current stressing condition because the mechanical reliability after the transition time would decrease abruptly. If the amount of Sn in Cu pillar bump is changed, the transition time would be changed also. In this work, we firstly measured the transition time of Cu pillar as a function of current density.

4. Conclusions

The IMCs growths behaviors in Cu pillar bump during annealing with/without current stressing were studied by in-situ SEM observation method. Results revealed that the thicknesses of IMCs during annealing without current stressing were proportional to square root of time.

Also, IMCs growths under current stressing were proportional to square root of time due to the localized joule heating. It was observed that Cu_3Sn growth rate was larger than that of Cu_6Sn_5 , which is opposite result observed in conventional solder bump. After the complete Sn exhaustion in the bump,

Cu_6Sn_5 thickness became to decrease and Cu_3Sn grew faster.

The Kirkendall void area also linearly increased as the Cu_3Sn IMC thickness linearly increased with annealing time. When current applied in Cu pillar bump, IMC grew faster than annealing condition, and the transition time of IMC growth was shortened, and the transition time showed inverse proportional to current density.

Acknowledgments

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