

An Interconnection Verification Method and a New Substrate Option for Cu Pillar Flip-chip Module Applications

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Abstract

Cu pillar flip-chip technology has been in development and production for several years. It has clear advantages over solder flip chip. These advantages include fine pitch capability, flexible bump shape, and short thermal/electrical path. Challenges in the assembly process are also well known. This paper introduces an easy and effective test method to verify the interconnection quality between Cu pillar flip chip and substrates for a volume production environment. Qualification lots using this process were built and passed a full range of reliability tests. The reliability of the Cu pillar flip-chip modules that were assembled on Au surface finish substrates was also evaluated. The study shows the feasibility of a low cost option to assemble flip chip and wire bond die on the same substrate.

Key Words: Cu pillar, flip-chip, reliability, low cost.

Introduction

Cu pillar flip chip offers some distinct advantages [1] over solder flip chip. The following are a few of the assembly related benefits.

- Controlled collapse of the bumps leads to predictable interconnect impedance and hence more stable product performance
- The low solder volume allows for elimination of the solder mask for fine pitch interconnection.
- The solder cap makes it compatible as a drop-in replacement for solder bump flip chip package with 180 μ m pad pitch.

A typical assembly process flow for solder flip-chip in an over-molded package is described in table 1.

Table 1: Typical flip-chip module process flow

1	Wafer backgrinding & dicing
2	SMD mount
3	FC chip attach on laminate
4	Reflow & flux wash
5	Pre molding bake, plasma
6	Molding
7	Post molding bake
8	Marking, dicing & pick to tray

In this study, Cu pillar flip chip modules were assembled using a standard solder flip chip process for a RF component application. Figure 1

shows the outline of the Cu pillar flip-chip die. The corresponding laminate design is shown in figure 2. To ensure a reliable joint, the laminate trace must be protected from contaminants. In this application, the copper trace is protected with an organic solderability protectant (OSP). As an alternative to dispensed underfill, a special mold compound is utilized to provide support to the flip chip device. To maximize the open volume under the die, the soldermask is removed. Since there is enough room around the center bump, the soldermask is removed. This allows designing to a solder-mask-defined (SMD) pad like those used in typical solder bump applications.

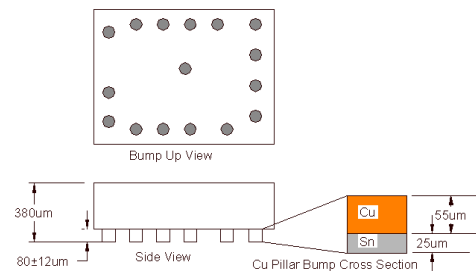


Figure 1: Cu pillar Flip chip die

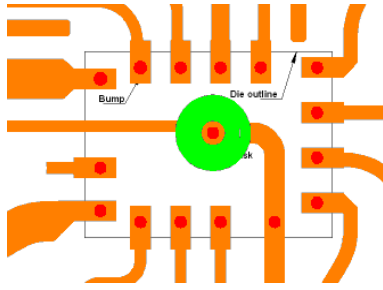


Figure 2: Substrate design

Assembly Verification Procedure

To determine the interconnection bonding quality between the flip chip die and the substrate, JEDEC standard No. 22-B109A specifies a die pull test. The die pull test requires a stud to be attached to the backside of the flip chip die and a fixture to hold the substrate during the pull test. These test setups make the pull test less practical as an in-line verification method in volume production, especially for small size RF flip chip die applications.

In this study, it is demonstrated that a die shear test, sketched in figure 3 is an effective method to verify the interconnection bonding. The tool is set to shear the die at one third the die thickness. This ensures that the tool clears features on the substrate and distributes the force to the bumps. The test is able to correlate both die shear strength and failure mode to solder joint quality.

The die shearing was performed on a Dage 4000 bondtester, after the flip-chip die are attached and reflowed onto the laminate substrate. Figure 4 illustrates the three die shear failure modes by looking at substrate pads. Mode “A” is an ideal failure mode. Shear failure occurs within bulk of solder with a consistent wetting area. It provides a consistent and predictable solder standoff. In mode “B”, the solder wicks down to the sidewalls and along the substrate trace due to excessive flux. Although the bonding strength is as strong as mode “A”, the long term joint strength will be diminished during reliability testing due to a lower solder standoff and an increase in intermetallic compounds (IMC). In failure mode “C”, the flux is not sufficient; the solder on the bump is not transferred to the trace and causes non-wetting. Failure mode “C” corresponds to low die shear values.

This is an easy test procedure which can be used as an in-line monitoring method to ensure a consistent bonding quality between Cu pillar flip-chip and substrate

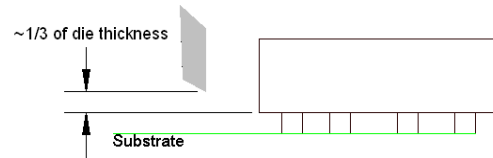
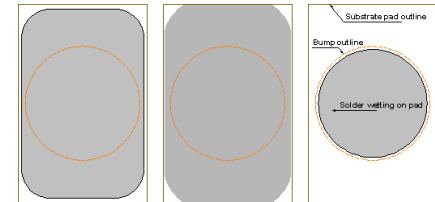


Figure 3: Schematic of die shear after reflow



Shear mode	A	B	C
Shear strength*	1	1	0.8

*: The value of shear strength is an average of about 450 samples and was normalized for easier comparison

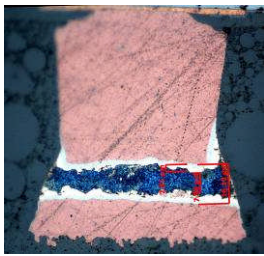
Figure 4: Correlation between die shear strength and failure mode to solder joint quality

Reliability result

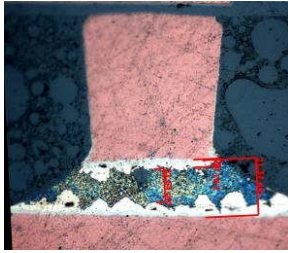
After this assembly verification test method was defined, the assembly process parameters were modified to produce type “A” joints. Three qualification lots were built and submitted to reliability testing. All parts passed the test successfully. Table 2 gives an overview of the reliability test with condition and sample size. X-sectioning (see Figure 5) was performed on the virgin parts and stressed parts to compare and verify the integrity of bump and solder joints. Sn/Cu IMC growth was observed on post high temperature storage (HTS) parts as expected.

Table 2: Reliability

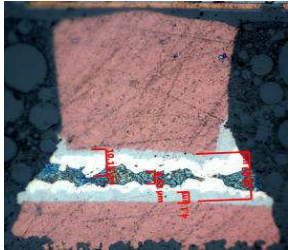
Rel. Test	Standard	Sample Size/lot	Results
High Temperature Storage (1k hrs)	JESD22-A 103	44/3	Passed
MSL 3 (@ 260C)	IPC/JEDEC J-STD-20A	44/3	Passed
TC loose w MSL precondition (1k cycle)	JEDEC 22-A104C	44/3	Passed
THB (1k hrs)	JESD22A101	44/3	Passed
Vibration	JESD22B103	44/3	Passed
DC Monitored TC on board (1K cycle)	JESD22A10	12/3	Passed
DC Monitored Drop Shock	JESD22B111	36/3	Passed



(a) Virgin: ~16μm solder height with ~2μm Cu/Sn IMC



(b) 1k cycle TC: ~19μm solder height



(c) 1k hr HTS: ~8μm Sn/Cu IMC on each side with ~4μm pure Sn remaining in the joint

Figure 5: Cross sections of Cu pillar interconnection on virgin and stress tested bumps

Substrate surface DOE and results

The discussion on the preceding qualification work revolved around substrates using Cu with organic solderability protectant (OSP) on the topside (flip chip attach side) and Au finish on the bottom side. Au finish I/O pads on the bottom are needed to create a stable contact between the pads and electrical test probing. These dual surface finishes do not result in the most cost effective solution. Substrates with Au surface finish on both sides are available in industry for standard solder flip chip. However the concern of adopting such finishes with Cu pillar flip chip is Au embrittlement due to low solder volume and IMC's.

Generally, gold embrittlement occurs in solder when the Au concentration in the solder is in the range from 2~7wt%. Some reports showed the tendency of Au embrittlement increases when the Au concentration is only about 0.3 wt% in Pb-Sn solders.[2] The concentration of gold in solder can be calculated using the following equations:

$$wt\%Au = \frac{wtAu}{wtAu + wtSn} \times 100$$

$$wt\%Au = \frac{V\rho_{Au}}{V\rho_{Au} + V\rho_{Sn}} \times 100$$

V is volume and ρ is density of the material.

$$\rho_{Au} = 19.3g / cc; \rho_{Sn} = 7.3g / cc$$

At the time of writing this paper, no reliability study has been published for Pb-free Cu

pillar flip on Au pads in an over-molded package. To gather the data and prove the hypothesis, a design of experiments (DOE) was set-up to study the reliability of Cu pillar flip chip on Au surface finish substrates. Three lots of substrates with gold thicknesses of 0.02, 0.05 and 0.08μm, were manufactured. Au wt% calculations in each substrate case listed in table 3. The wt% ranges is calculated considering the manufacturing variations from substrate trace and solder height on the bump.

Table 3: Au wt% range vs. substrate Au thickness

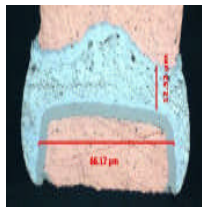
L o t	Au thickness (μm)	Min Au wt% (Max bump solder on a min trace)	Max Au wt% (Min bump solder on a max trace)
1	0.02	0.4%	0.8%
2	0.05	1.1%	2.1%
3	0.08	1.9%	4.4%

Using the laminates, samples were assembled and submitted to reliability tests. Table 4 gives a summary of the reliability test results.

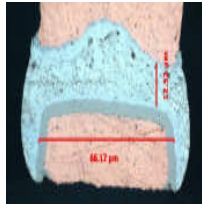
Table 4: Substrate Au thickness DOE reliability results

L o t	Au Thickn ess (μm)	1k hr HTS (22 samples/lot)	Vibration (22 samples/lot)	MSL3 + 1k Temp cycle (50 samples/lot)
1	0.02	Passed	Passed	Passed
2	0.05	Passed	Passed	Passed
3	0.08	Passed	Passed	Passed

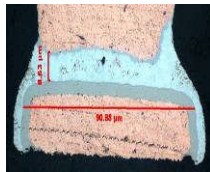
All samples passed the battery of reliability stress tests. Cross sectioning was performed on post HTS parts to exam IMC growth and verify the solder joint integrity (see Figure 6 for the cross sectioning pictures). No samples revealed any structural failure. This successful experiment enables the possibility to use a low cost Au surface finish substrate for Cu pillar flip chip module applications. Since Au surface finish is commonly used for wire bond die assembly, this also opens the possibility of flip chip and wire bond assembly within the same substrate.



(a) Au thickness: 0.02 μ m. No cracking observed after 1h HTS test



(b) Au thickness: 0.05 μ m. No cracking observed after 1h HTS test



(c) Au thickness: 0.08 μ m. No cracking observed in a relatively thin joint layer

Figure 6: Cross sections of Cu pillar interconnection on 3 Au surface finish substrates

In order to understand the IMC's effect to reliability associated with Au concentration, TC tests are continuing past 1000 cycles and post HTS parts were submitted to additional TC stress test. The temperature cycling tests will continue until failure.

Conclusion

The following conclusions are drawn from the experiments:

- Die shear tests can be an easy and cost effective alternative to die pull tests. This test can quickly and reliably verify the solder joint quality.
- Cu pillar flip chip can use the same manufacturing process as solder flip chip. This study shows that it is a reliable process.
- Au and OSP surface finishes are reliable options for Cu pillar flip chip modules

Acknowledgments:

Many thanks to all the staff for the great support of this work. Special thanks go to Jeppe Bendixen who designed RF flip chip module, Marwan Naim who built all modules and Randy Love who conducted failure analyses.

References:

- [1]:Bend Ebersberger, Charles Lee," Cu pillar Pumps as a Lead-Free Drop-in Replacement for Solder-Bumped, Flip-Chip Interconnects", 2008 Electronic Components and Technology Conferences, pp58- 66
- [2]:Xingjia Huang, S.W.Ricky Lee "Gold Embrittlement of Solder Joints in Wafer-Level Chip-Scale Package on Printed Circuit Board With Ni/Au Surface Finish. IEEE Transactions on electronics packaging manufacturing. Vol. 31, No3, July 2008, pp 185-191