

An Investigation of Materials Selection and Manufacturing Process on Resulted Device Alpha Emissivity Levels

Peng Su, Rick Wong, and Shi-Jie Wen

Cisco Systems, Inc.
Component Quality and Engineering
170 W Tasman Drive, San Jose, California 95134
Email: pensu@cisco.com

Andy Tseng, Jimmy Chen, and Simon Li

Advanced Semiconductor Engineering, Inc.
3590 Peterson Way, Santa Clara, CA 95054
Email: Andy.Tseng@aseus.com

Abstract

The continued decrease in Si feature sizes has resulted in significant increase in transistor and embedded SRAM density. In the meantime, this decrease in feature size, along with the the reduction in operating voltages, has also resulted in a reduction in the charge stored for SRAMs and transistors. Both of these changes may result in an unintended increase of SER (Soft Error Rates) in IC devices. One of the major contributing factors for SER is alpha particles emitted from packaging materials, which mostly comes from the decay of Th and U. These elements typically have a concentration of a few parts per billion in materials such as silica fillers and solder alloys. Even at these levels, however, small amount of contamination on the assembly process due to mix-use of equipment or tooling can result in high and unreliability alpha emissivity near the active silicon, resulting in an increase of SER.

In this work, we investigate the effects of key process steps and equipment use on the alpha emissivity levels on flip chip packages. First, blank silicon wafers are processed through major steps of the assembly process. Both a dedicated ULA (Ultra Low Alpha) assembly line and a mix-use line are evaluated. Contacts and handling by equipment and tooling are simulated on these wafers, and after every step, one wafer is taken out of the process for alpha emissivity measurement. Second, actual flip chip components with an ULA package material set are assembled on the same dedicated ULA and mix-use assembly lines. Alpha emissivity levels near the active silicon surface are measured for both groups of components. Alpha emissivity measurements on the blanks wafers and the flip chip components will be reported and compared.

Key words: Ultra Low Alpha, Soft Error Rate, Underfill, Assembly Process

Introduction

Soft errors occur in semiconductors when energetic particles interact and create charges near sensitive nodes. [1] For nodes such as SRAMs, SER (Soft Error Rate) is a function of the charge generated by energetic particles, the charge collection efficiency of the node, and the critical charge of the node. As feature sizes continue to shrink, the charge that can be collected by a node is reduced, but the critical charge is also reduced. The combined effect is an overall increasing SER per bit. In most cases soft errors can be captured and corrected by on-chip

algorithms. However for some devices such as ASICs, on-chip error detection and correction may not cover 100% of the chip and thus additional measures must be taken to manage the source of SER. One of such areas is packaging material selection and assembly process control.

Specifically for flip chip devices, packaging materials such as underfill and solder bumps are the main sources of alpha emission. The close proximity of these materials to the active surface of the silicon suggests that even small doses of contamination by high-alpha materials can have significant impact on

the SER. For devices that require high reliability and low FIT (failure in time) rate, ULA (Ultra Low Alpha) underfill and solder bumps have been implemented by most manufacturers. In addition, maybe more importantly, the assembly process must also be strictly controlled. For many assembly lines, components with 100% ULA materials are processed on the same equipment with those are not 100% ULA. Cleaning is performed between the change-over of material sets, but the possibility for cross-contamination exists and the impact of such contamination needs to be evaluated.

For packaging materials, alpha particles are typically emitted from the decay of impurities such as Th and U, which exist in constituents including silica fillers and metals. [2] The decay sequence and energies of the alpha particles emitted from these decays are listed in Table 1.1 and Table 1.2. [3] These data show that the highest alpha energy is less than 10MeV.

Table 1.1 Th decay sequence and alpha particle energies

Species	Alpha Energy (MeV)
Th-232	4.1
Th-228	5.5
Ra-224	5.8
Rn-220	6.4
Po-216	6.9
Bi-212	6.3
Po-212	8.9

Table 1.2. U decay sequence and alpha particle energies

Species	Alpha Energy (MeV)
U-238	4.3
U-234	4.9
Th-230	4.8
Ra-226	4.9
Rn-222	5.6
Po-218	6.1
Po-214	7.9
Po-210	5.4

The penetration range of these alpha particles in the active silicon is dependent upon the initial energy of the particles and the material properties that they travel through. For back end of the line (BEOL) materials such as Cu and SiO₂, the range of alpha particles is reproduced in Figure 1 from [4]. For the maximum possible alpha energy,

the range for these particles in SiO₂ and Cu would be approximately 50 μ m and 20 μ m, respectively.

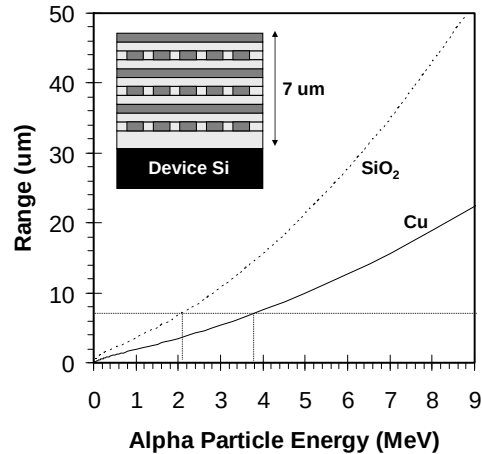


Figure 1. Penetration range in Cu and SiO₂ for alpha particle with energy below 9MeV.

For alpha particles emitted from impurities away from the silicon surface, they will lose energy as they travel through various packaging and BEOL materials. Considering that majority of the alpha particles have relatively low initial energy levels [2] and they become even lower as they reach the silicon surface, we only need to be concerned with materials immediately adjacent to the die surface. For flip chip packages, these materials include underfill, solder bump, and pre-solder on the substrates for most plastic BGAs. A schematic view of a flip chip solder joint is shown in Figure 2.

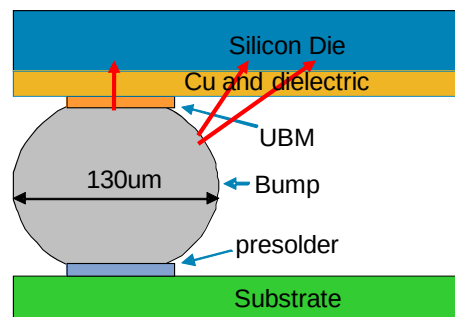


Figure 2. Schematic view of the cross-section of a flip chip solder joint.

In the following, we will investigate the effects of key process steps and equipment on the alpha emissivity levels on flip chip packages with two experiments. First, blank silicon wafers are processed through major steps of the assembly process. Both a dedicated ULA assembly line and a

mix-use line are evaluated. Contacts and handling by equipment and tooling are simulated on these wafers, and after each step, one wafer is taken out of the process for alpha emissivity measurement. Second, actual flip chip components with an ULA package material set are assembled on the same dedicated ULA and mix-use assembly lines. Alpha emissivity levels near the active silicon surface are measured for both groups of components.

Experimental

For the experiment using blank wafers, a total of 7 wafers are used. The selected process steps and split are shown below in Table 2. A set of 3 wafers are processed through 3 major assembly steps on both assembly lines. At each process step, equipment touch-downs and handling steps are simulated without the actual use or application of materials such as chip attach solder paste or underfill. After each of the 3 steps, one wafer is taken out from each of the 2 assembly lines and sent out for alpha emissivity measurements. The measurements time for each wafer is approximately 48 hours.

Table 2. Wafer allocation for the two assembly lines. Only one T0 wafer is used. For each of the 2 assembly lines, 3 wafers are used and after each of the 3 steps, one wafer is removed for alpha emissivity measurement.

Process	Dedicated ULA Assembly Line	Mix-Use Assembly Line
T0	1 wafer	
Cap Attach Solder Printing	1 wafer	1 wafer
Chip Attach Reflow	1 wafer	1 wafer
Underfill Cure	1 wafer	1 wafer

The second portion of the work uses actual flip chip components. All packaging materials are ULA grade, including underfill and solder bump. The same material set is process on 2 separate assembly lines. For the dedicated ULA line, a segment of the assembly process (shown in Figure 3) is entirely isolated from the rest of the facility and only ULA materials are processed. These steps are considered the necessary and sufficient steps to ensure no cross-contamination occurs near the die surface. For the second assembly line, the selected flip chip component is processed on a mix-use assembly line

with all necessary cleaning steps performed per specifications.

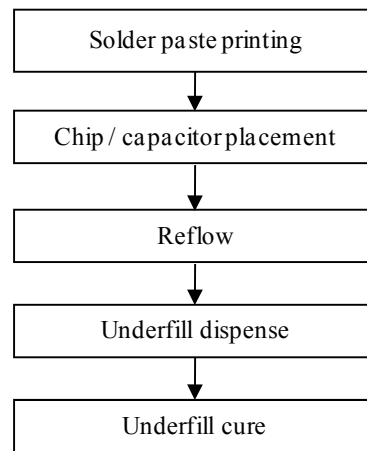


Figure 3. Portion of the assembly flow for the flip chip component. For the dedicated ULA line, only ULA materials are processed on these equipment. For the mix-use line, cleaning is performed between switch-over per specifications.

To measure the alpha emissivity near the die surface, the flip chip components are ground and polished to the plane right below the silicon. Referencing Figure 3, the polishing plane would be immediately below the UBM layers. To ensure sufficient accuracy, a large number of components are used and a total of ~100 cm² exposed areas were measured. The total data collection time is a minimum of 24 hours.

Results and Discussion

Alpha Emissivity Data Collection

The alpha emissivity data are collected on a low-background ionization counter manufactured by XIA. Counting low-level alpha emissivity in the presence of background in a counter is a difficult task. As the count rate from the sample falls to or below the background rate, the time required to gather the necessary statistics increases dramatically. It has been shown that the necessary counting time t follows [5]

$$t = \frac{K^2}{S^2} (S + 2B) \quad (1)$$

where S and B are the sample emissivity and background emissivity, respectively, and K is the ratio of S to its standard deviation σ . As can be seen from this equation, reducing background is the most critical step in reducing total counting time. Improvement in background reduction and

measurement can result in 5-fold or more reduction in counting time. Further discussion on reducing the background count and improving counter construction can be found elsewhere. [5]

For the current evaluation, the counting gas used is Ar, and the counting time is approximated 48 hours for each wafer or component sample. The background emissivity level is measured prior to each sample.

Alpha Emissivity on Blank Wafer Samples

A typical energy spectrum of the alphas from the wafer samples are shown below in Figure 4. In this case the wafer measured is the T0 sample. The maximum energy observed is slightly below 10 MeV, which is the case for all 7 wafers measured.

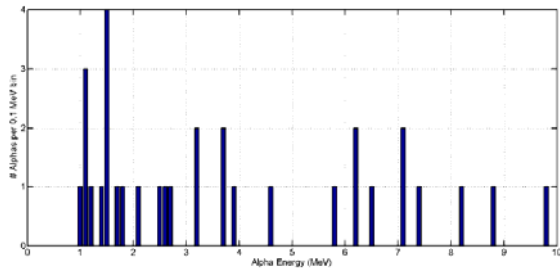


Figure 4. Energy spectrum of alphas from blank wafer at T0. The highest energy is slightly less than 10 MeV.

Within the total data collection time of 48 hours for this wafer, the arrival time distribution for the alphas captured is shown in Figure 5. The calculated alpha emissivity based on this data set is shown in Figure 6. The decreased confidence interval suggests that the 48-hour data collection time offers sufficient data accuracy.

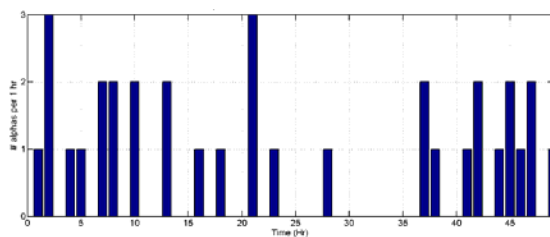


Figure 5. Arrival time for alphas on the T0 wafer.

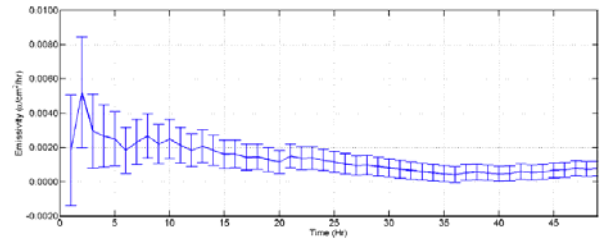


Figure 6. Calculated alpha emissivity for wafer T0

The measured alpha emissivity data on all 7 wafers are listed below in Table 3 and plotted in Figure 7. Wafers from the dedicated line are indicated with the diamond symbols, and wafers from the mix-use line are indicated with the square symbols. For both sets of data, the vertical dashed lines are the values of the calculated error.

Table 3. Alpha emissivity measurements on wafers from the dedicated ULA line and the mix-use line. These data are also plotted in Figure 7.

Wafer	Alpha Emissivity for the Dedicated ULA Line	Error
T0	0.000758	0.000427
Cap Attach Solder Printing	0.001062	0.000469
Chip Attach Reflow	0.001025	0.000429
Underfill Cure	0.001122	0.000396

Wafer	Alpha Emissivity for the Mix-Use Line	Error
T0	0.000758	0.000427
Cap Attach Solder Printing	0.000401	0.000407
Chip Attach Reflow	0.000951	0.000445
Underfill Cure	0.001314	0.00047

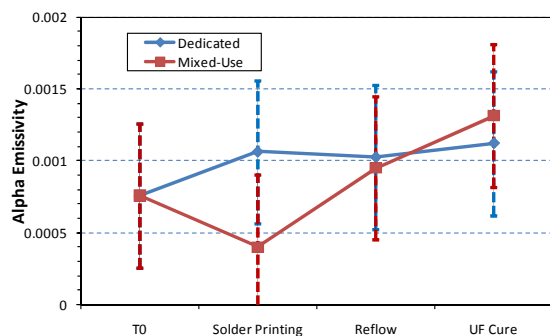


Figure 7. Alpha emissivity measured on all 7 wafers as designated in Table 2.

The magnitude of the error bars appears to be large relative to the calculated alpha emissivity values of the wafers. However for emissivity levels seen here, these ranges of errors are in fact reflective of the much improved counter design, and can help provide a qualitative comparison of the two processes. With the consideration of the range of error, the alpha emissivity data from the wafers appear to suggest that there is no statistical difference between the two processes.

Alpha Emissivity on Flip Chip Components

For the flip chip component samples, the alpha emissivity measurements are shown below in Table 4. Compared with the wafer samples, the difference in alpha emissivity is much larger, and the samples from the dedicated ULA line showed clearly lower alpha emissivity levels.

Table 4. Alpha emissivity data on the flip chip components processed on the dedicated ULA line and on the mix-use line. The difference is larger than those seen on the blank wafer samples.

Assembly Line	Alpha emissivity (count / hour / cm ²)
Dedicated ULA	0.0038±0.004
Mix use	0.038±0.005

The results from the wafer samples and the component samples suggest that the dedicated ULA assembly line can consistently offer low alpha emissivity levels. With the equipment and tooling completely isolated from high-alpha materials, the risk for cross-contamination can be effectively controlled.

For the mix-use assembly setup, although the wafer samples showed good emissivity levels, the component samples showed otherwise. The elevated alpha emissivity level could come from a variety of

sources, including contamination from the equipment, tooling, or handling. Considering it is nearly impossible to perform in-line alpha emissivity monitor, these results suggest that when ULA emissivity is required for a component, in addition to the use of ULA material set, the assembly process setup and control is equally critical in order to achieve high device reliability performance, and a dedicated ULA line may offer the most reliable solution.

Conclusions

In this work we analyze the impact of assembly process setup on the alpha emissivity levels near the active silicon surface. Simulated processing is performed using blank silicon wafers on a dedicated ULA line and a mix-use line, and actual flip chip components with 100% ULA material set are also manufactured on the same two lines. The results suggest that the dedicated ULA line offered consistently low alpha emissivity levels, while on the mix-use line, large variation in alpha emissivity levels are observed. These results suggest that for devices that require the highest reliability and lowest SER from packaging materials, a dedicated ULA line may be the most consistent and reliable solution.

Acknowledgments

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