

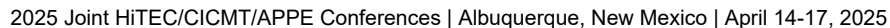


AFRL

TEMPERATURE, VOLTAGE, AND PROXIMITY LIMITATIONS IN AISCN NON-VOLATILE MEMORY DEVICES FOR EXTREME ENVIRONMENTS

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LOGIC

- SiC
- III-Nitrides
- $\beta\text{-Ga}_2\text{O}_3$
- Diamond

GATE DIELECTRICS AND INSULATORS

- Oxides (SiO_x , HfO_x , AlO_x)
- Nitrides (AlN , SiN)

MEMORY

- Flash memory (HfAlO , ZrAlO)
- Resistive memory (HfO_x , TiO_x , NiO)
- Ferroelectric memory (AlScN , HfZrO , PZT)

CONTACTS AND INTERCONNECTS

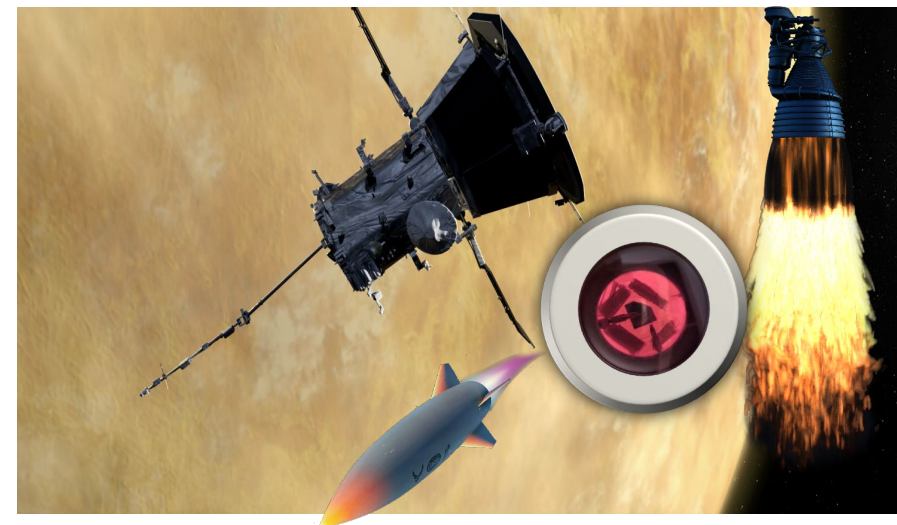
- Pt, Au, Ti, Ni, Mo, TiN, W, TaSi_2

Bonding metals

- Au alloys, Ag-Cu alloys

INTEGRATION AND PACKAGING

- AlN substrate
- Ceramic substrates (Post- and co-fired)

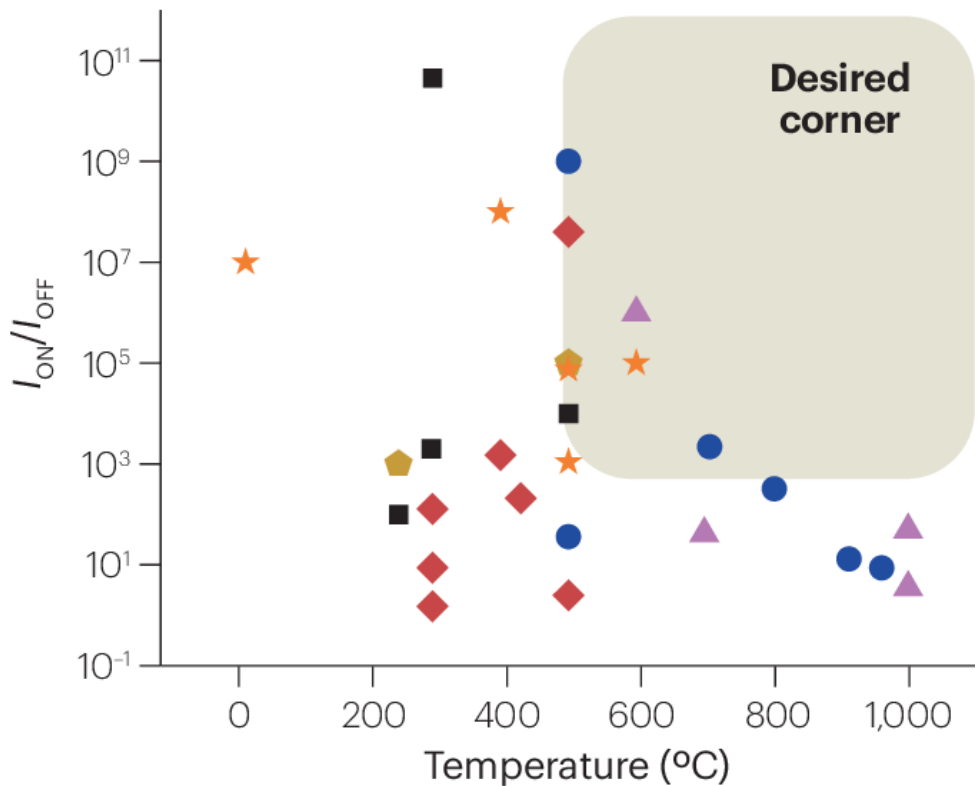


		Application Domains							
		Commercial		Industrial	Automotive	Military	SOI CMOS	WBG	UWBG
Phase Transitions / Temps of Interest	°C	Standard Temp. Range [Organic Packaging]			Extreme Temp. Range [Ceramic Packaging]			Environments	Substrates
Magma	1000								Postfire Ceramic Systems
	800							Hypersonic Flight	
	700							Molten Salt Reactors	
	600								
	500								
Lead melts	400							Enhanced Geothermal	
	362							Venus surface	
	327								
	315							Internal Combustion Engines	Co-fired Ceramics Systems
	300							Down Hole Oil Exploration	
	225								
	150							Automotive (high)	
	125							Military Aerospace (high)	
Liquid water boils	100							Industrial Electronics (high)	Organics
	85							Commercial Electronics (high)	
	15							Mars surface, daytime (high)	

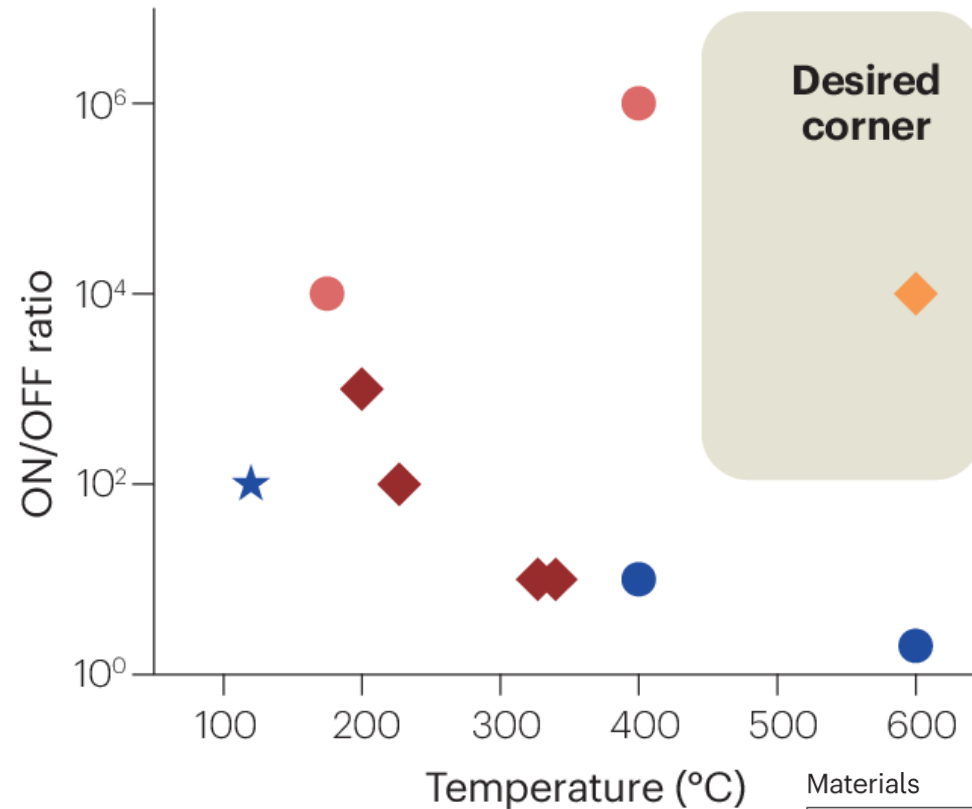
Moore, D.C. et al. Nat. Rev. Mater. 9, 790–807 (2024)

HT Non-Volatile Memory (NVM) is Less Mature than Logic

2024 SOTA Transistor Performance



2024 SOTA NVM Performance

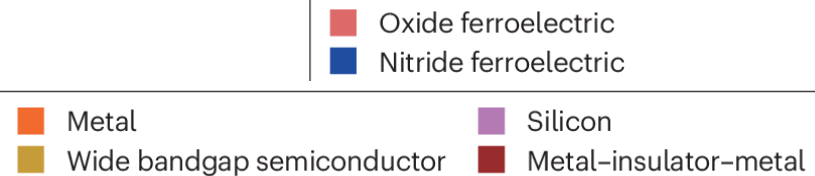


Moore, D.C. et al. Nat. Rev. Mater. 9, 790–807 (2024)

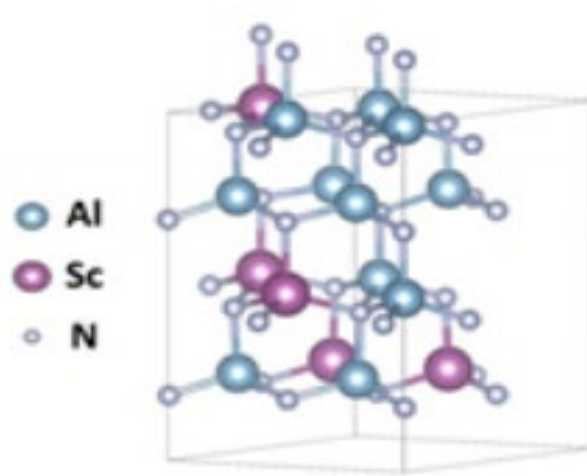
Device architecture



Materials



Wurtzite-Structured AlScN



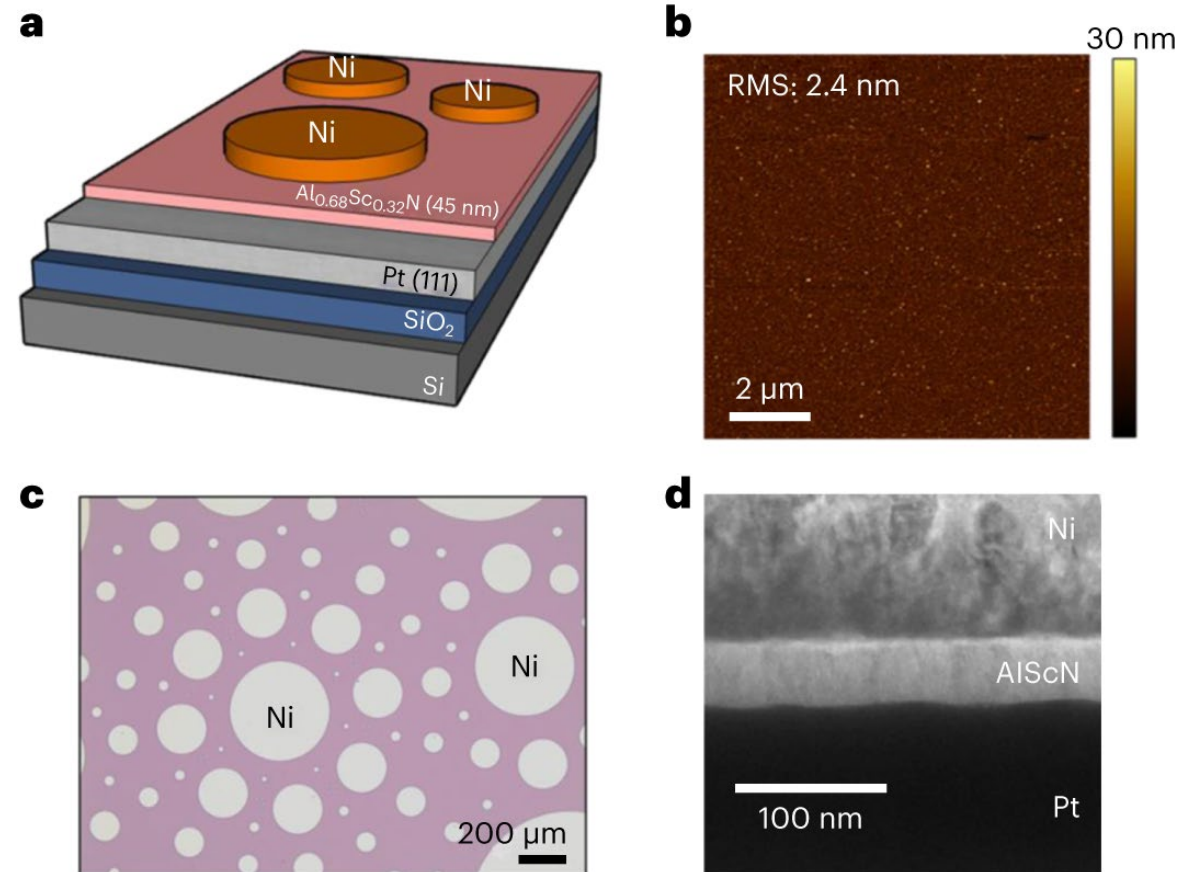
E_c (kV/cm) ~2000–5000

P_r ($\mu\text{C}/\text{cm}^2$) ~80–150

E_g (eV) ~2.9–6.1

T_c ($^{\circ}\text{C}$) >1100

Qin H. et al. Nanomaterials. 2024

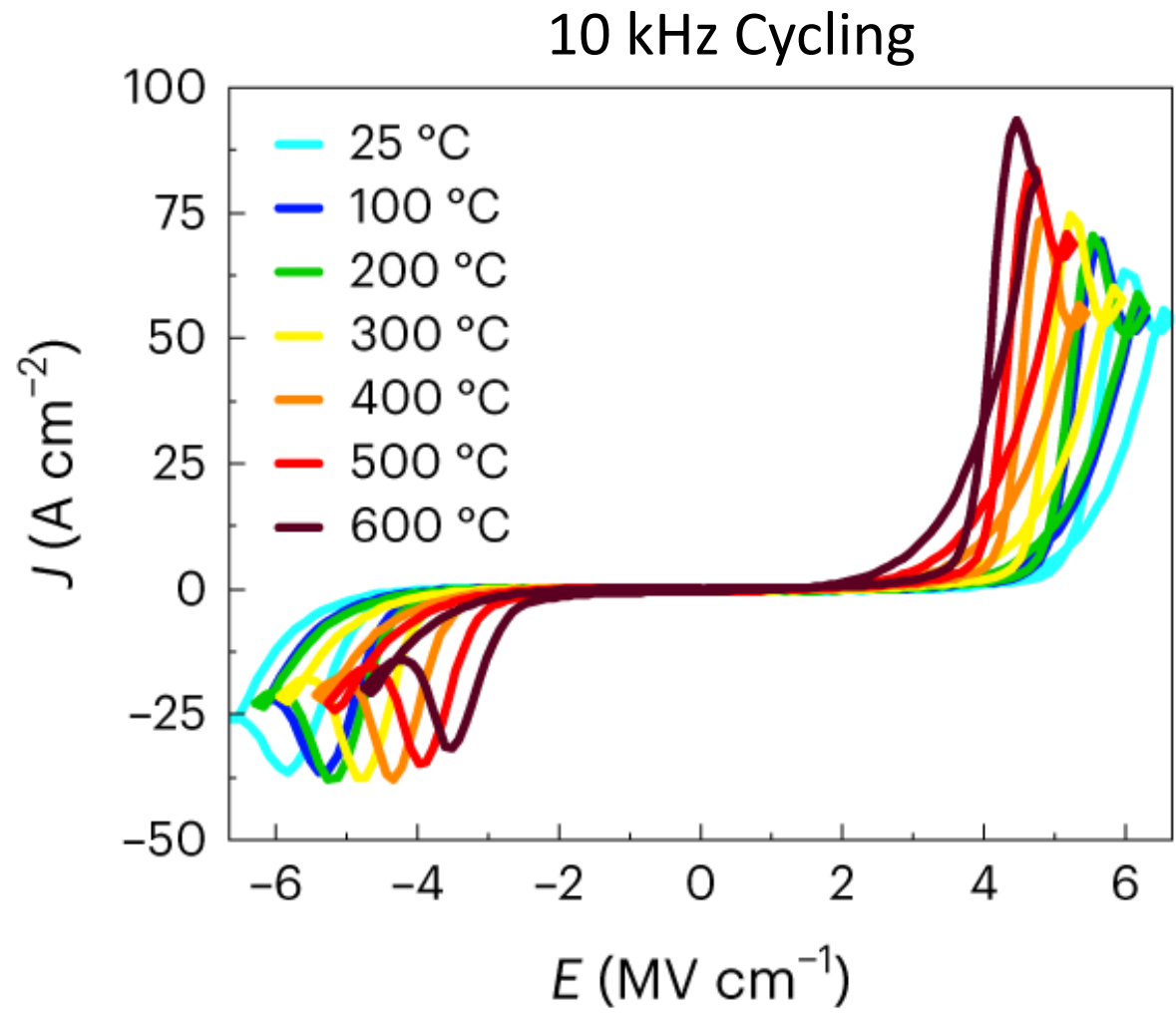
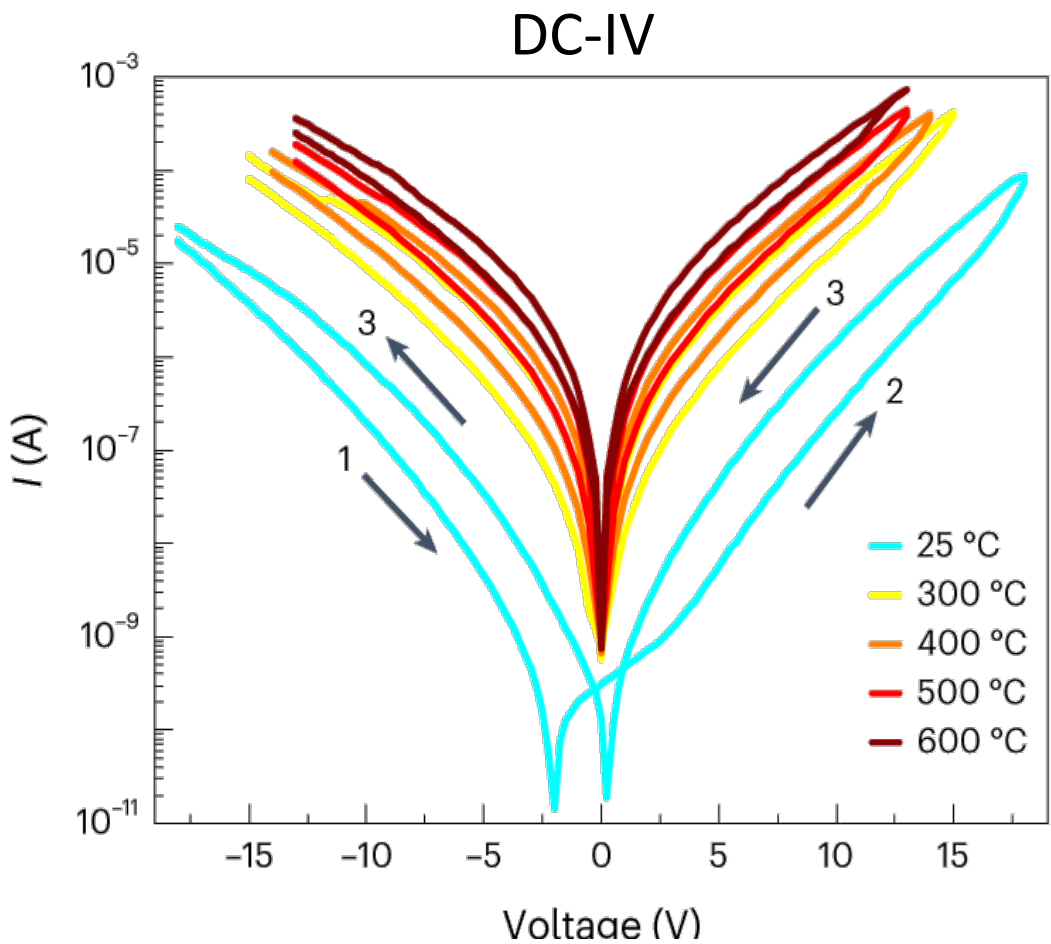


Excellent films down to 10 nm

Moore, D.C. et al. Nat. Electron. 7, 348–355 (2024)



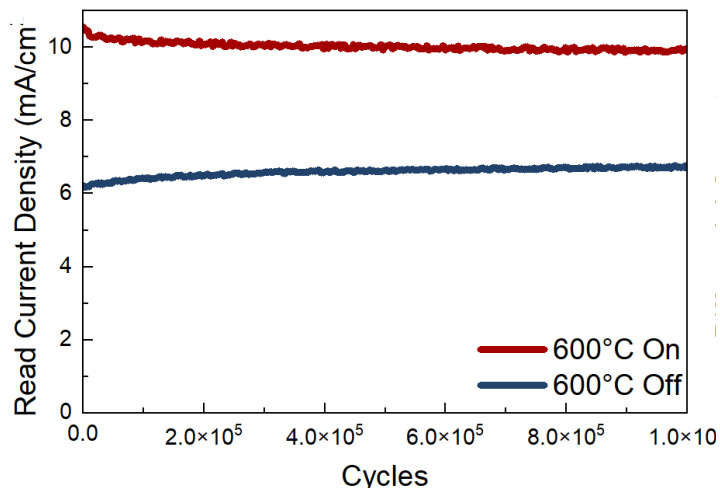
Device Demonstration



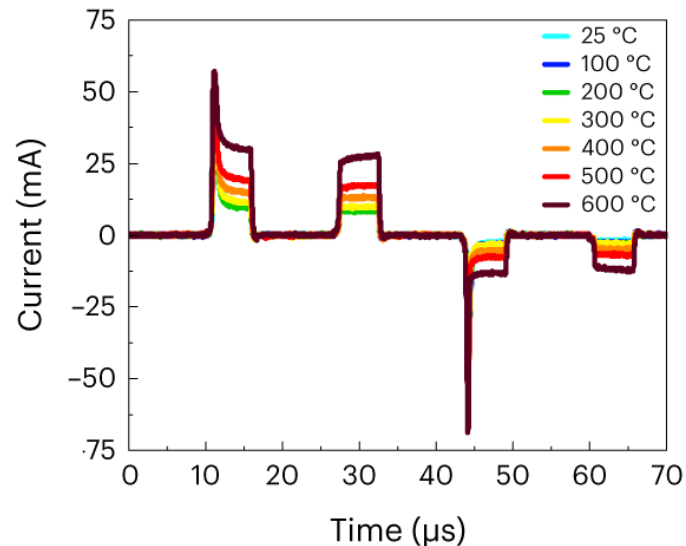
Moore, D.C. et al. Nat. Electron. 7, 348–355 (2024)

Device Demonstration

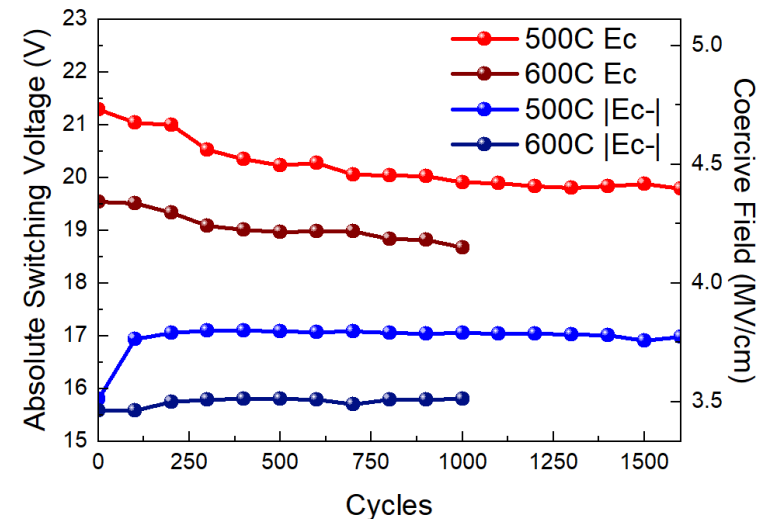
Read Endurance



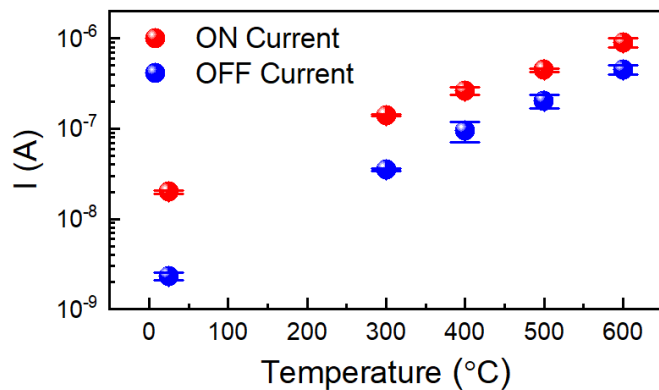
PUND



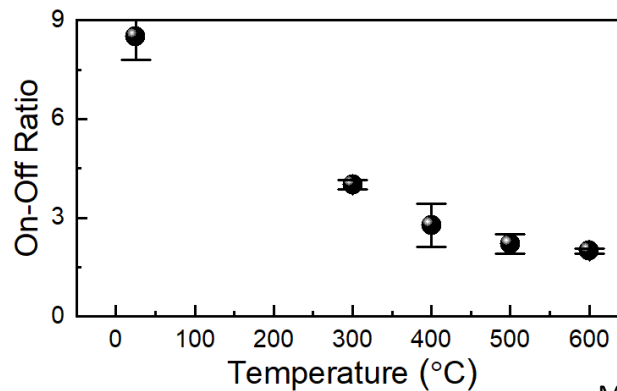
Write Endurance



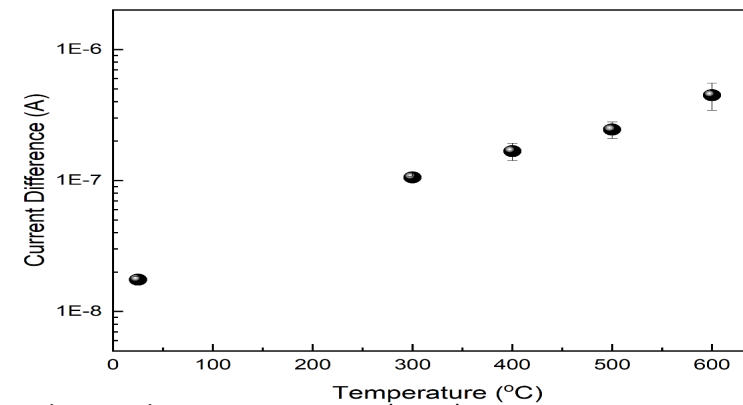
Read Currents



Read Current Ratio



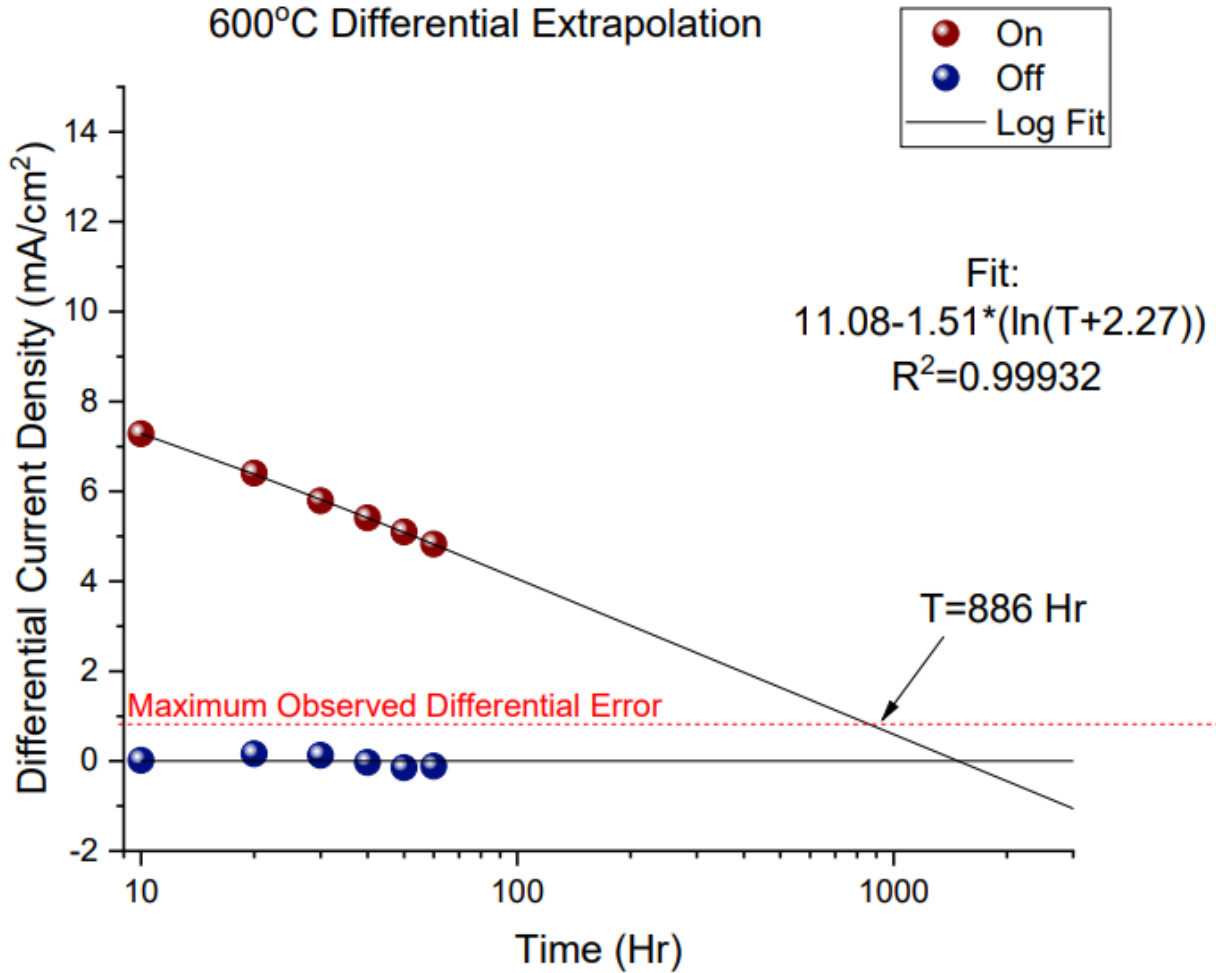
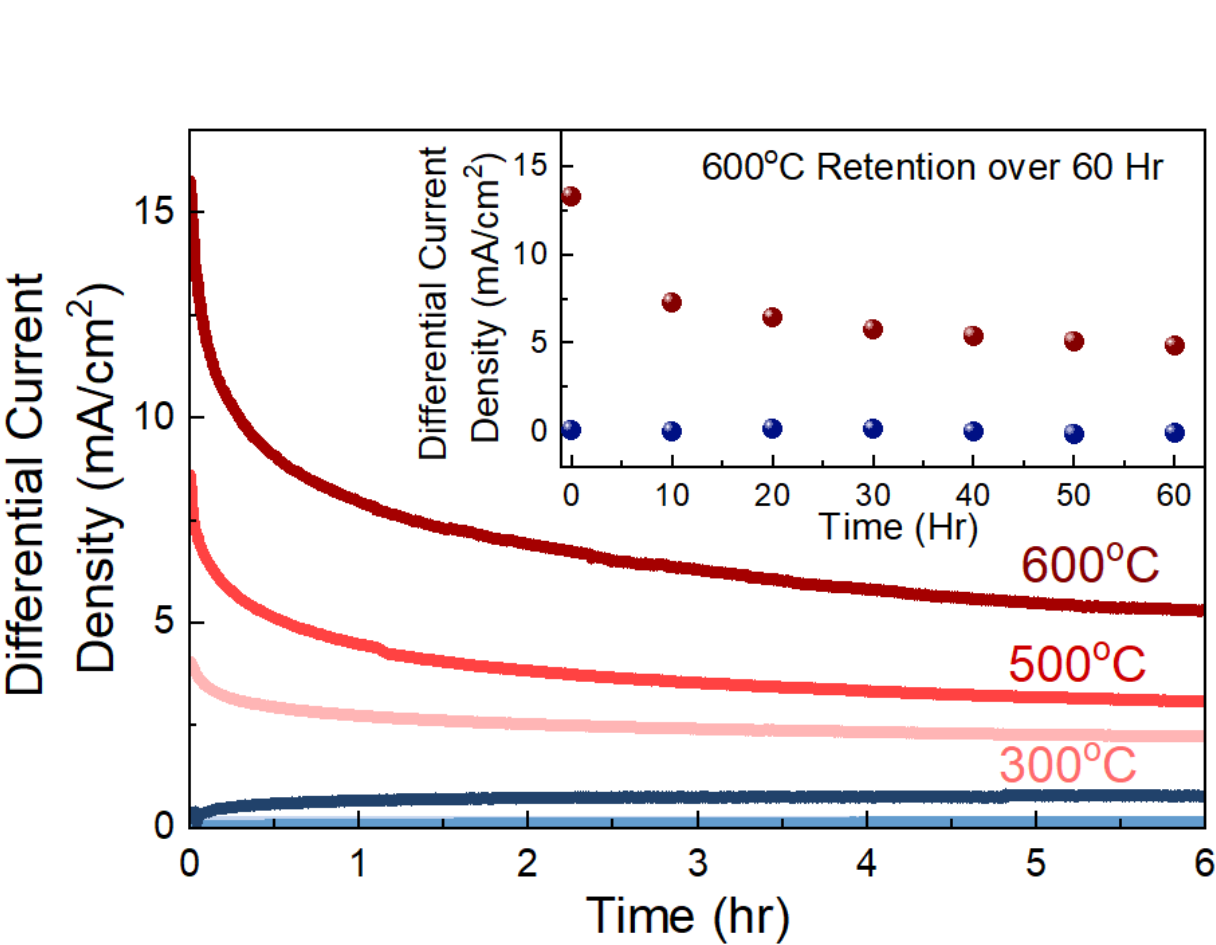
Absolute Read Current Difference



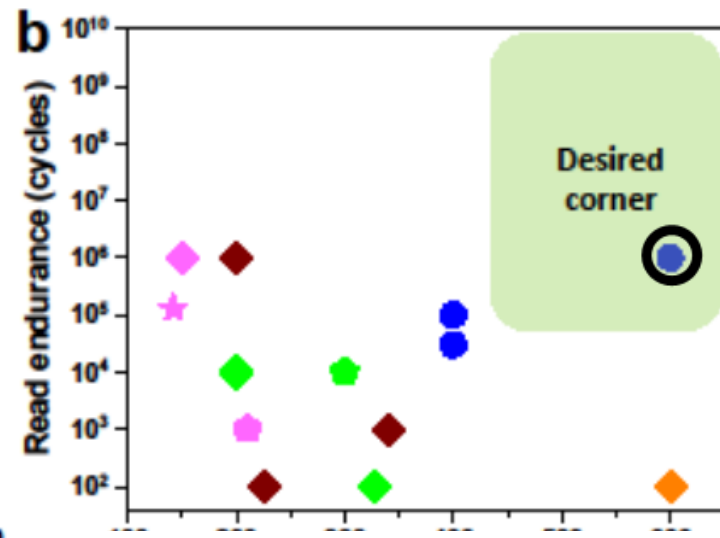
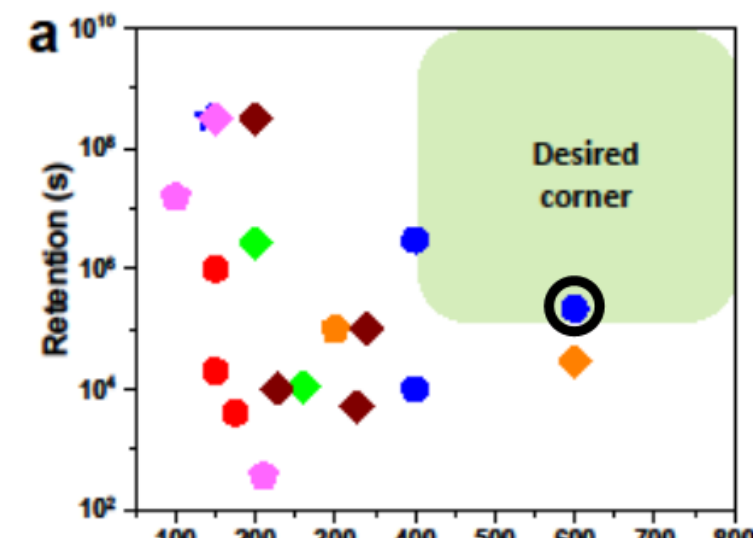
Moore, D.C. et al. Nat. Electron. 7, 348–355 (2024)



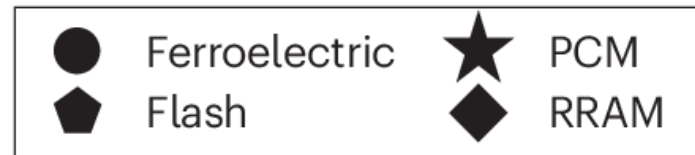
Retention at 600 °C



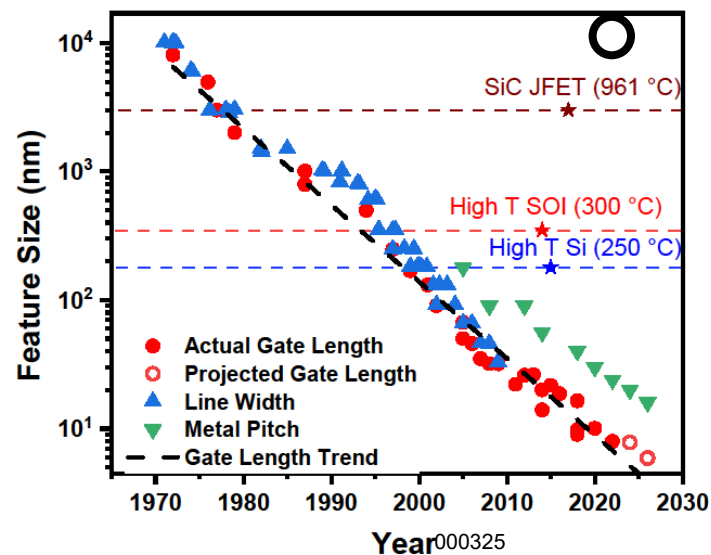
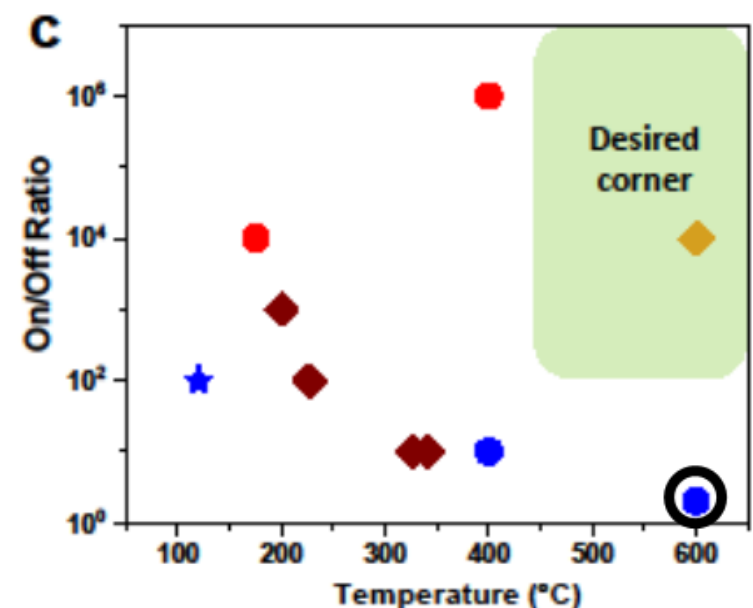
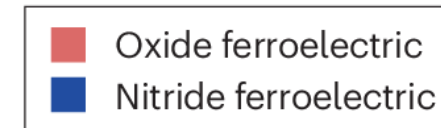
State of the Art (early 2024)



Device architecture



Materials

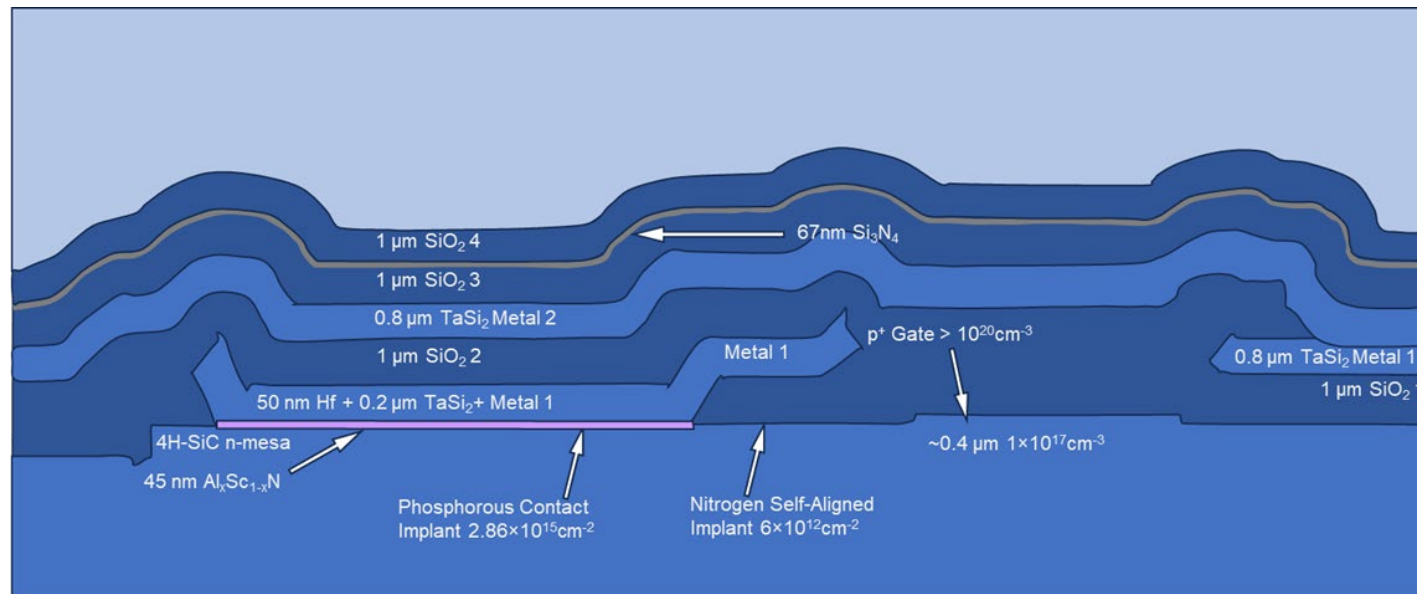
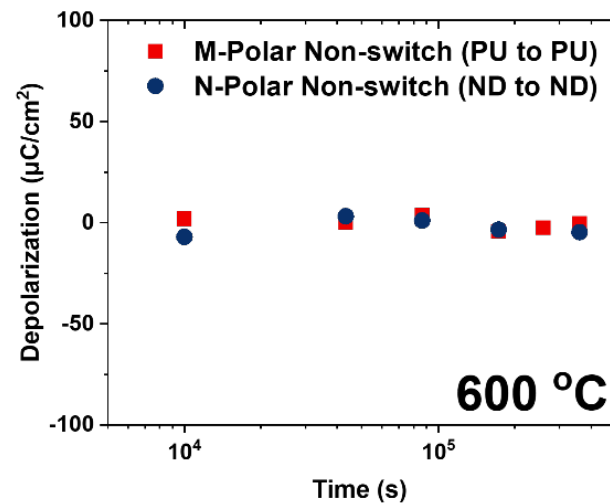
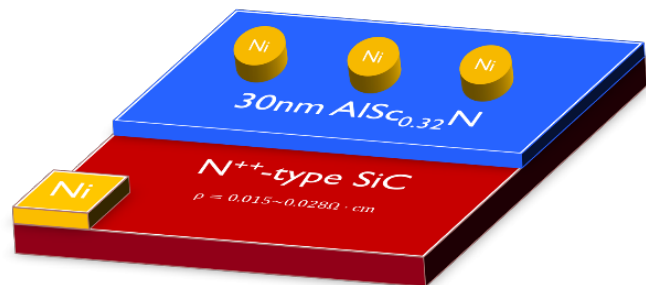


○ Presented 2024 Work

- Great retention and read endurance
 - Bad On/Off ratio

Moore, D.C. et al. Nat. Rev. Mater. 9, 790–807 (2024)

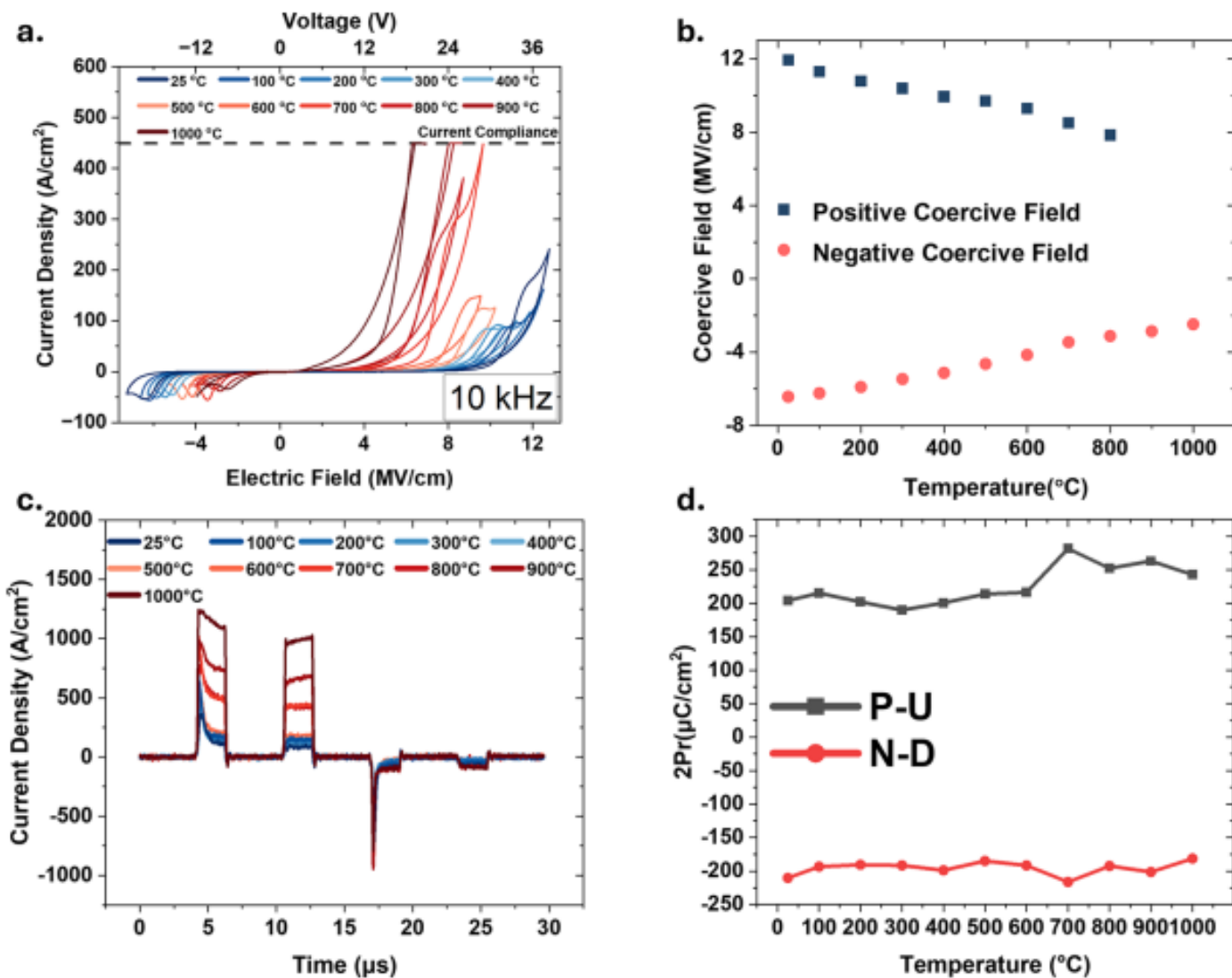
SiC Integration



No depolarization through 100 Hrs at 600 °C

He, Y.; Moore, D.C. et al. Nano Lett. 2025, 25, 12, 4767–4773

Demonstration to 1000 °C



He, Y.; Moore, D.C. et al. Nano Lett. 2025, 25, 12, 4767–4773



Current Efforts

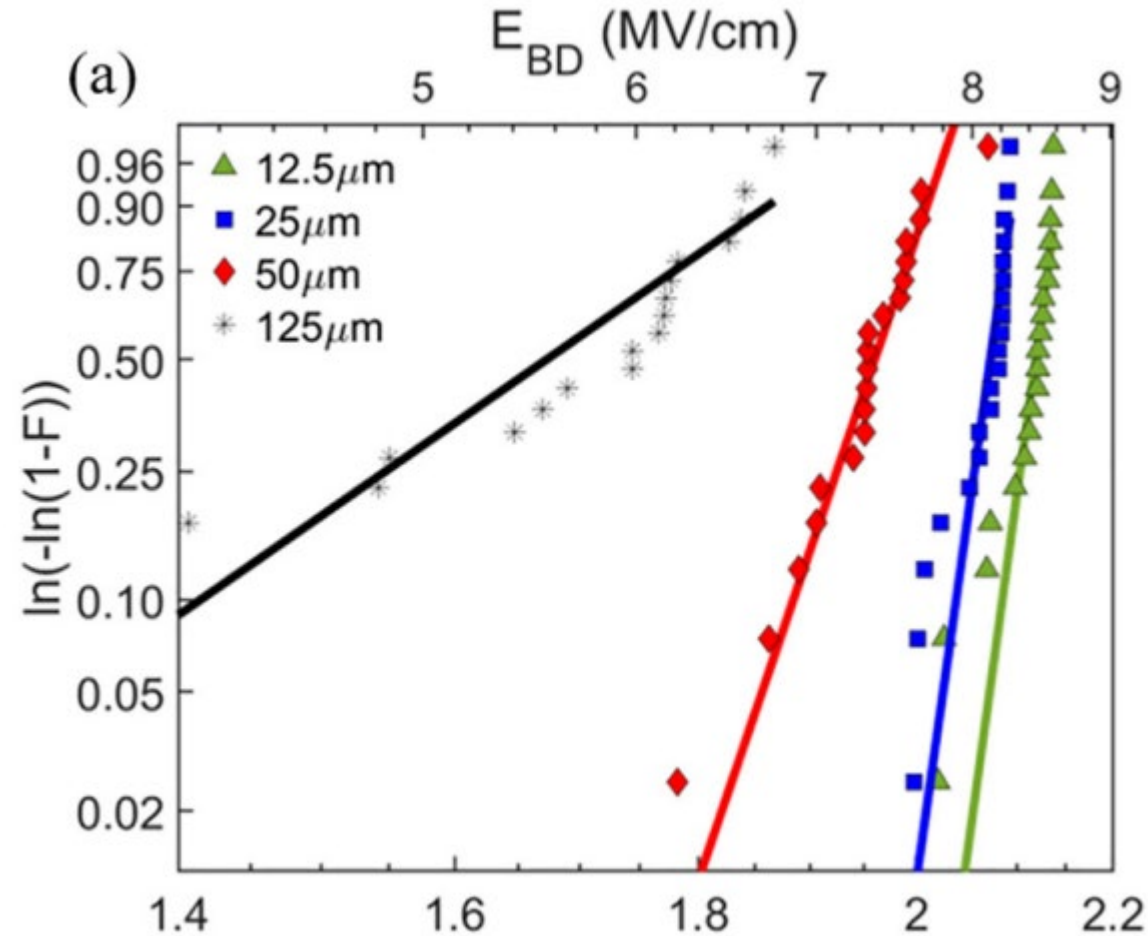
- ✓ High Temperature Operation
- ✓ Retention
- ✓ Substrate Variety

Improved
Data
Density

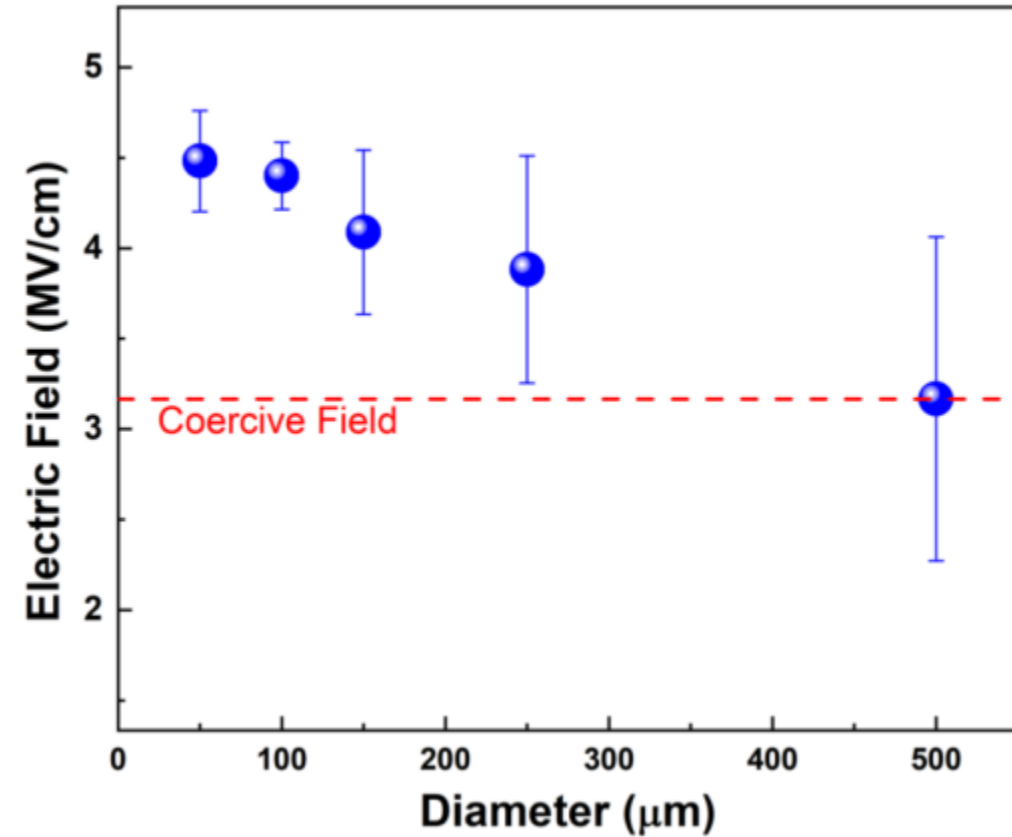
Improved
On/Off
Ratio

Endurance

Miniaturization Improves Data Density and Endurance

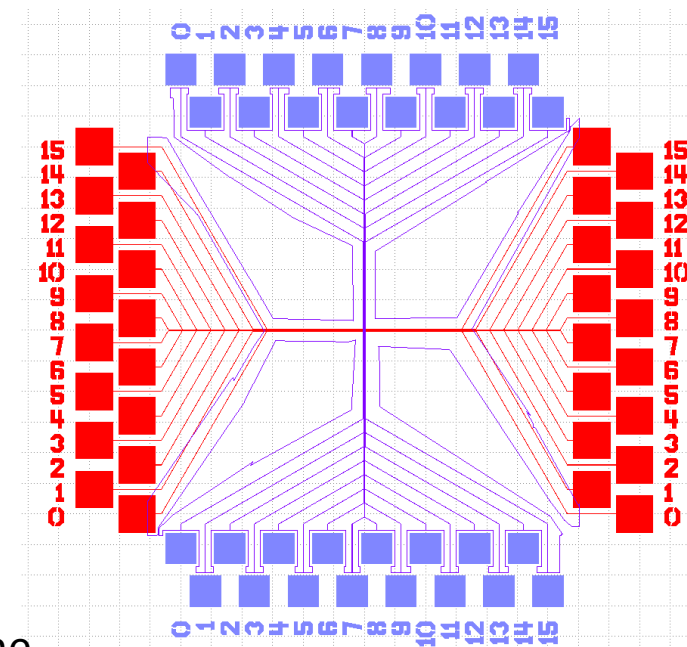
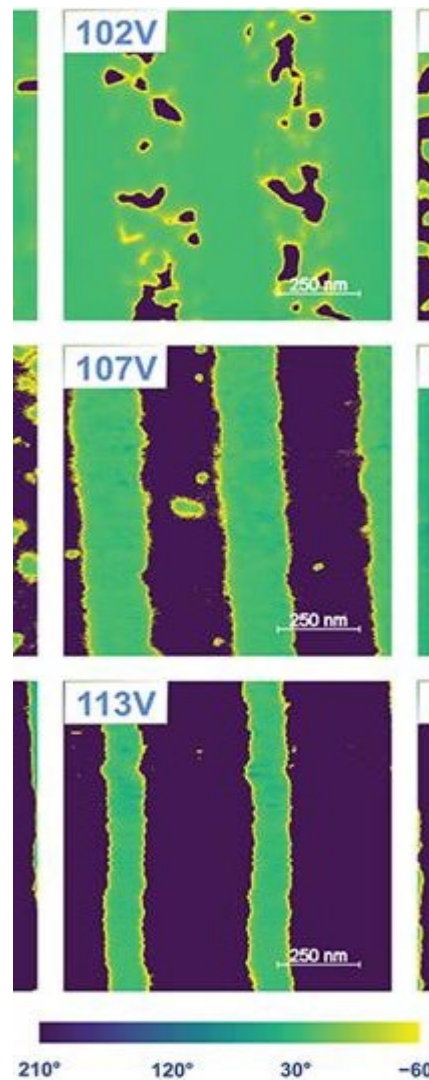
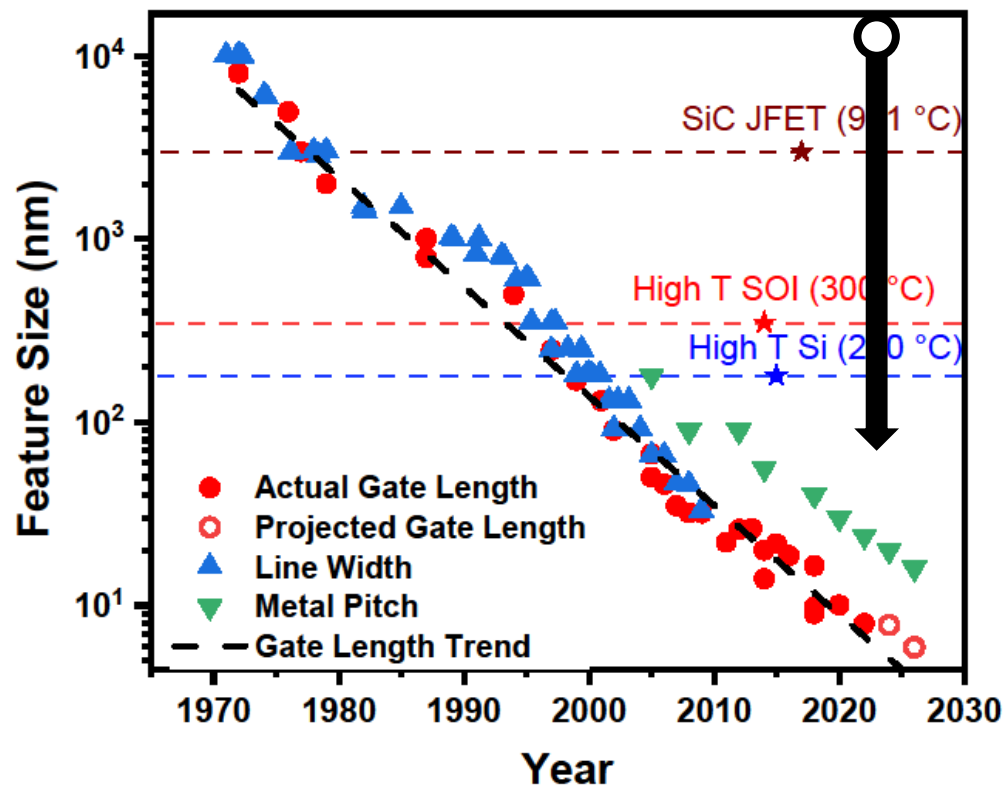


Zheng J. *et al.* Appl. Phys. Lett. 122, 222901 (2023)



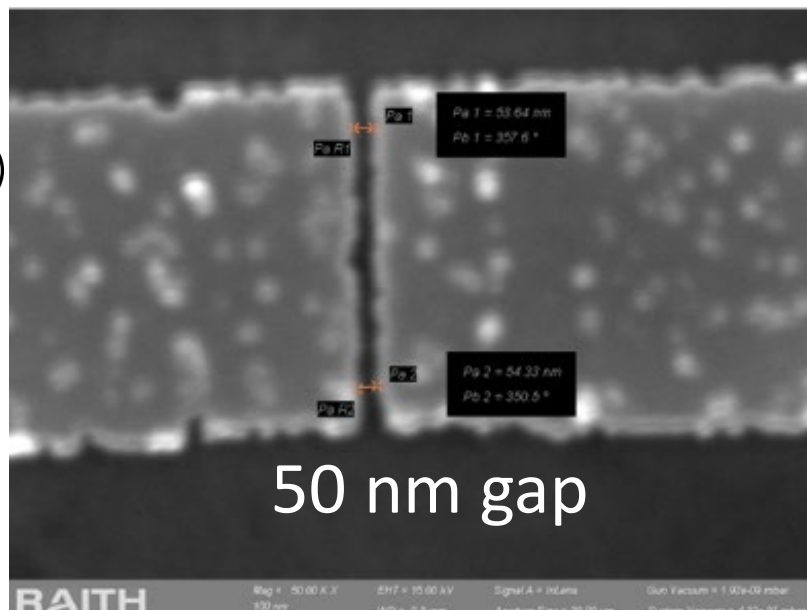
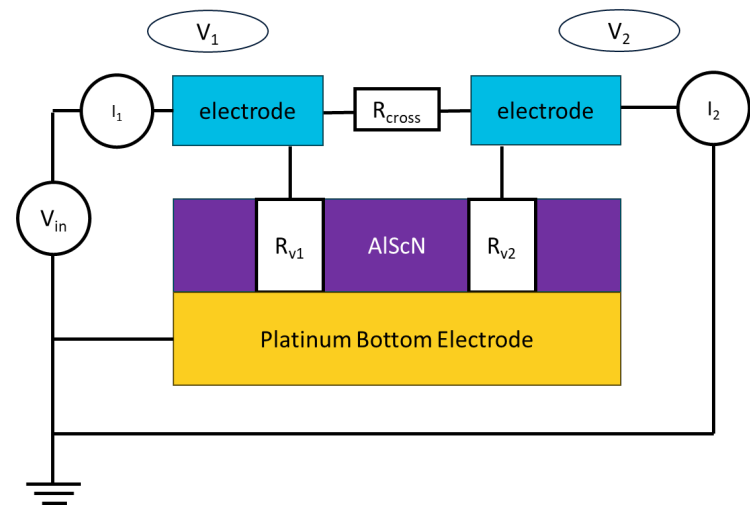
Moore, D.C. *et al.* Nat. Electron. 7, 348–355 (2024)

Is There a Limit to Miniaturization?

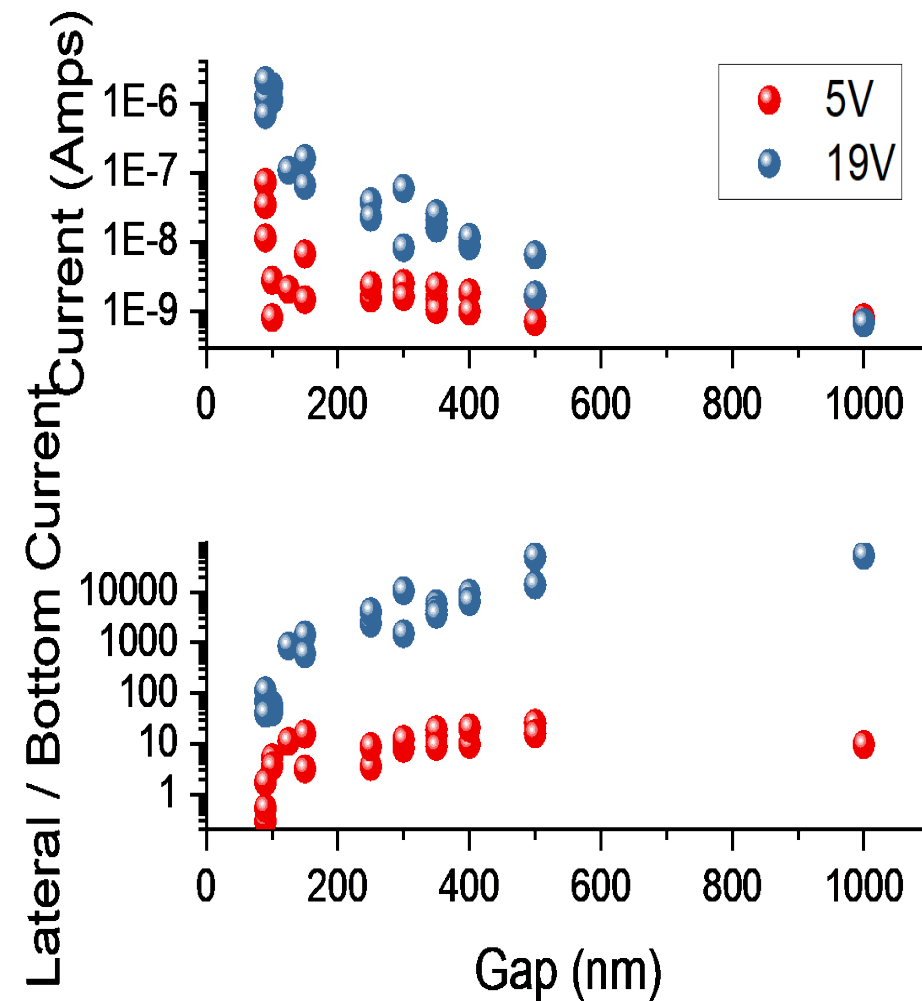
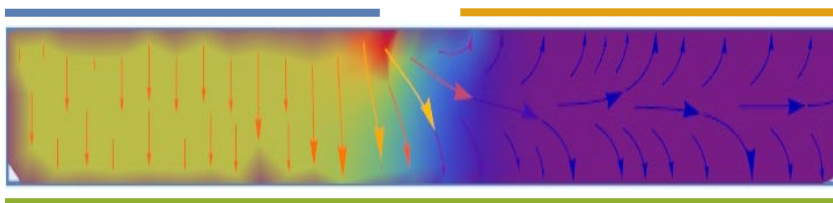


Ferroelectric domains on the order of 100 nm

Lateral Leakage



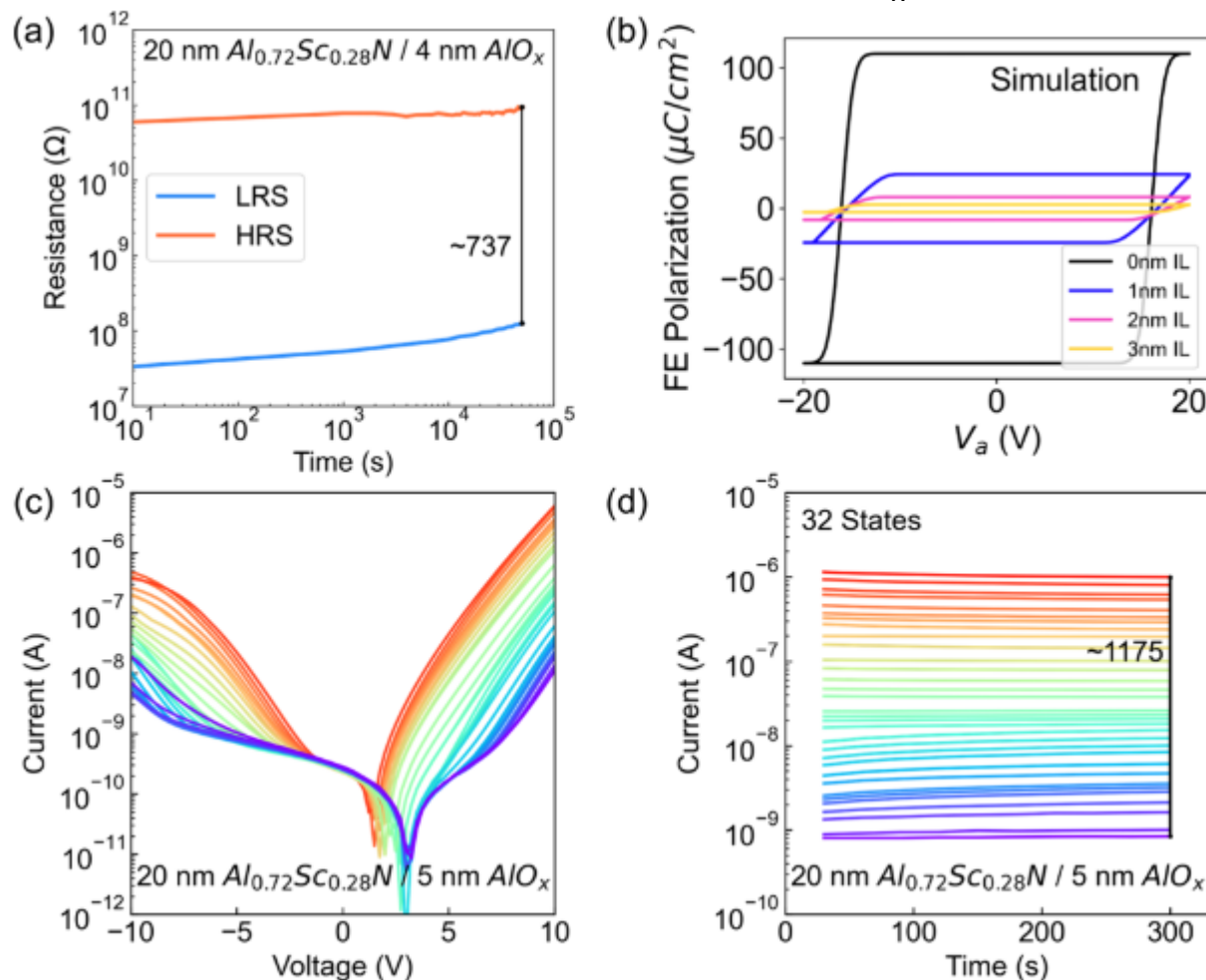
- Active Pad
- Reference Pad
- Bottom Electrode



False writes unlikely, false reads possible up to 3x thickness

Improved On/Off Ratio Via Encapsulating Layer

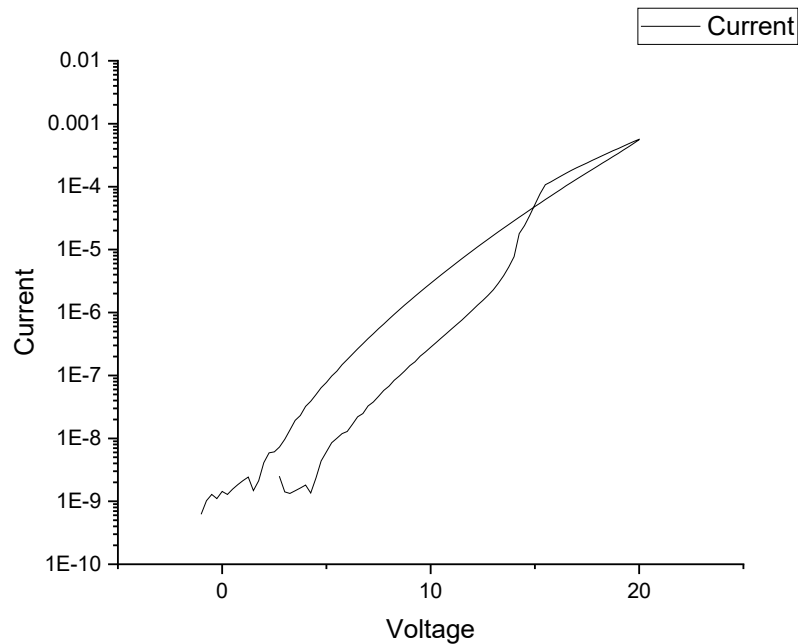
20 nm AlScN with 4 nm Al/O_x



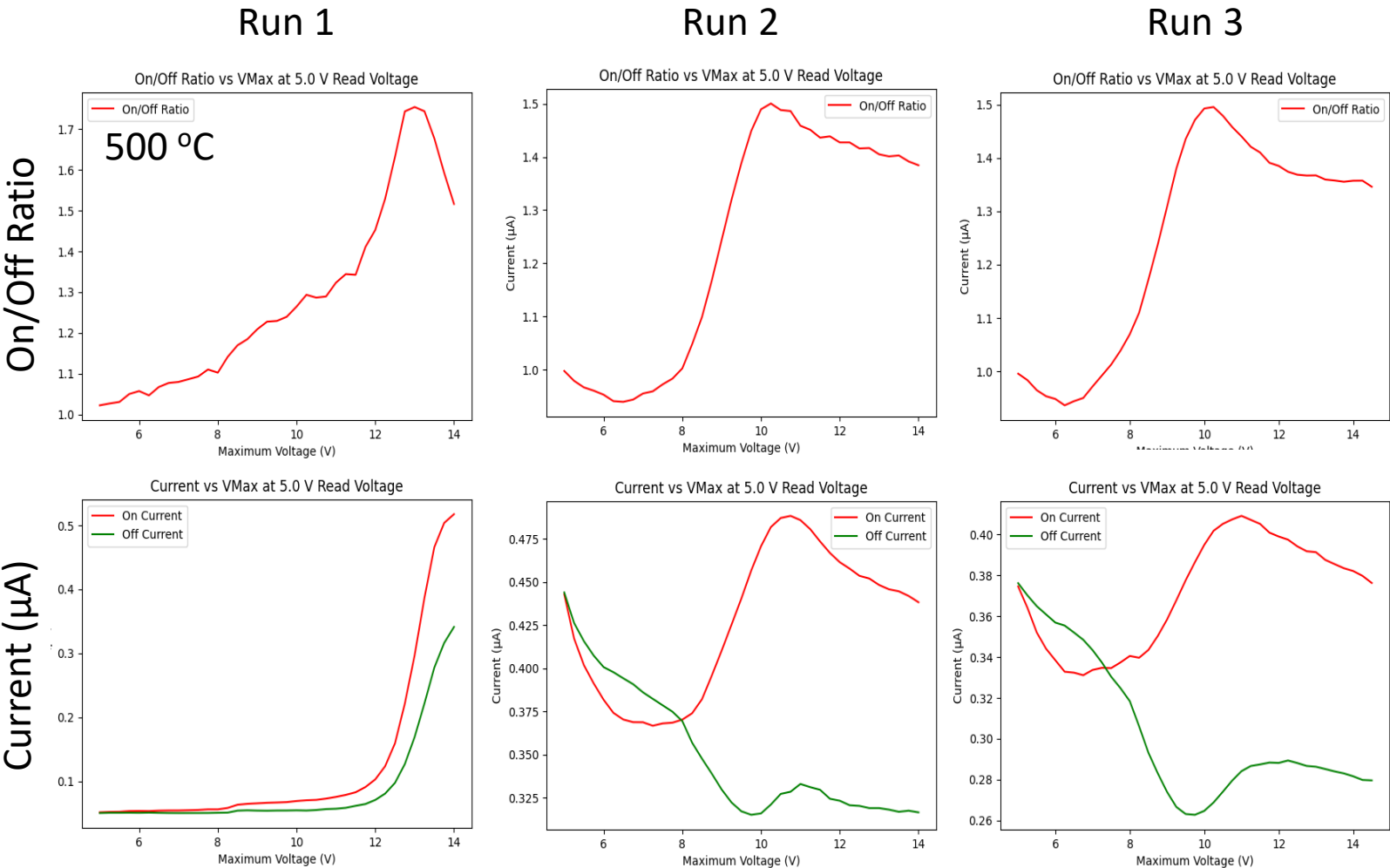
Kim K. *et al.* ACS Nano 2024, 18, 24, 15925–15934

On-Sate Current Loss: Impending Breakdown Indicator?

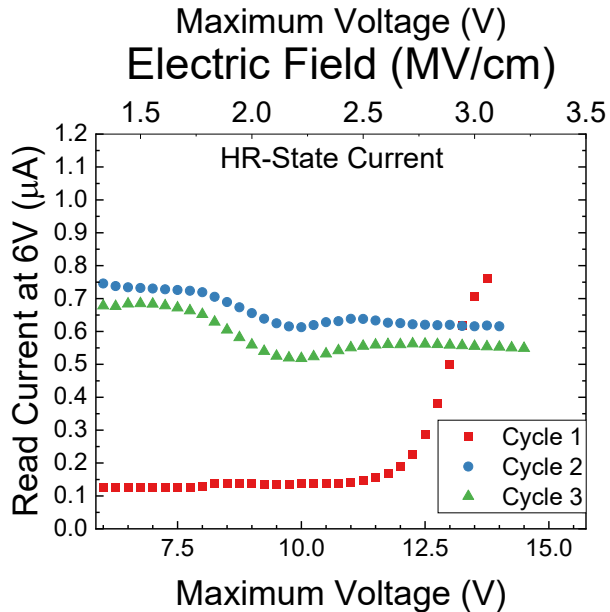
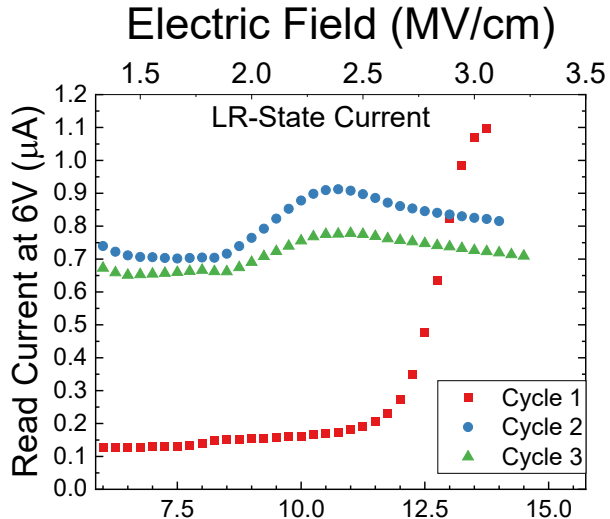
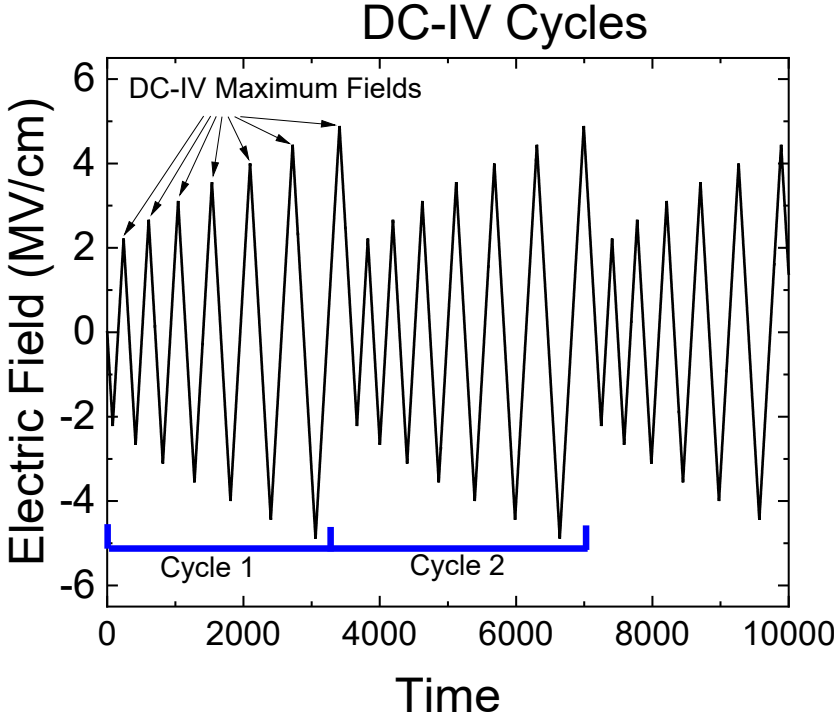
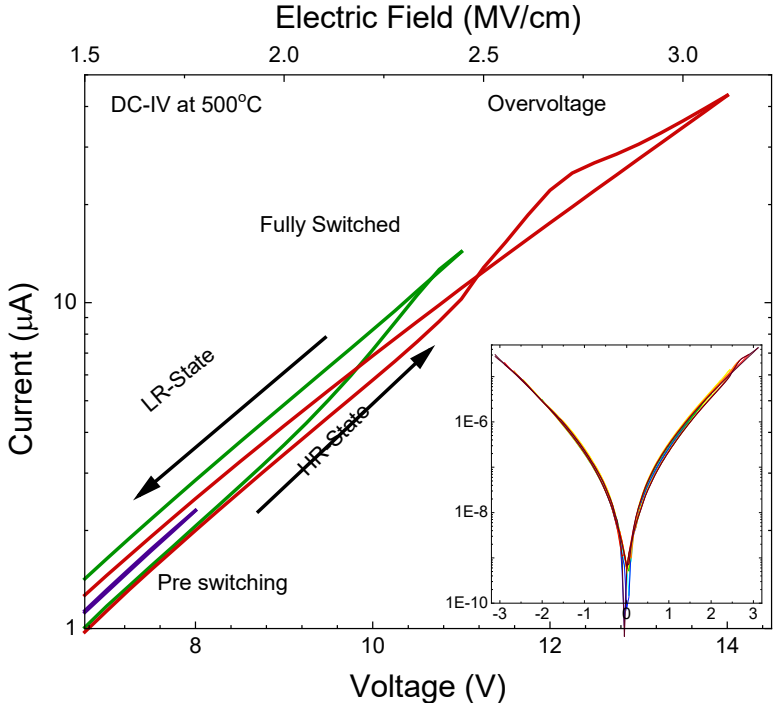
What about these loops?



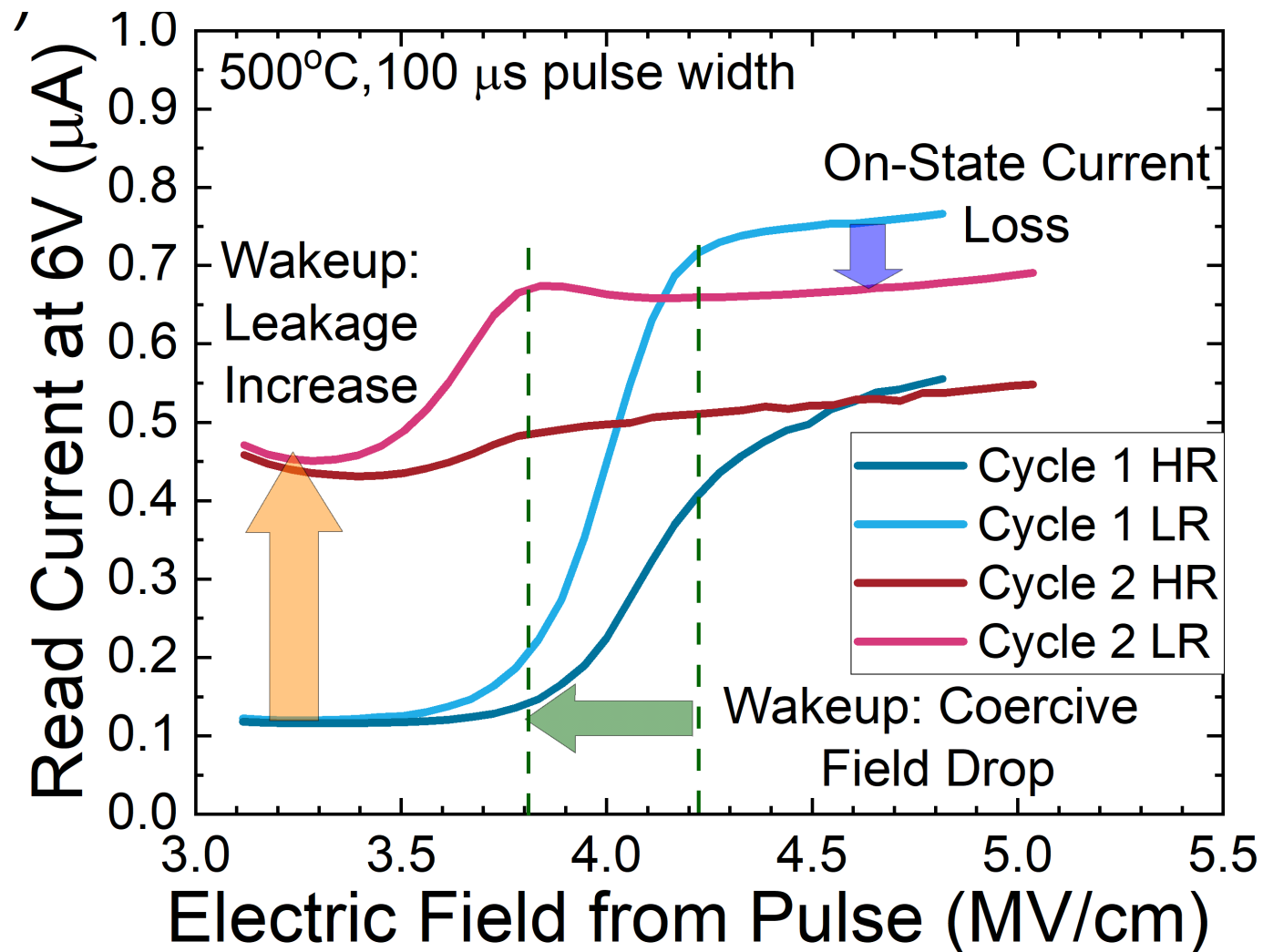
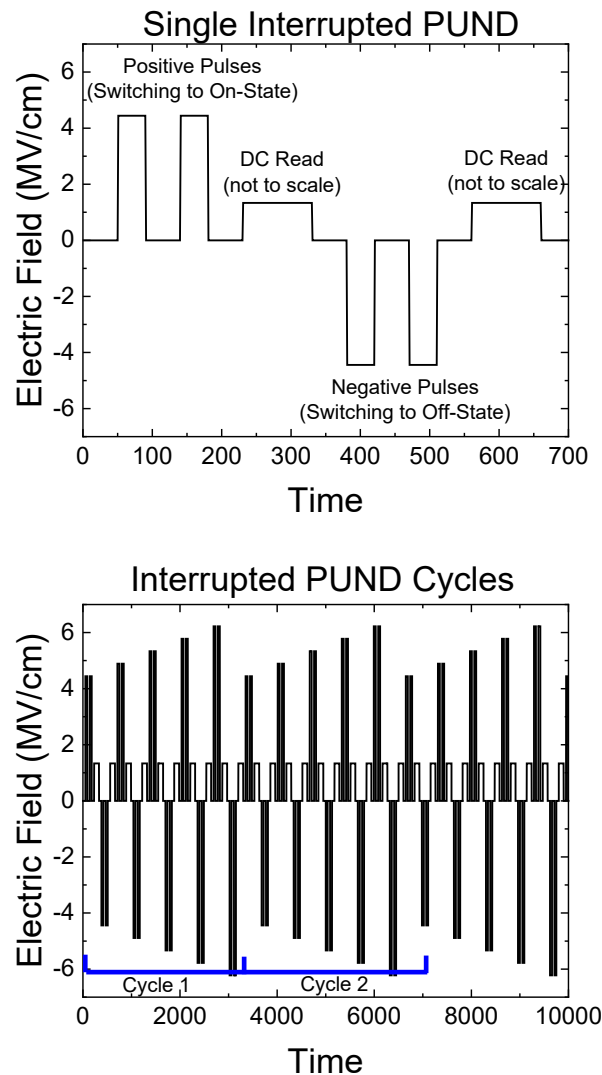
Switching current leech into the DC-IV?



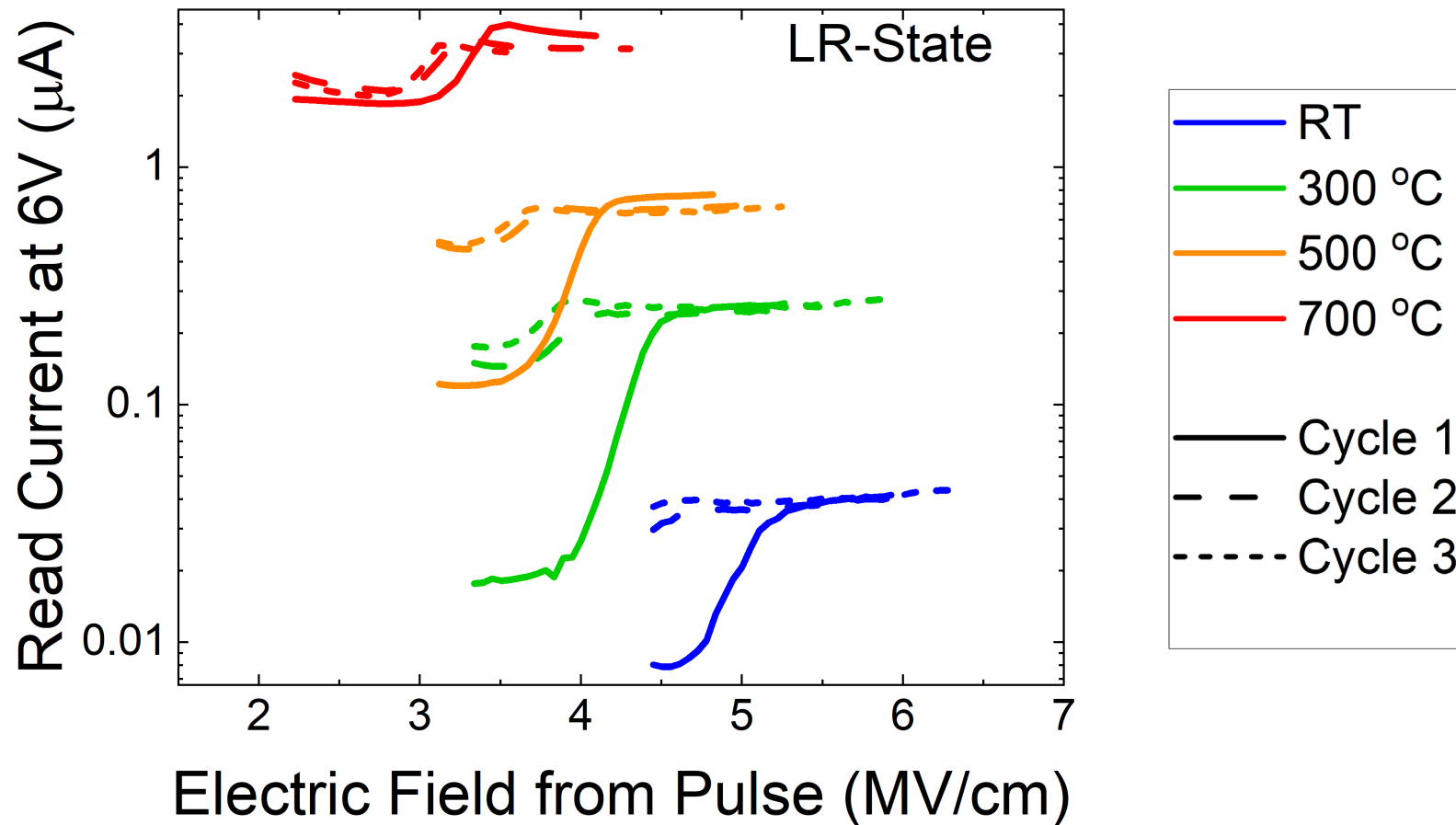
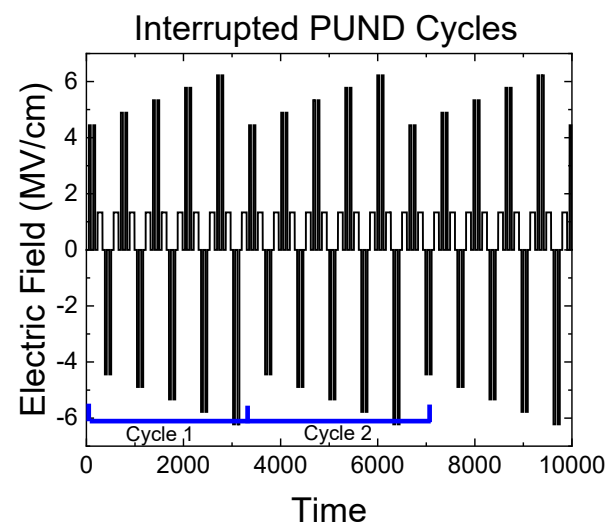
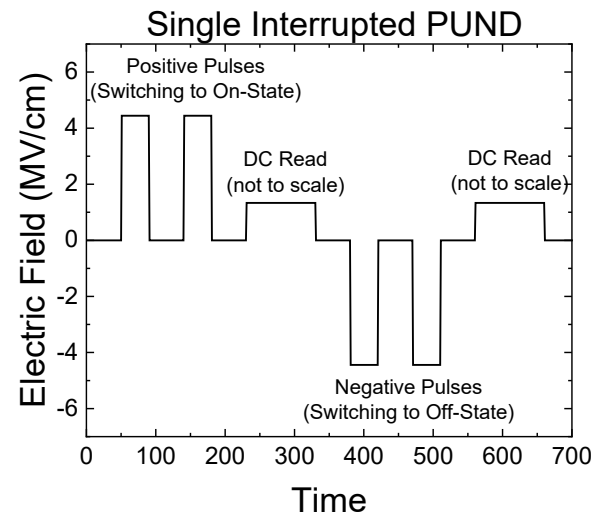
Transitory Device Behavior



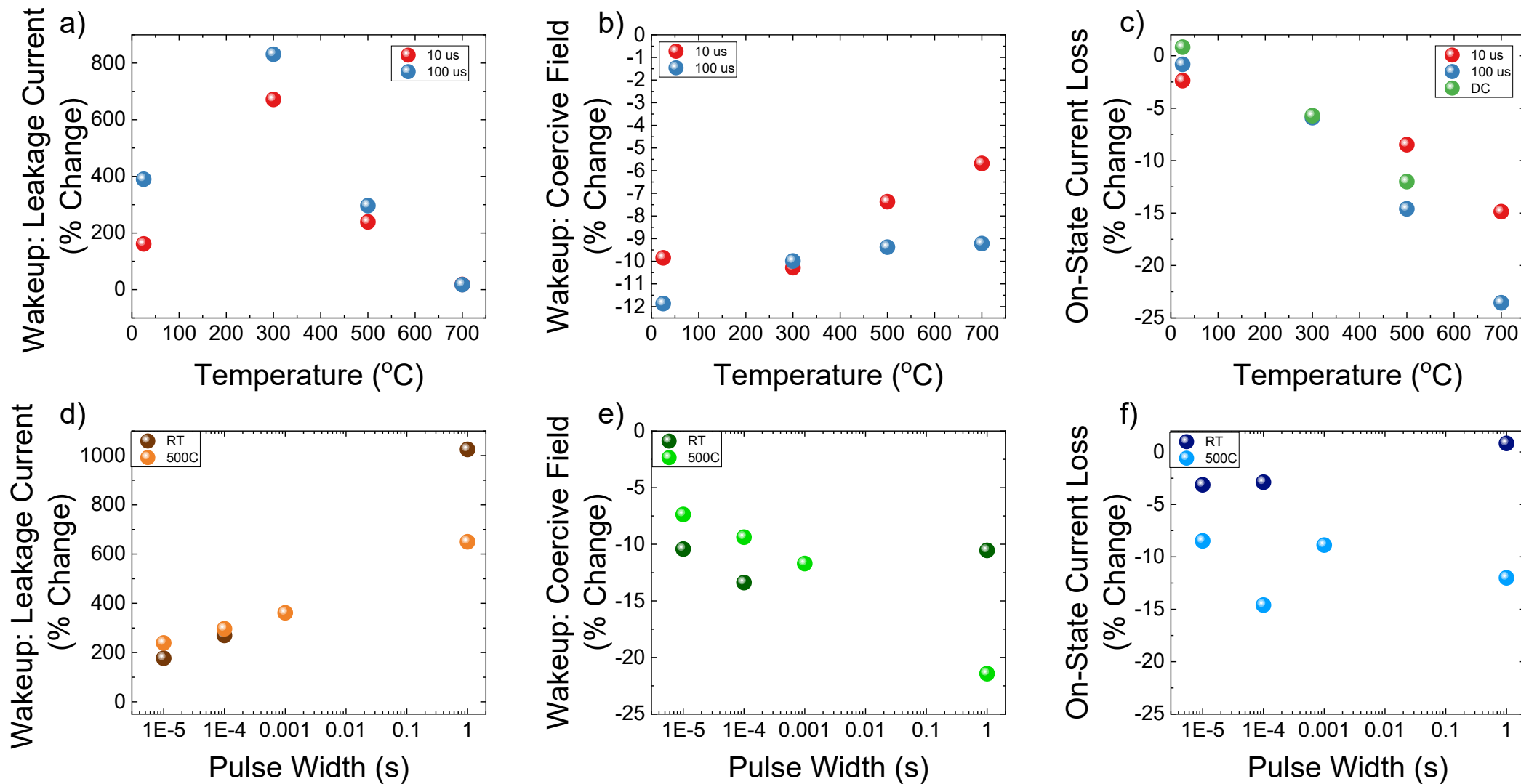
Not Just Wakeup (Though That Hides It)



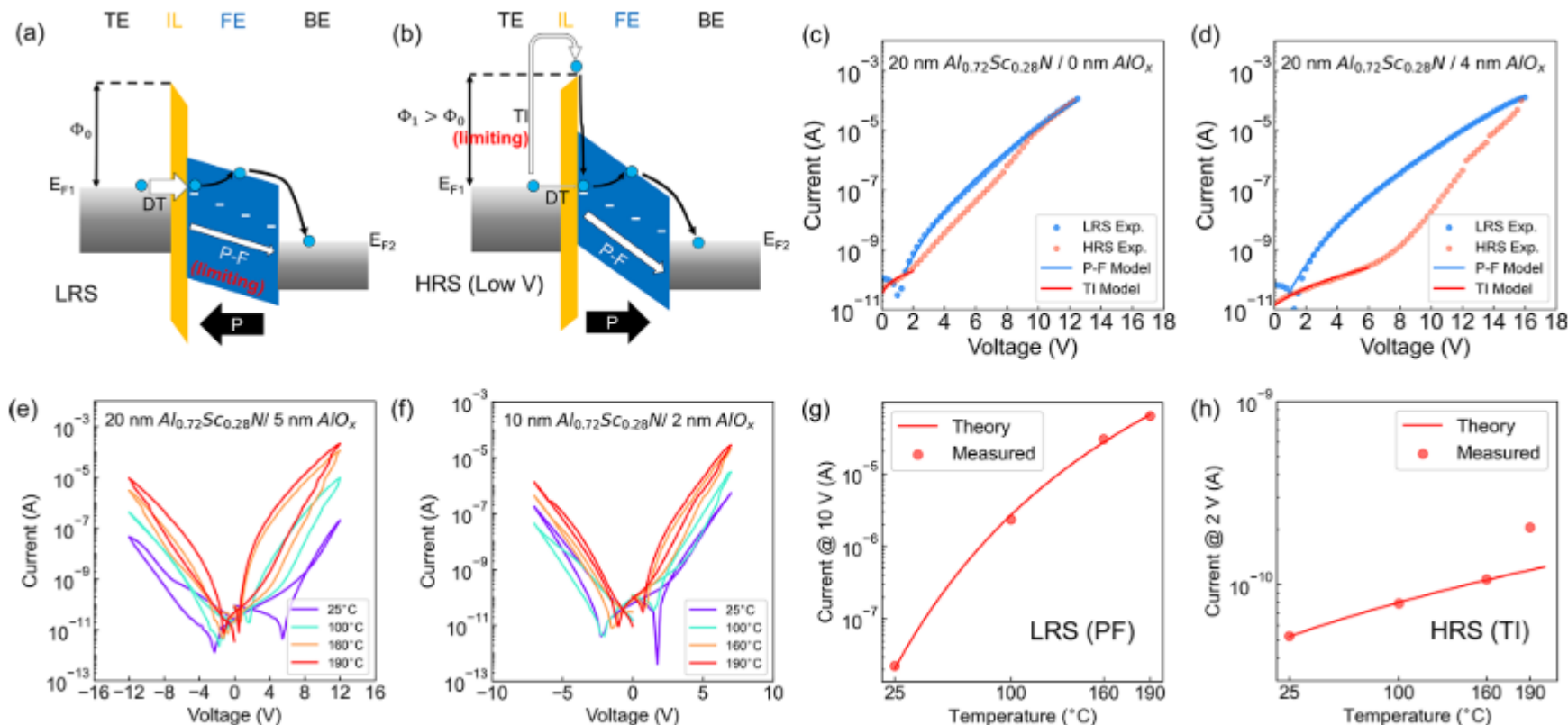
Current Loss Only at High Temperature



Temperature and Time Dependence



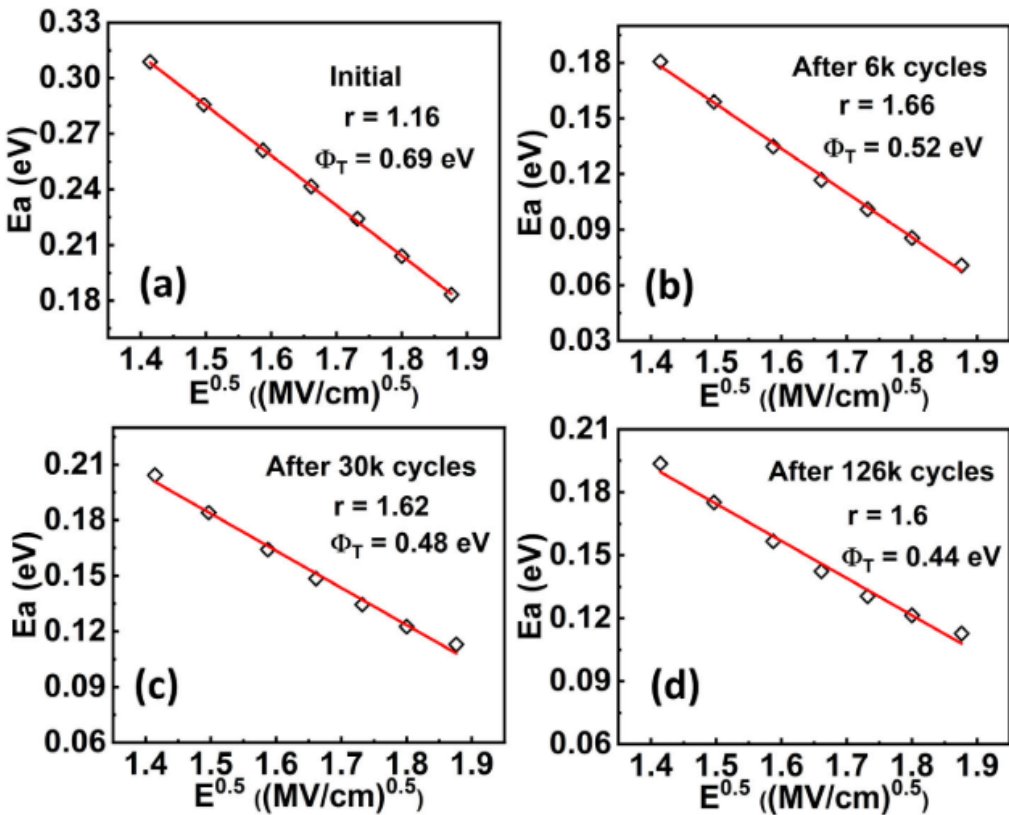
Conduction Mechanisms (Poole Frenkel and Field Assisted Thermionic Emission)



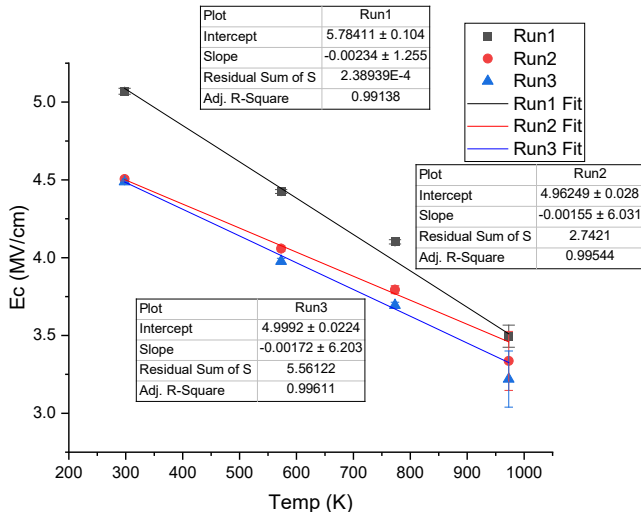
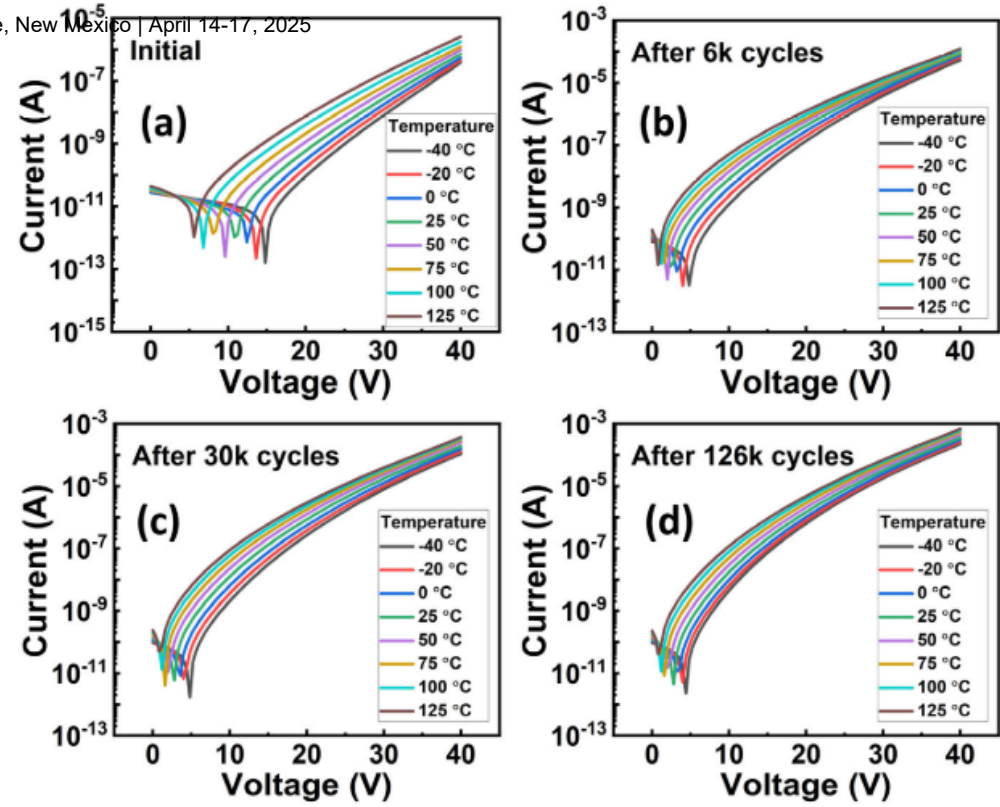
Kim K. *et al.* ACS Nano 2024, 18, 24, 15925–15934



Not Fatigue



Chen, L. *et al.* Leakage Mechanism and Cycling Behavior of Ferroelectric Al_{0.7}Sc_{0.3}N. *Materials (Basel)*. **17**, 397 (2024).

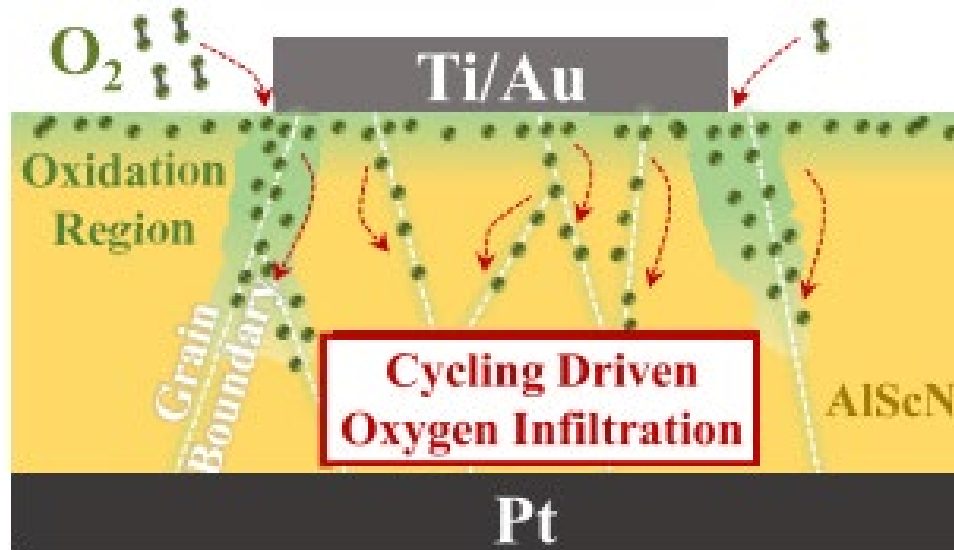


Reduction in activation energy matches literature, but not increase in leakage

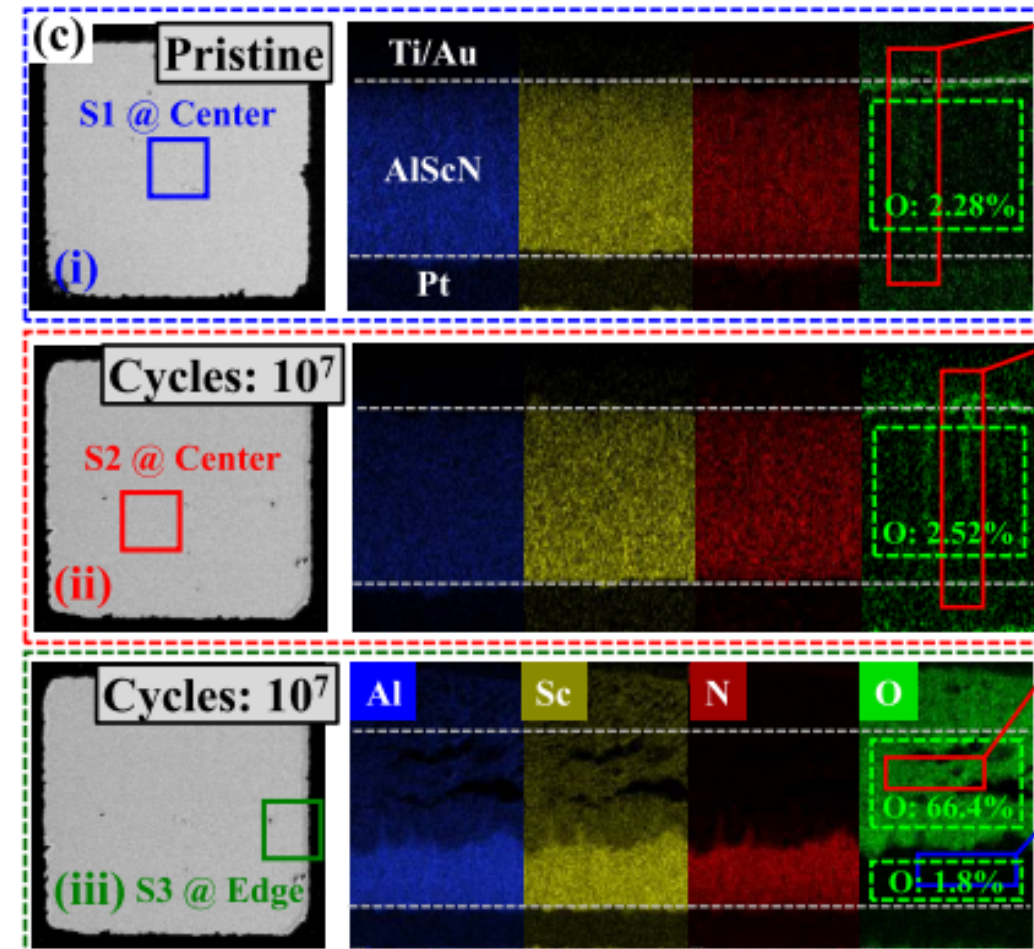
(Reverse?) Field and Temperature Assisted Ion Migration

Not:

- Piezoelectric Stress (should affect E_c)
- Domain Depinning (should increase current)
- Grain Boundary Conduction (should increase leakage)
- Charge trapping/detrapping (should be reversible)



Wang, R. *et al.* *IEEE Electron Device Lett.* **46**, 381–384 (2025).

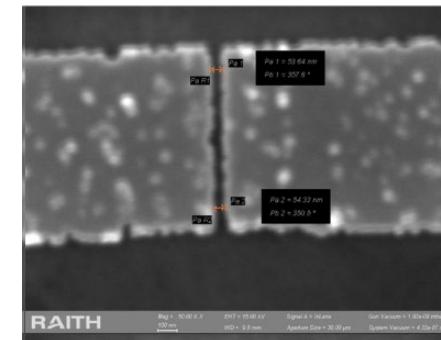
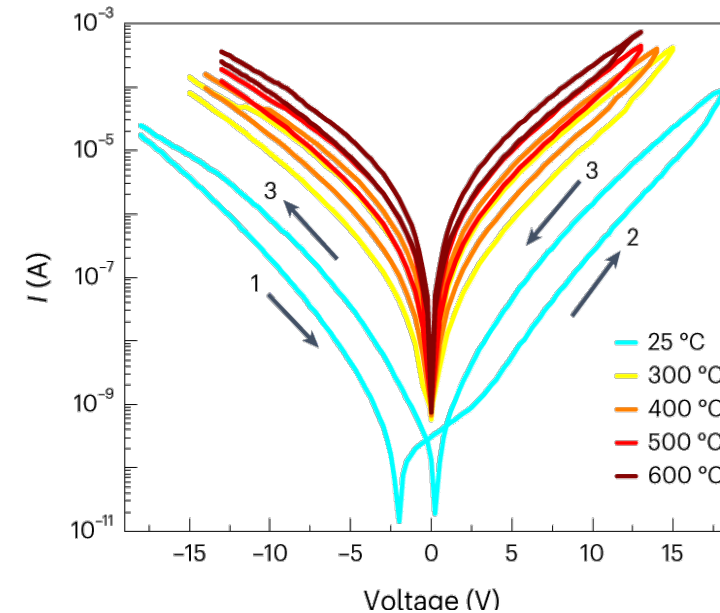


Conclusions

- AlScN NVM demonstrated at 700 °C (1000 °C at UPenn)
- SiC Integration successfully demonstrated
- On/Off Performance Enhanced with Encapsulating Layer
- Consistent fabrication with lateral gaps of 50nm

Future Work:

- Breakdown and transitory mechanisms
- Continue investigating lateral limits
- Optimize performance via fabrication
- Miniaturization of crossbar array (fab and connectivity)





Thank you



Dirhen Pradhan
Yunfei He
Spencer Ware
Yubo Wang
Sizhe Ma
Zekun Hu
Xingyu Du
Deep Jariwala
Troy Olsson



Nicholas Glavin
Joshua Kennedy
Venkata Puli
Mike Newburger
Emmanuel Rowe



Matt Francis,
Jacob Kupernik
Sonia Perez
Nick Chiolino