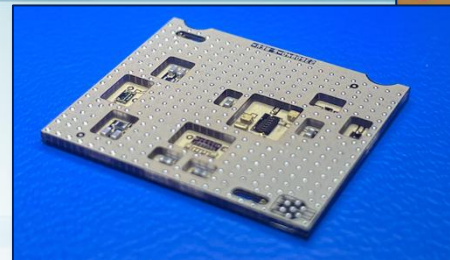
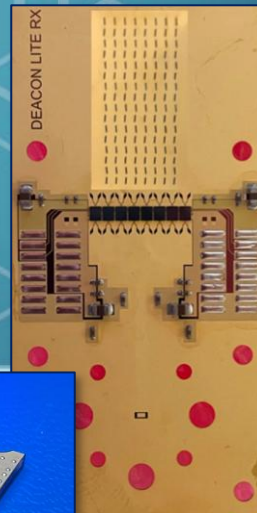
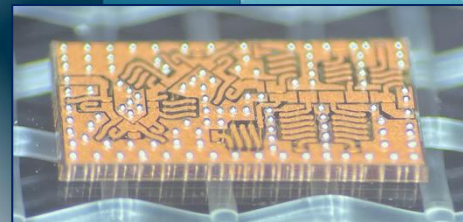




High Temperature Substrate from 3D Glass Solutions

Matt Heidel
Design Engineer at 3D Glass Solutions

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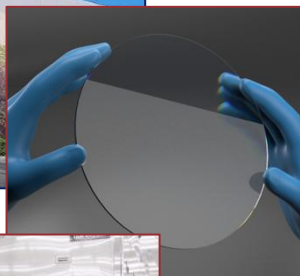




About 3D Glass Solutions

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What do we do and why is it different?



- A provider of advanced electronic packages with substantial Size, Weight, and Power reductions (SWAP) to enable a new generation of electronic devices using glassy materials
- Full turnkey manufacturing: Design → Wafer Fab → Assembly → Test
- Enabling major advancements in:
 - Millimeter wave applications
 - High performance antenna, electronic warfare, counter-electronics
 - High performance computing, silicon photonics and DoD special programs.
- Headquarters and **40,000 Sq. Ft. of advanced manufacturing space** in north Albuquerque, USA.
- Lockheed Martin & In-Q-Tel as major investors and board member
- **Flight legacy on F-35 and IC Satellites**
- ITAR Compliant, ISO:AS9100 qualified, 100% US manufacturing
- Foundational IP, with market leading customer base, and product/results to support world class performance claims

Key drivers: substantially reduced SWAP, RAD hard, high temperature, 3D Heterogeneous Integrated systems-in-package

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- ▶ High temperature applications. For this conversation we focus on temperatures greater than 400°C

- **Energy**

- ▶ Downhole oil and gas
- ▶ Geothermal
- ▶ Generator systems

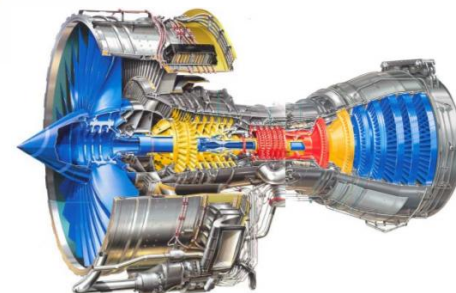
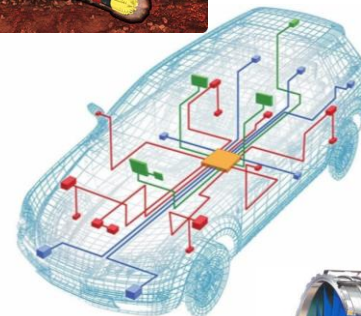
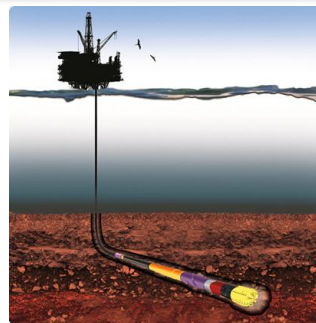
- **Automotive**

- ▶ Under-the-hood electronics
- ▶ Exhaust monitoring
- ▶ Electric vehicle systems

- **Mil-Aero**

- ▶ Avionics
- ▶ Hypersonics
- ▶ Space exploration

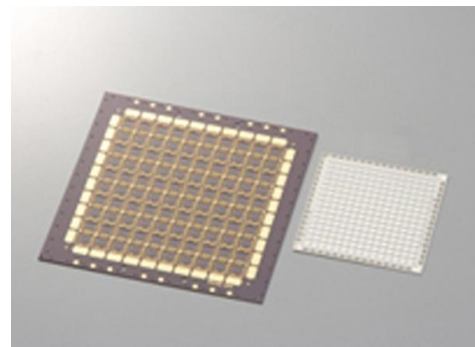
- **Many others**





Challenges in Common High Temperature Substrates

- ▶ **Organic substrates typical to PCBs such as rogers materials**
 - Cannot withstand 400°C dependably
- ▶ **Common HTCC and LTCC substrates**
 - Lower CTEs create stresses with conductor layers and assembly materials
 - Substrate shrinkage of 10-15%
 - Line/space limiting restrictions for electrical traces 100/100 typ
 - Conductor material limitations like refractory metals
 - Other material compatibility issues for integrated passive devices
 - RF properties for frequency applications
 - Through substrate vias must be laser drilled to $30 \pm 10 \mu\text{m}$ or larger
 - No substrate cavities
 - No 3D heterogeneous integration
- ▶ **3DGS high temp ceramic provides unique material properties, processing capabilities, and scalability potential.**

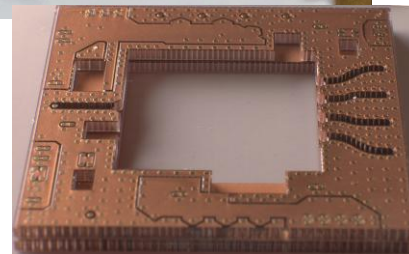




Why 3DGS Photopatternable Glass Ceramic?

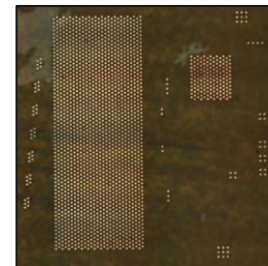
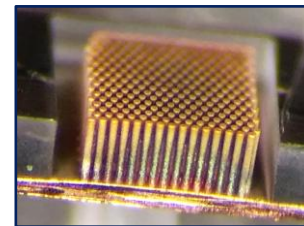
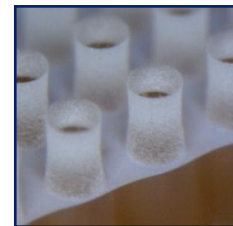
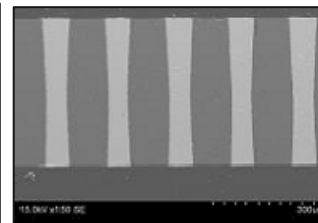
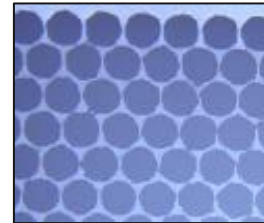
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- ▶ Ceramic phase is a typical conversion of 3DGS mainstay substrate.
- ▶ Stable up to 500°C
- ▶ Non-toxic and radiation stable.
- ▶ Mechanical, shock, and vibe durability
- ▶ CTE of 6.7ppm/K from 20 to 500°C
- ▶ Simultaneous photopatterning of through vias down to $25 \pm 2 \mu\text{m}$ diameter
- ▶ Cu conductor layers down to 10/10 μm line/space
- ▶ Good RF properties for high frequency applications Dk of 5.8 supported by cavity features
- ▶ RF properties can be augmented with through substrate cavities enabling air filled waveguide structures, embedded die packaging and more.
- ▶ 3D heterogeneous integrations capabilities allow for System In Package design for reduction in size mass and power consumption



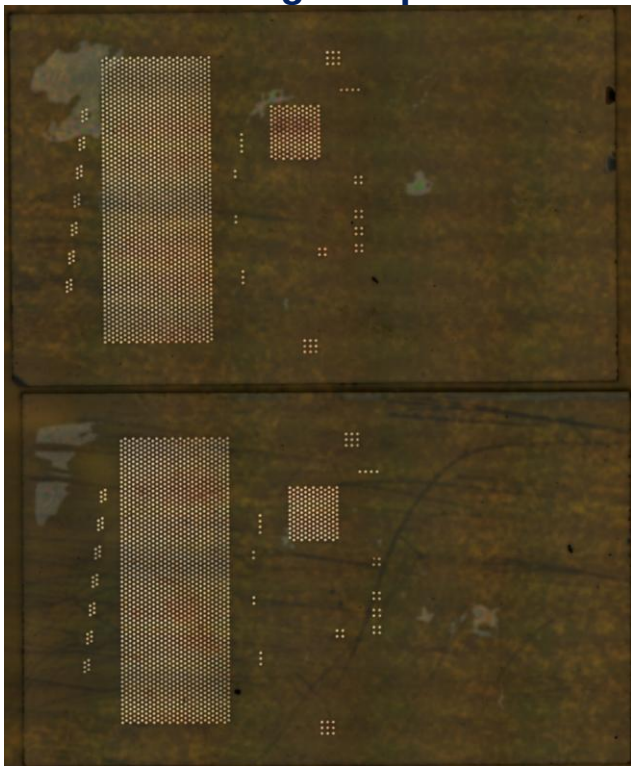


- ▶ Use of an inexpensive wet etch process for 3D glass structuring:
 - Lithography defined patterning means vias of all different sizes, shapes and quantities are formed in the same quick process step.
- ▶ Defined by aspect ratio of diameter and thickness
 - Via diameters as low as $25\mu\text{m}$ and as large as $100\mu\text{m}$
 - Via pitch as low as $50\mu\text{m}$
- ▶ Highly cylindrical profile
 - Less than 3° taper on via wall angles maintains consistent diameter through the substrate
- ▶ Solid copper filled vias
 - Vias filled with solid 99% pure copper allowing for high electrical and thermal conductivity
- ▶ High density via arrays for thermal management
 - Regions can be designed with thermal transfer greater than 90W/mK

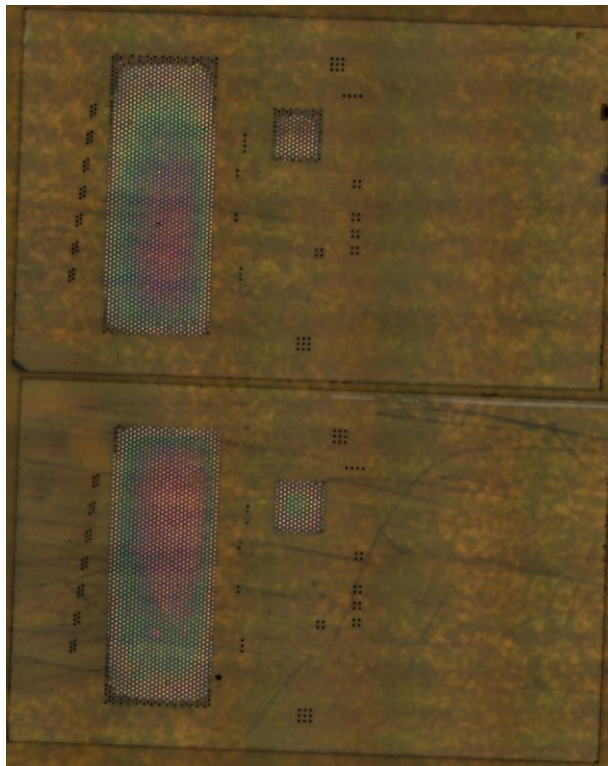




Starting Samples



20x 250C Reflows



- ▶ 40µm diameter vias on 80µm pitch
- ▶ Effective Thermal Transfer = $\sim 90\text{W/mK}$
- ▶ No glass cracking
- ▶ No TGV cracking
- ▶ Oxidation due to TGVs being exposed copper



The Power of Cavities

Mini-Faraday Cages

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Cavities perform several important functions

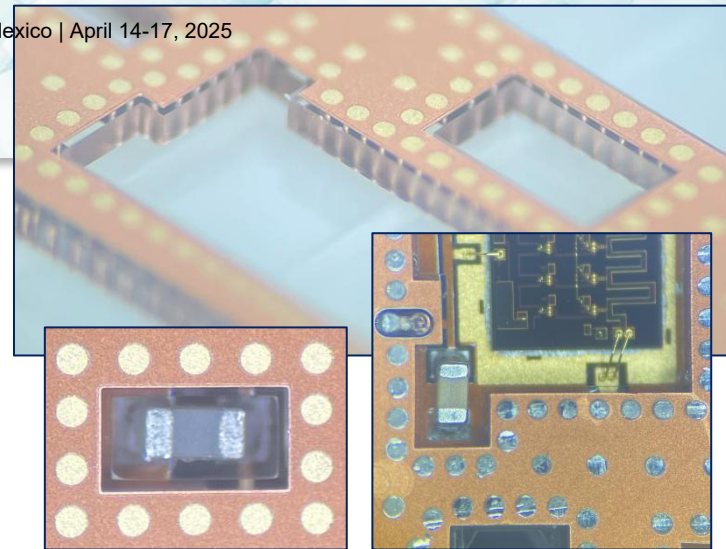
► Embedding ICs

- Cavities provide space for embedded die and their electrical connections (e.g. wire bonds) to exist between layers
- Complex shapes and outlines are easily produced
- Minimum cavity size = $200\mu\text{m} \times 400\mu\text{m}$ enables the isolation of even the smallest SMT parts

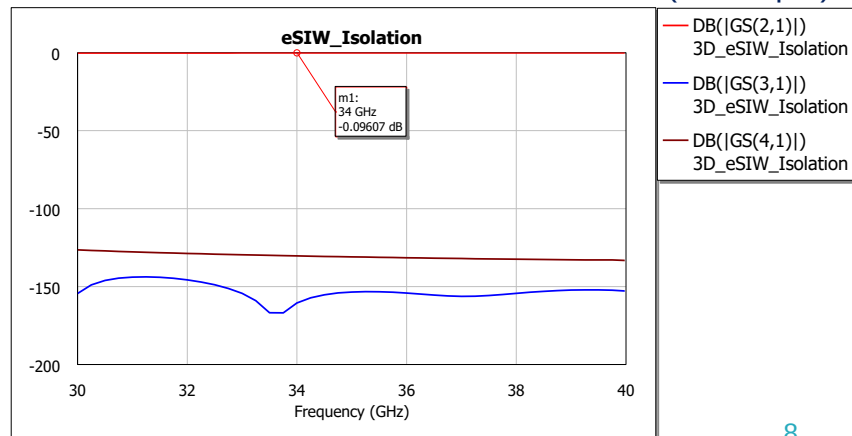
► High isolation

- They provide 6-sided isolation to adjacent chips with TGV ground fence along edge of cavities to form micro-Faraday cages.
- Achieve up to 60dB of isolation between adjacent cavities spaced only $300\mu\text{m}$ apart

► Metal etch stop can also be included on one side of cavity to form a lid, fully enclosing the cavity



Simulated Isolation with three rows of TGVs ($60/120\mu\text{m}$)





90GHz eSIW Reference Design (Back-to-Back Test)

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eSIW are unique structures to 3DGS processing that involve minimal process modifications.

Top View

Back View

X-Ray

Waveguide Launch

Glass Parameter

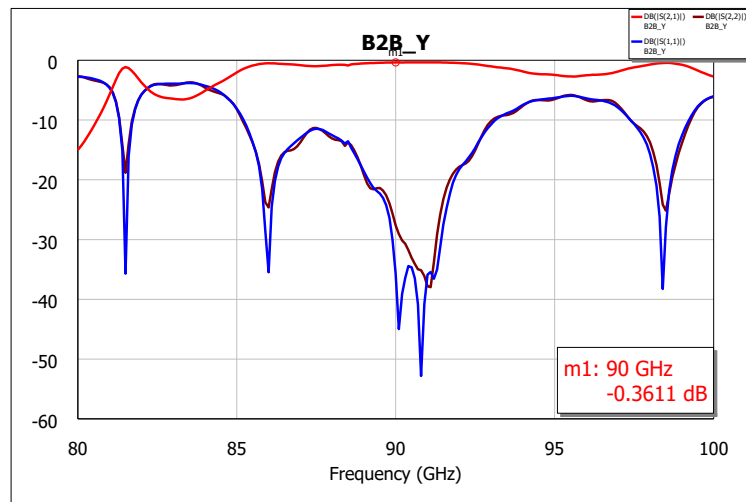
Y-Splitter

Air Cavity

Waveguide Launch

TGVs (black dots)

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	SIM (dB)	MEAS.(dB)
Full B2B-Y	0.209	0.361
eSIW-WR10 (ea.)	0.093	0.110
B2B-Y / 2 cm	0.023	0.140



Connecting Glass Layers

RF 3DHI – High Frequency Performance

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KEYSIGHT

cadence

AWR
RF/MICROWAVE
DESIGN SOFTWARE

Create low-loss high frequency
controlled impedance transitions
between glass layers

CPWG

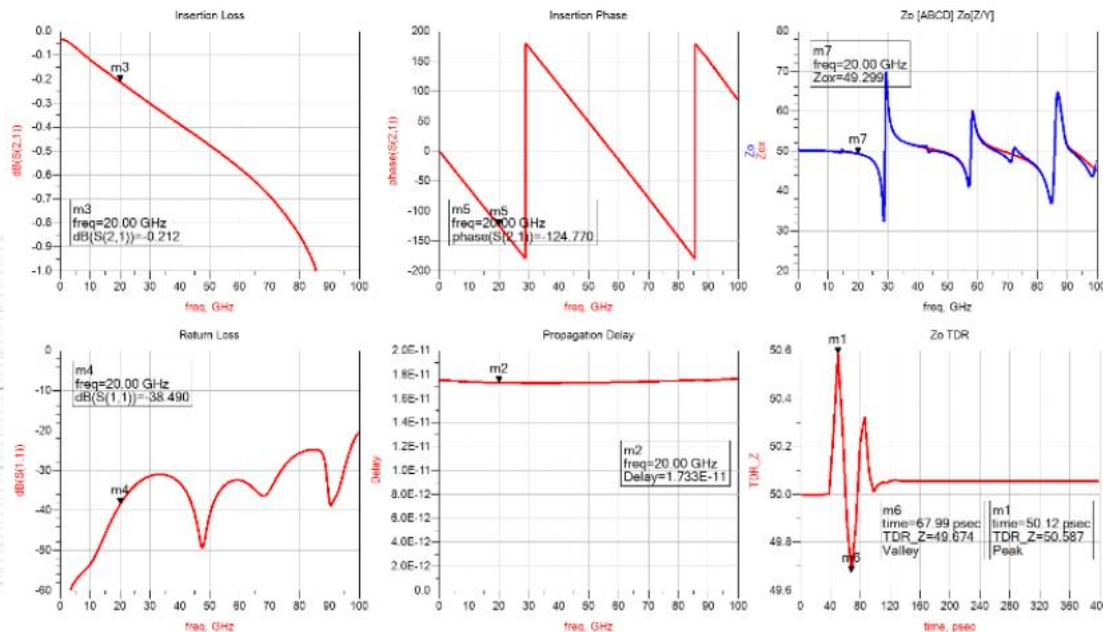
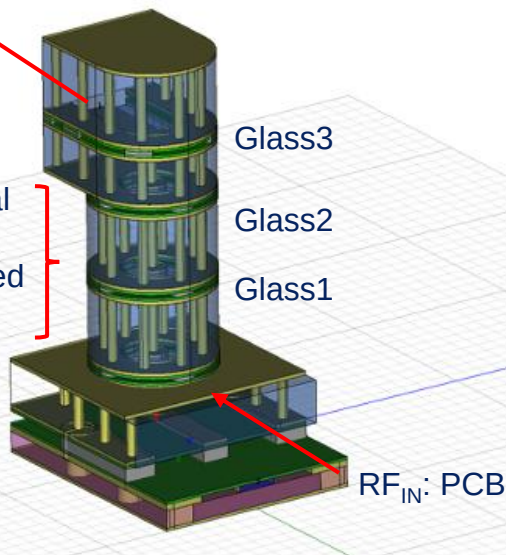
- RF trace = 160um
- Space = 67um

Silver

- Diameter = 120um
- Height = 50um

RF_{OUT}: Glass 4

Center signal
and ground
vias optimized
for 50Ω

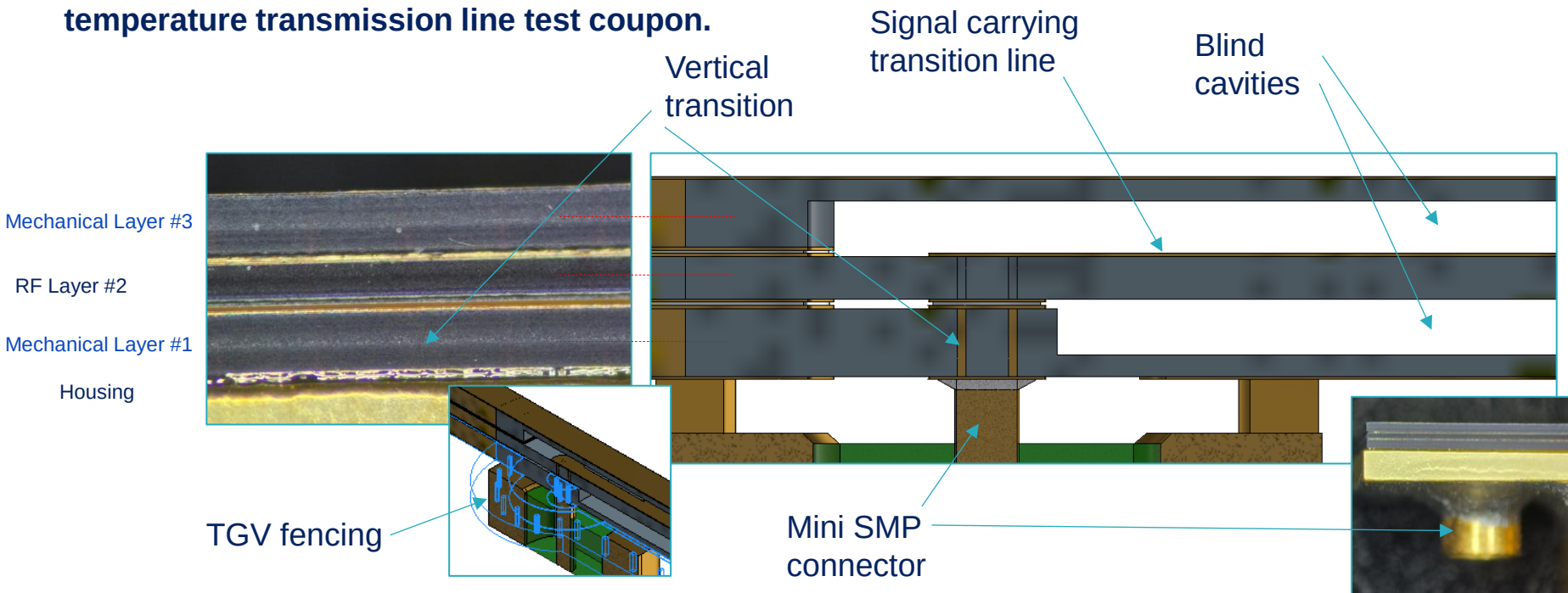


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Transmission Line Test Structure

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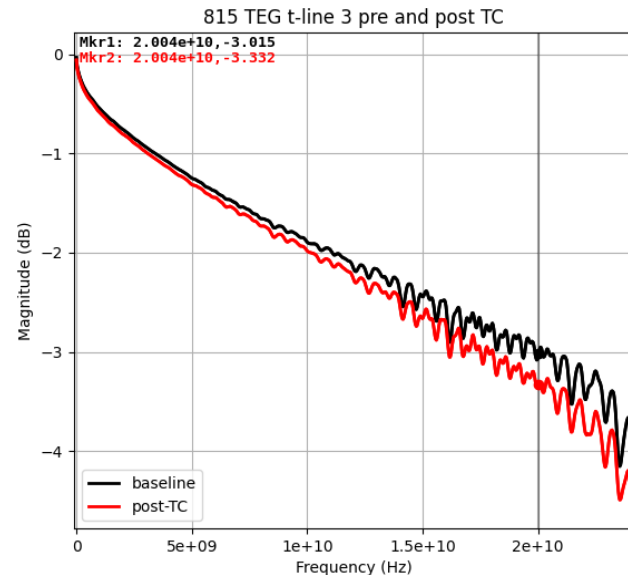
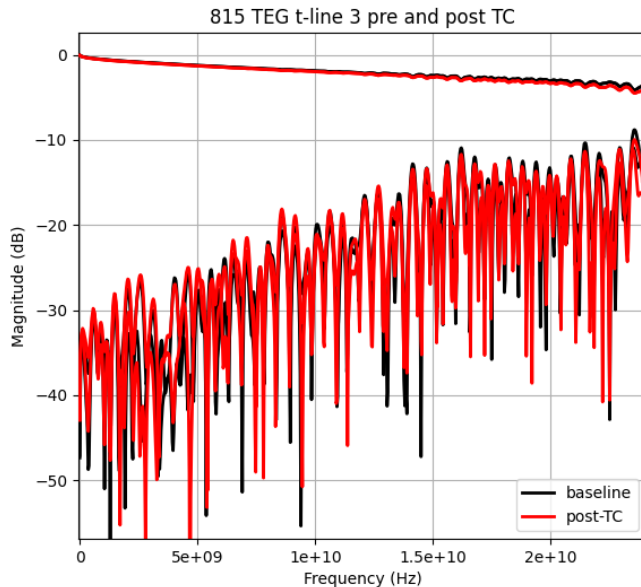
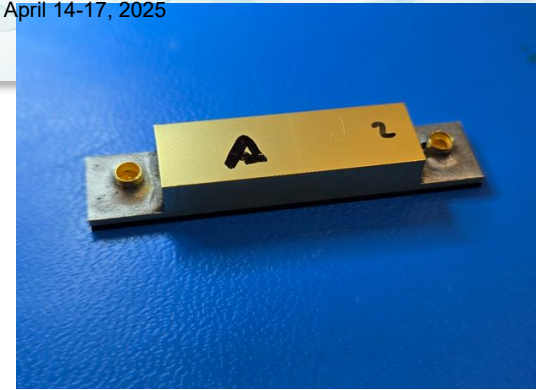
The building blocks mentioned before can come together to form structures like this high temperature transmission line test coupon.



Transmission Line Test Structure

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- ▶ 4mm transmission line length
- ▶ Ramp rate: 133°C/ min
- ▶ Hold at 500°C for 10 minutes
- ▶ Test fixture has not been de-embedded and makes up a significant portion of the loss and reflection in these graphs





- The world needs high temp electronics, and many industries need them faster, cheaper, and hotter than it can currently get them
- 3DGS has developed and demonstrated a simple way to convert our primary photo patternable glass ceramic substrate into its ceramic phase and thus enable it to withstand temperatures up to 500°C.
- This method is compatible with many of the unique structures and processing methods that 3DGS offers to allow for advanced packaging and RF solutions.
- Our understanding of the possibilities and limitations of this technology will continue to grow and we look forward to finding out more alongside our friends and partners in industry and academia.



▶ Thank You