



# IMAPS APPE/CICMT/HiTEC



## Memory Phenomenon of GaN pn Junction by Engineering Its Interface, Which is Stable at High Temperatures up to 500 C

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# Outline

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- GaN for High-temperature applications
- GaN resistive switching memory status
- **Discovery** of memory behavior in GaN p-n diodes
- **Mechanism** for the threshold switching behavior
- **Enhanced GaN memory behavior** up to 500 C
- Summary

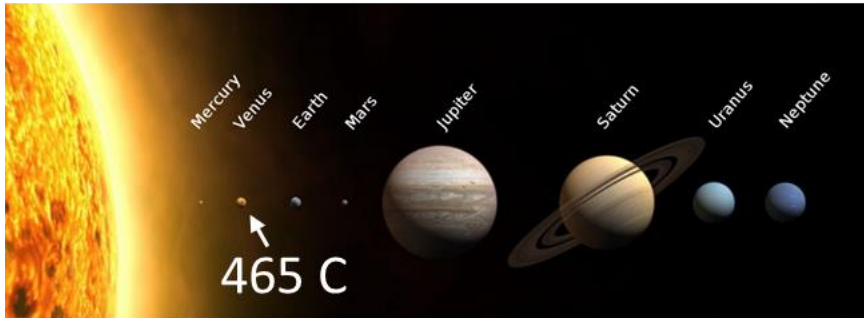
# High Temperature Applications



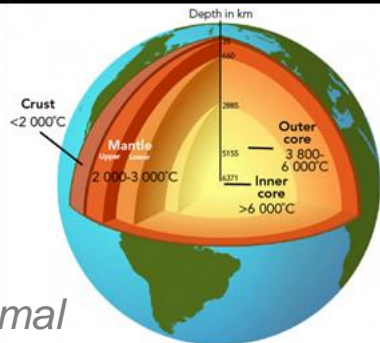
automotive



aircraft engine



space exploration



Geothermal

**TABLE 6.1** Semiconductor Technologies for Some Selected High-Temperature Electronics Applications

High-Temperature Electronics Application	Peak Ambient ( $^\circ\text{C}$ )	Chip Power (kW)	Current Technology	Future Technology
<b>Automotive</b>				
Engine control electronics	150	<1	BS and SOI	BS and SOI
On-cylinder and exhaust pipe	600	<1	NA	WBG
Electric suspension and brakes	250	>10	BS	WBG
Electric/hybrid vehicle	150	>10	BS	WBG
<b>Turbine engine</b>				
Sensors, telemetry, control	300	<1	BS and SOI	SOI and WBG
	600	<1	NA	WBG
Electronic actuation	150	>10	BS and SOI	WBG
	600	>10	NA	WBG
<b>Spacecraft</b>				
Power management	150	>1	BS and SOI	WBG
	300	>10	NA	WBG
Venus and mercury exploration	550	~1	NA	WBG
<b>Industrial</b>				
High-temperature processing	300	<1	SOI	SOI
	600	<1	NA	WBG
<b>Deep-well drilling telemetry</b>				
Oil and gas	300	<1	SOI	SOI and WBG
Geothermal	600	<1	NA	WBG

Source: Neudeck, P.G. et al., *Proc. IEEE*, 90(6), 1065. © 2002 IEEE.

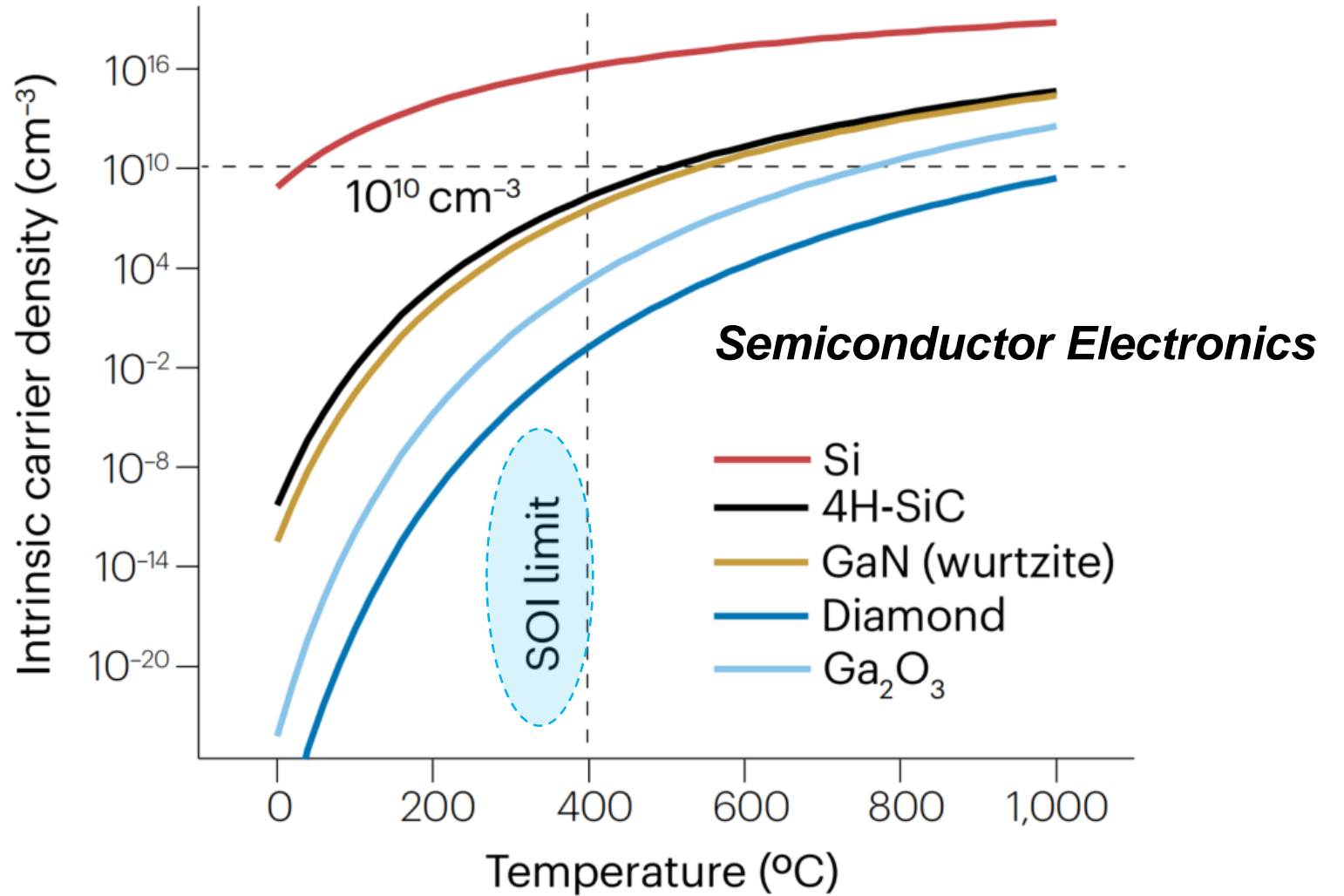
BS, Bulk silicon; SOI, silicon-on-insulator; NA, not presently available; WBG, wide bandgap.

John D. Cressler, H. Alan Mantooth, *Extreme Environment Electronics*, 2013 by Taylor & Francis Group

# GaN for High Temperature Applications

## Intrinsic Carrier Density

$$n_i = \sqrt{N_c N_v} e^{-E_g/2kT}$$



Pradhan, D.K., Moore, D.C., Francis, A.M. et al. Materials for high-temperature digital electronics. Nat Rev Mater 9, 790–807 (2024)

# GaN for High Temperature Applications

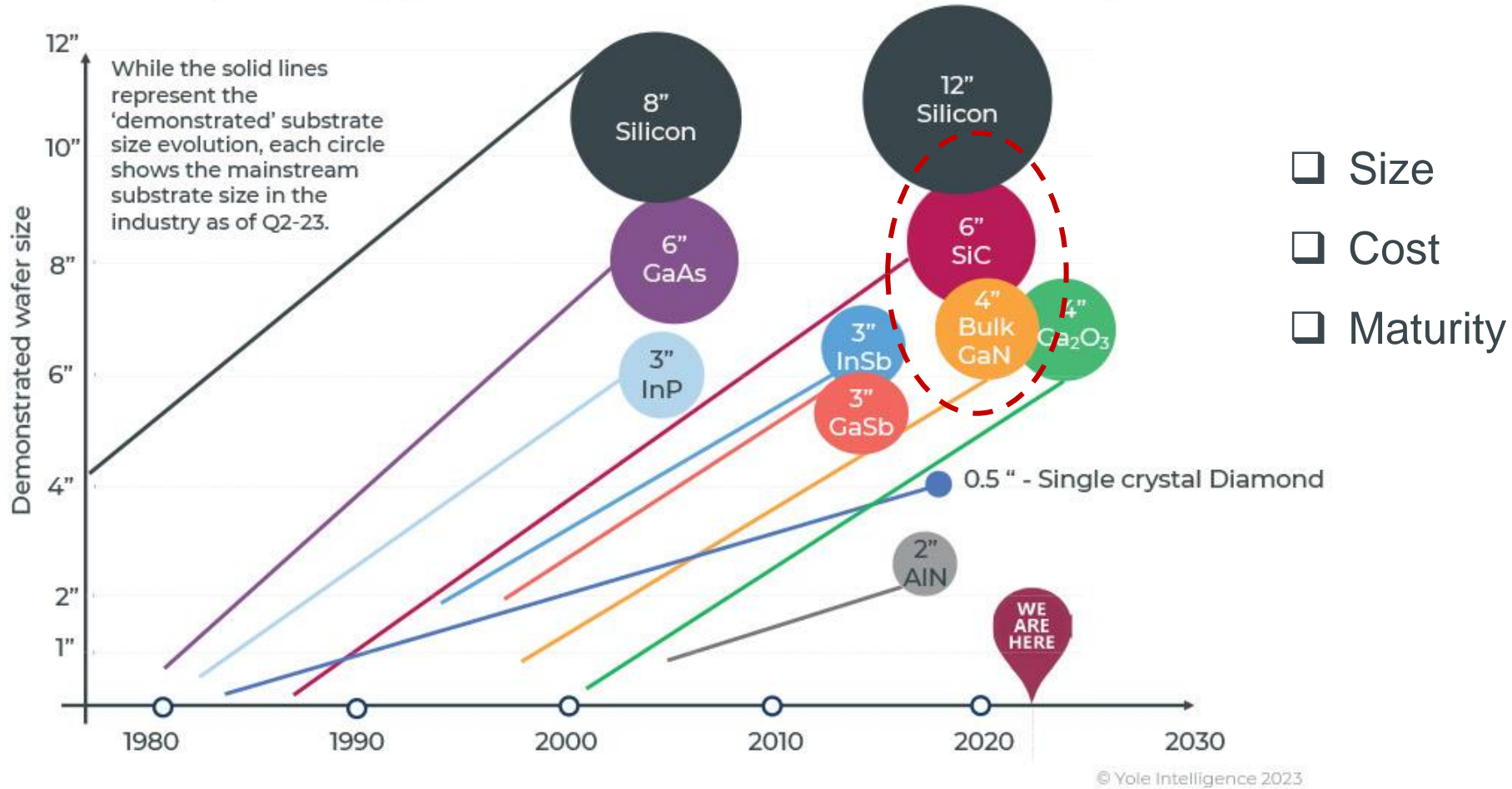
Materials parameters	Si	GaAs	4H-SiC	GaN	Diamond	$\beta$ -Ga <sub>2</sub> O <sub>3</sub>	Comments
Bandgap, $E_g$ (eV)	1.1	1.43	3.25	3.4	5.5	4.85	Bandgap of Ga <sub>2</sub> O <sub>3</sub> reported in range 4.6–4.9 eV
Dielectric constant, $\epsilon$	11.8	12.9	9.7	9	5.5	10	
Breakdown field, $E_C$ (MV/cm)	0.3	0.4	2.5	3.3	10	8	Experimental values for Ga <sub>2</sub> O <sub>3</sub> have reached ~0.5 times the theoretical maximum
Electron mobility, $\mu$ (cm <sup>2</sup> /Vs)	1480	8400	1000	1250	2000	300	
Saturation velocity, $v_s$ (10 <sup>7</sup> cm/s)	1	1.2	2	2.5	1	1.8-2	1.8 $\langle 001 \rangle$ and $\langle 010 \rangle$ , 2.0 $\langle 010 \rangle$
Thermal conductivity $\lambda$ (W/cm K)	1.5	0.5	4.9	2.3	20	0.1–0.3	0.13 $\langle 100 \rangle$ , 0.23 $\langle 010 \rangle$
Figures of merit relative to Si							
Johnson = $E_C^2 \cdot V_s^2 / 4\pi^2$	1	1.8	278	1089	1110	2844	<u>Power-frequency capability</u>
Baliga = $\epsilon \cdot \mu \cdot E_C^3$	1	14.7	317	846	24 660	3214	Specific <u>on-resistance</u> in (vertical) drift region
Combined = $\lambda \cdot \epsilon \cdot \mu \cdot V_s \cdot E_C^2$	1	3.7	248.6	353.8	9331	37	Combined power/frequency/voltage
Baliga high frequency = $\mu \cdot E_C^2$	1	10.1	46.3	100.8	1501	142.2	Measure of <u>switching losses</u>
Keyes = $\lambda \cdot [(c \cdot V_s) / (4\pi \cdot \epsilon)]^{1/2}$	1	0.3	3.6	1.8	41.5	0.2	<u>Thermal capability</u> for power density/speed
Huang HCAFOM, $\epsilon \mu^{0.5} E_C^2$	1	5	48	85	619	279	Huang chip area manufacturing FOM

Pearton et al. , Appl. Phys. Rev. 5, 011301 (2018)

# GaN for High Temperature Applications

## 1980-2023 different crystals' diameter expansion history

(Source: Emerging Semiconductor Substrates 2023, Yole Intelligence, June 2023)

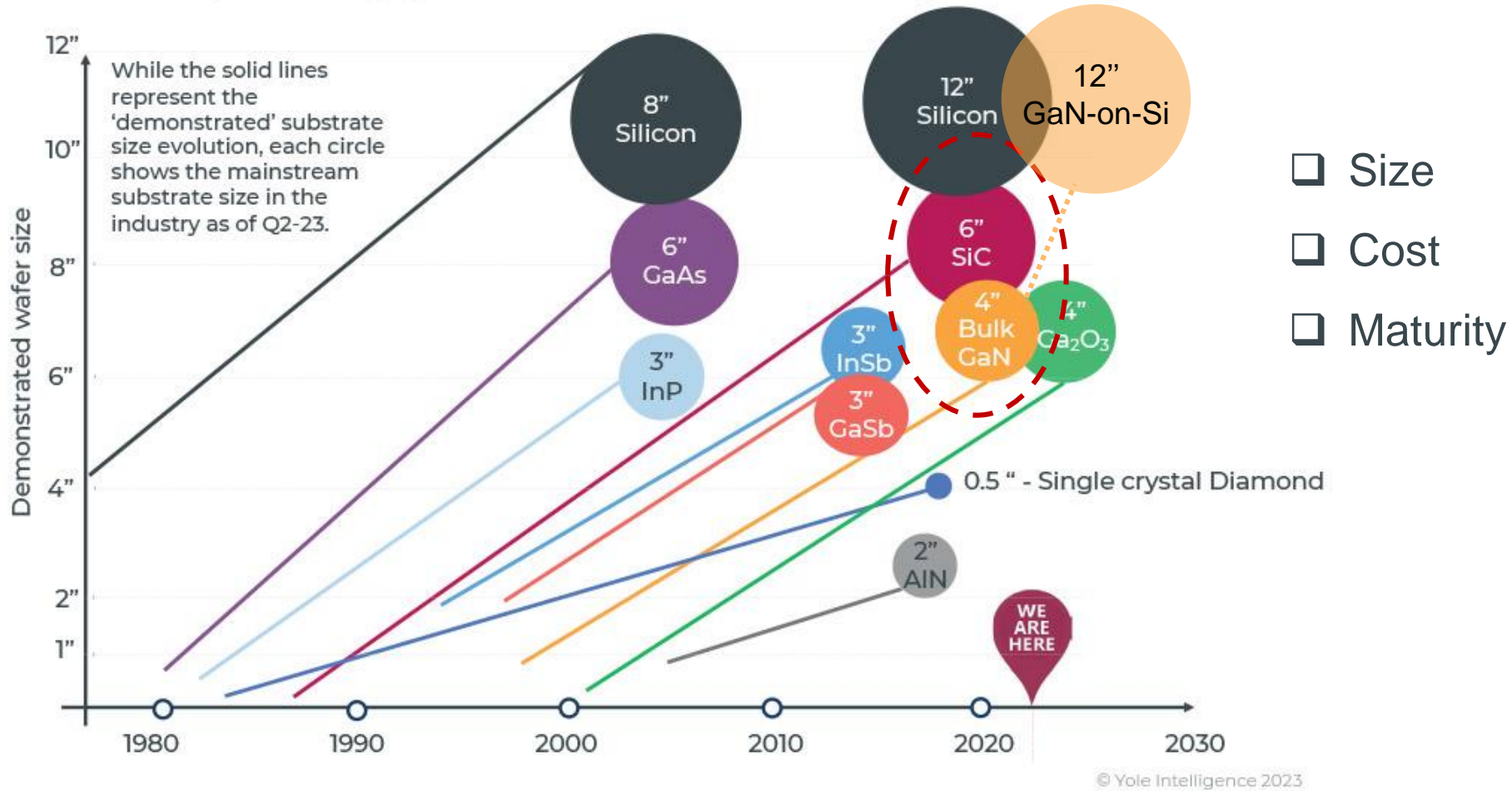


[https://www.semiconductor-today.com/news\\_items/2023/jun/yole-210623.shtml](https://www.semiconductor-today.com/news_items/2023/jun/yole-210623.shtml)

# GaN for High Temperature Applications

## 1980-2023 different crystals' diameter expansion history

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# Unique Potential of GaN Electronics and Photonics

## Photonics / Optoelectronics

- Lighting and Display
- Auto Headlights
- Photovoltaics
- Photodetectors



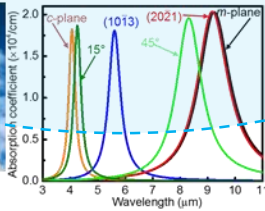
LED



Laser



Solar Cells



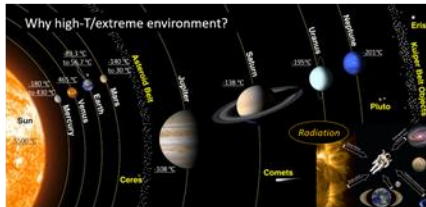
Detectors

## Smart Applications

- Plant Growth
- Visible Light Communication
- Biomedical



Li-Fi



Why high-T/extreme environment?

## Power Electronics

- AC/DC
- DC/DC
- inverter
- EV



**GaN**  
(Al, B, In, Ga)<sup>N</sup>

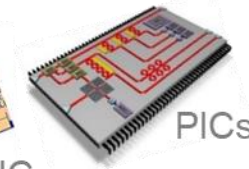
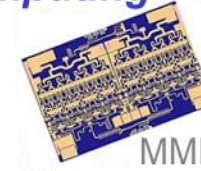
## RF communication

- 5G, sub-THz



## Processor / Computing

- Power ICs,
- PICs, Sensing

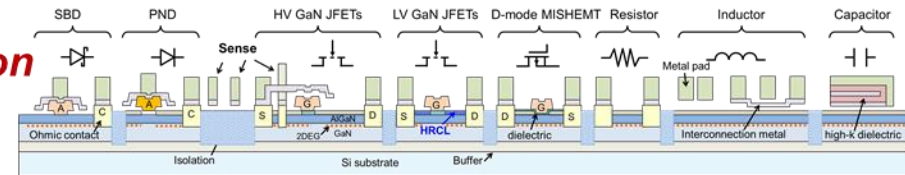


MMIC

PICs

## High Temperature, Radiation

- Space exploration
- turbine
- Deep-well drilling
- X-ray

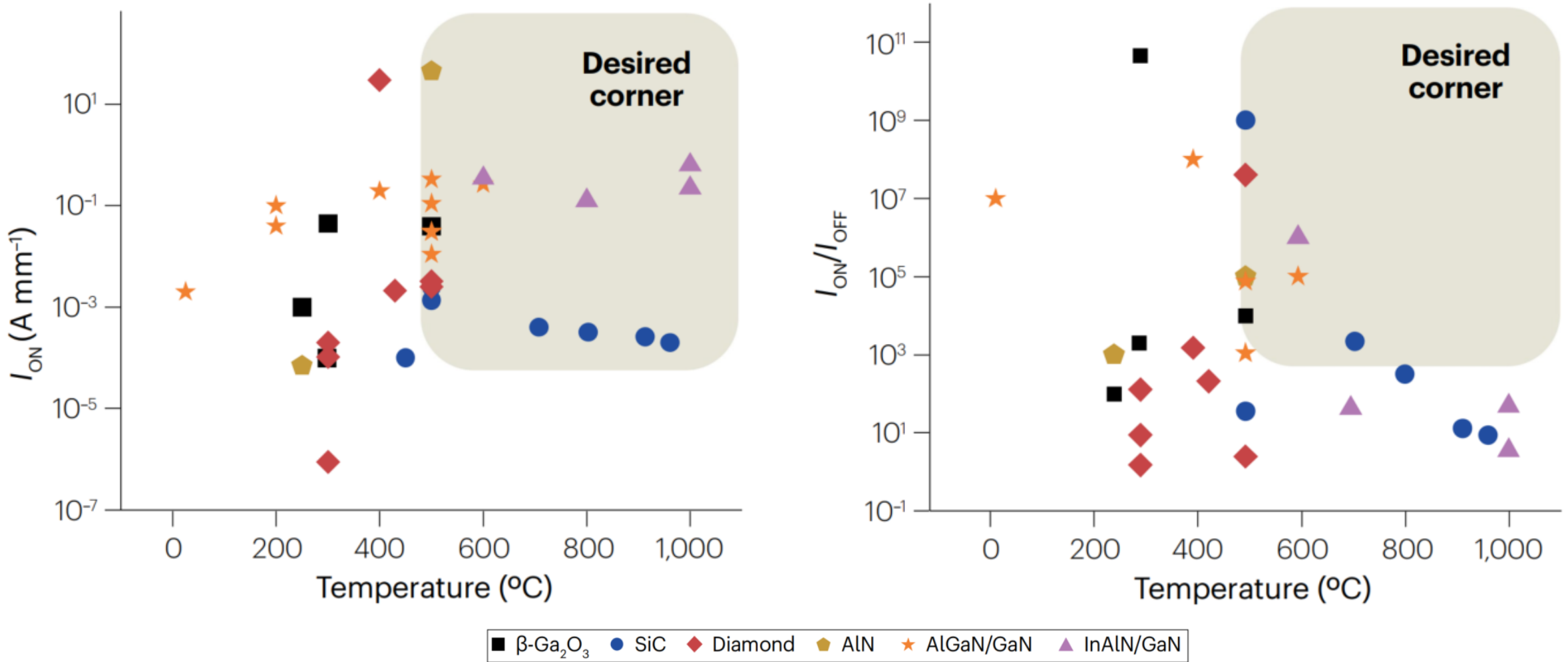


GaN: Discrete device → Integrated Circuits

Everything in one chip

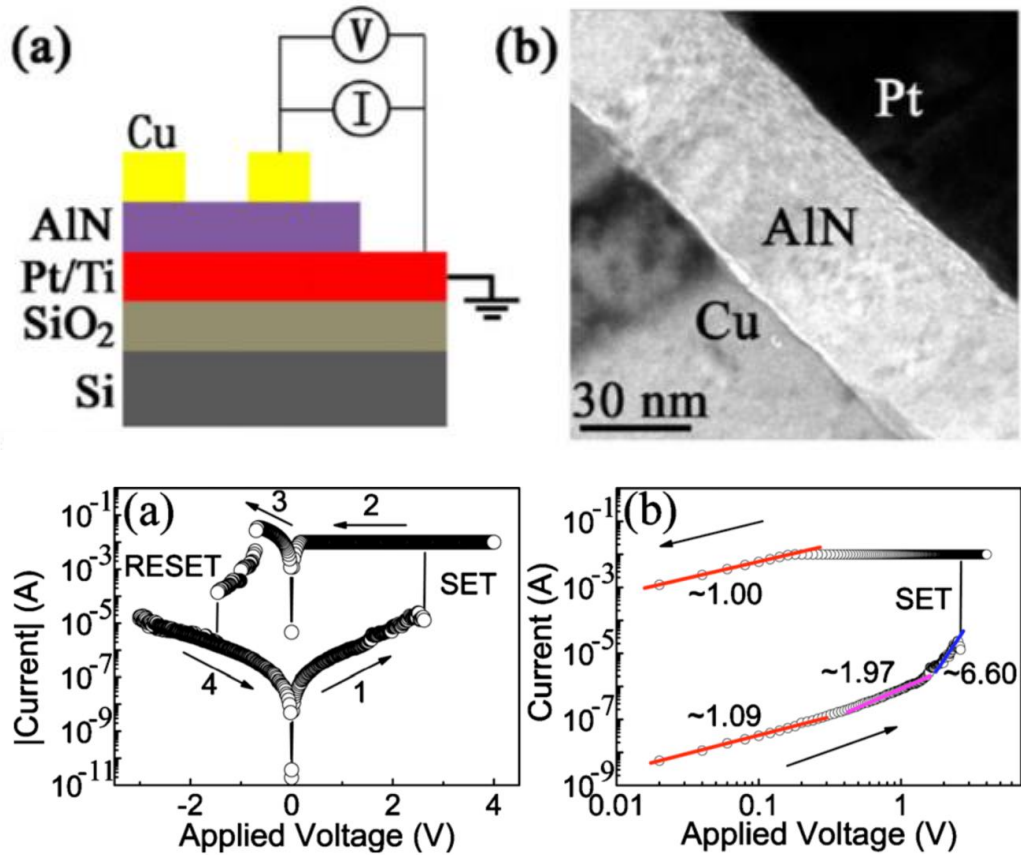


# Current Status of High-temperature Semiconductor Devices (Transistors)

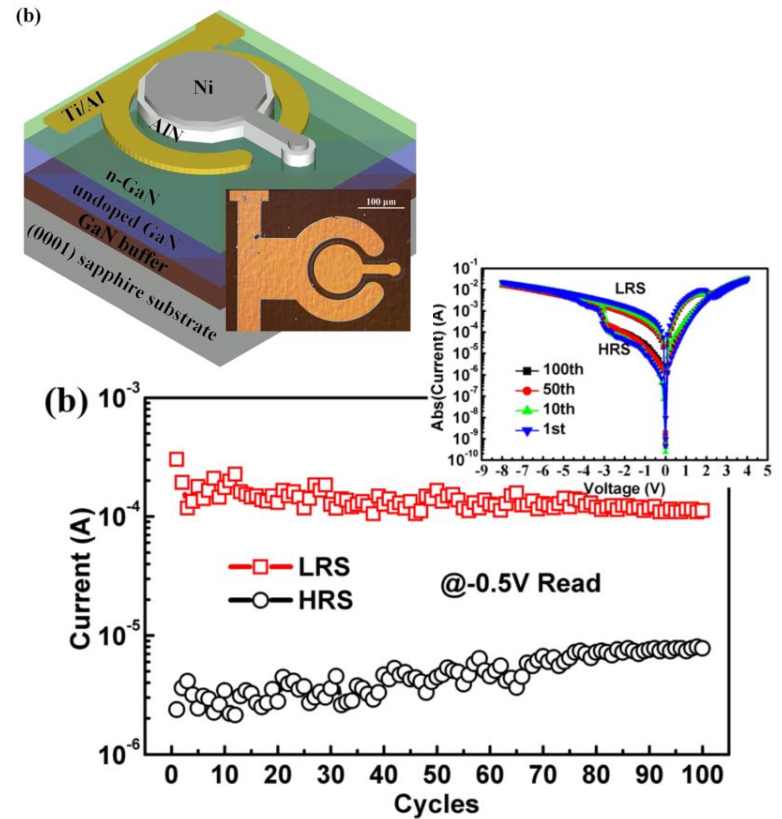
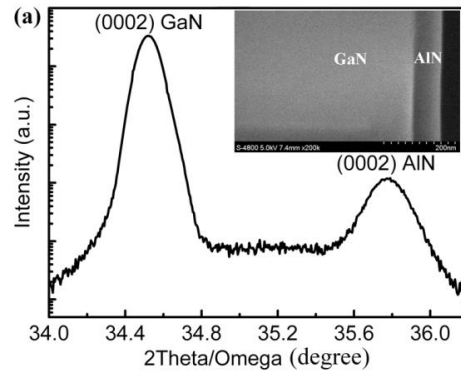


Pradhan, D.K., Moore, D.C., Francis, A.M. et al. Materials for high-temperature digital electronics. Nat Rev Mater 9, 790–807 (2024)

# Topic: GaN Resistive Switching Memory



C. Chen, Y. C. Yang, F. Zeng, and F. Pan, "Bipolar resistive switching in Cu/AlN/Pt nonvolatile memory device," *Appl. Phys. Lett.*, vol. 97, 2010.

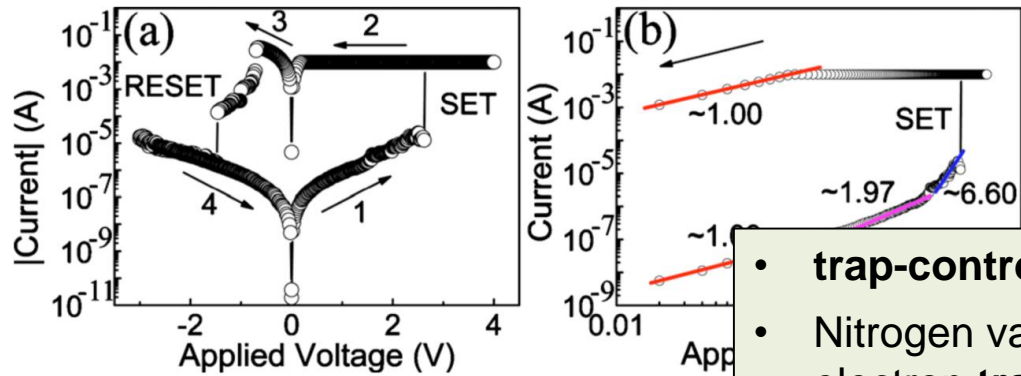
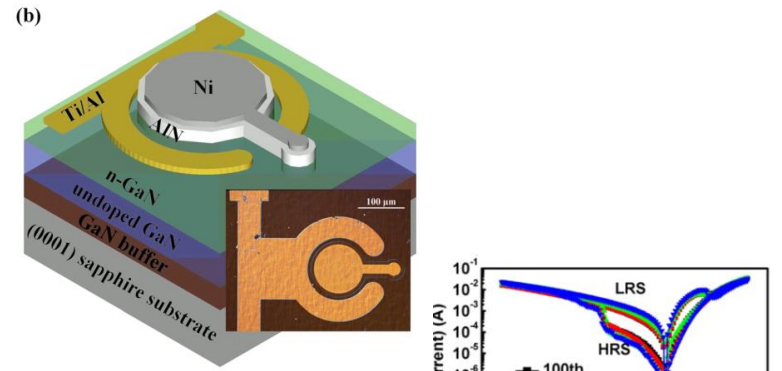
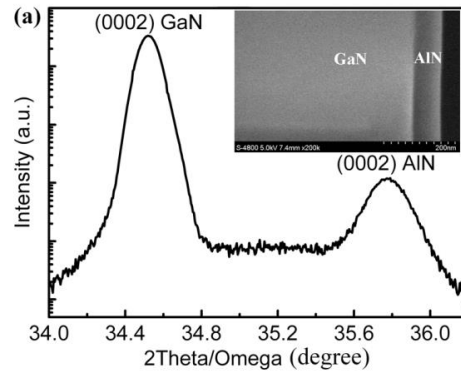
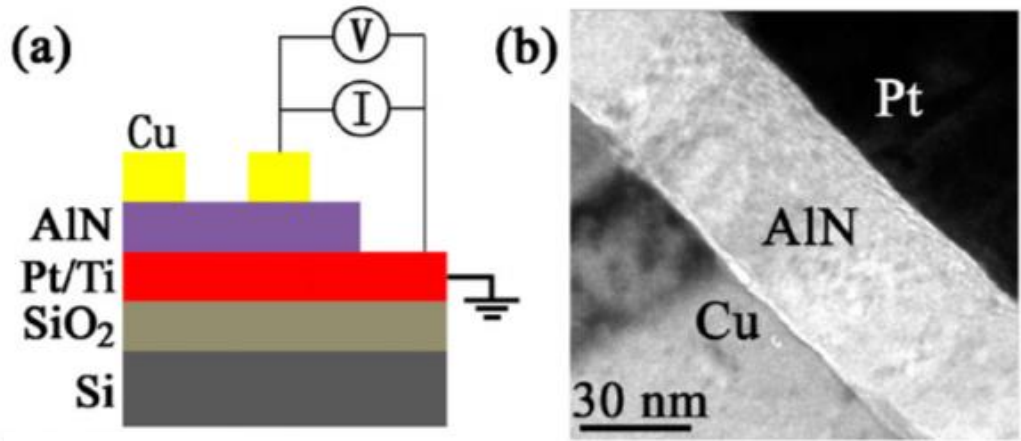


Y. Chen et al., "Reproducible bipolar resistive switching in entire nitride AlN/n-GaN metal-insulator-semiconductor device and its mechanism," *Appl. Phys. Lett.*, vol. 105, 2014.

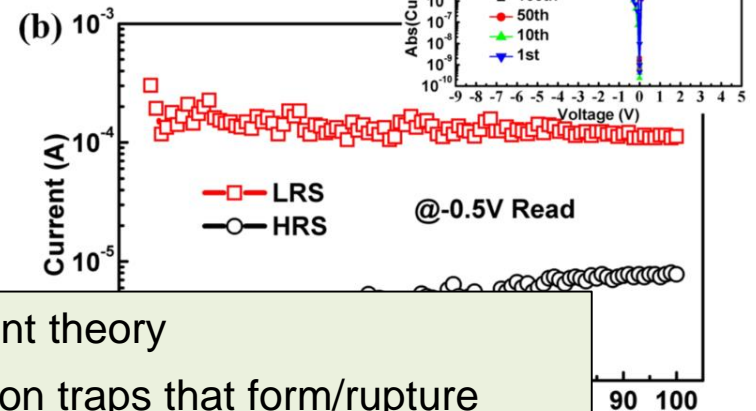
- *resistance-switching random access memory (RRAM)*
- *nonvolatile memory*
- *high response speed*
- *high scalability*
- *high density*

❑ Limited work on selector or memory before 2019: **<150 °C**, endurance problem

# Topic: GaN Resistive Switching Memory



- *resistance-switching random access memory (RRAM)*
- *nonvolatile memory*



• **trap-controlled** space charge limited current theory  
 • Nitrogen vacancies of AlN serving as electron traps that form/rupture electron **transport channel** by **trapping/detrapping electrons**  
 • → high resistance state (**HRS**) and low resistance state (**LRS**)

C. Chen, Y. C. Yang, F. Zeng, and F. Pan, "Bipolar resistive switching in GaN-based nonvolatile memory device," *Appl. Phys. Lett.*, vol. 97, 2010.

N/n-GaN metal-oxide, 2014.

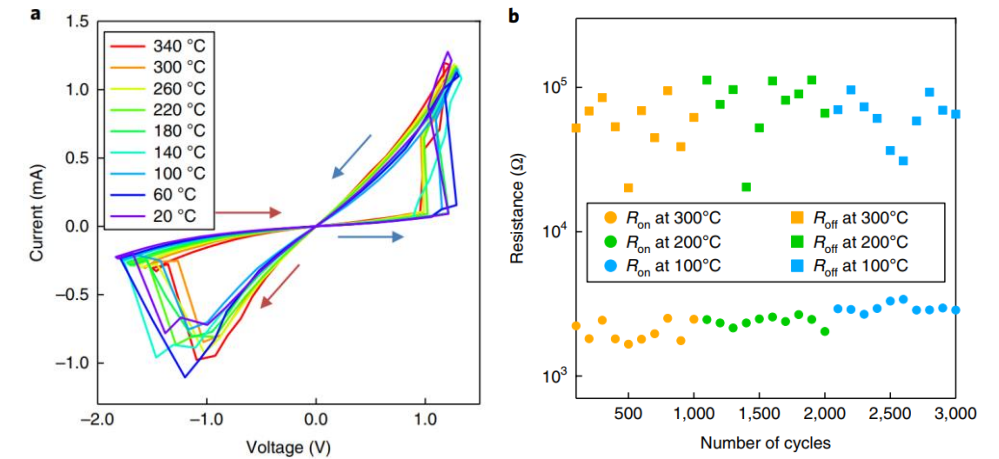
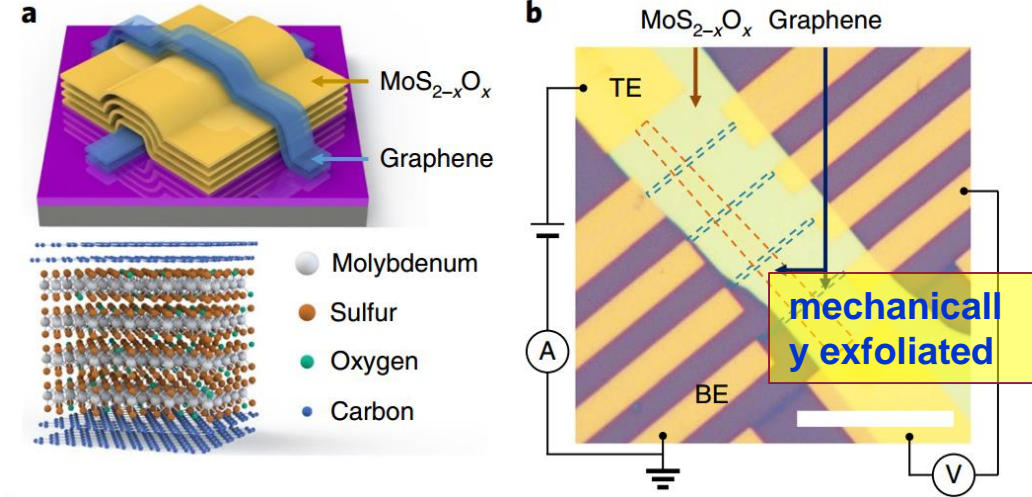
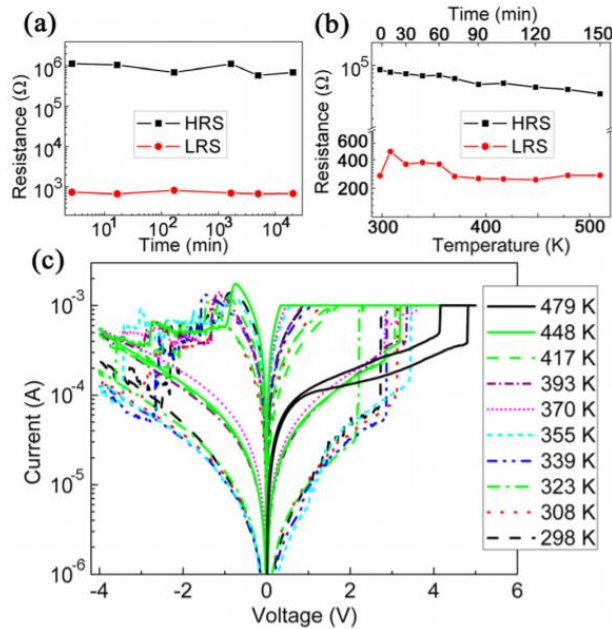
□ Limited work on selector or memory before 2019: <150 °C, endurance problem

Table 1.2: Summary of the materials that have been used for binary oxide RRAM reported in literature. Metals of the corresponding binary oxides used for the resistive switching layer are colored in yellow. Metals used for the electrodes are colored in blue. Used with permission from [4].

**The Periodic Table of the Elements**

corresponding binary oxide that exhibits bistable resistance switching  
 metal that is used for electrode

1																	1	2			
H																	H	He			
3	4															5	6	7	8	9	10
Li	Be															B	C	N	O	F	Ne
11	12															13	14	15	16	17	18
Na	Mg															Al	Si	P	S	Cl	Ar
19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36				
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr				
37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54				
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe				
55	56	57	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86				
Cs	Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn				
87	88	89	104	105	106	107	108	109	110	111	112										
Fr	Ra	Ac	Rf	Db	Sg	Bh	Hs	Mt													
		58	59	60	61	62	63	64	65	66	67	68	69	70	71						
		Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu						
		90	91	92	93	94	95	96	97	98	99	100	101	102	103						
		Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr						



S. Yu, "Resistive Random Access Memory (RRAM): From Devices to Array Architectures," in *Synthesis Lectures on Emerging Engineering Technologies*, vol. 2, 2016.

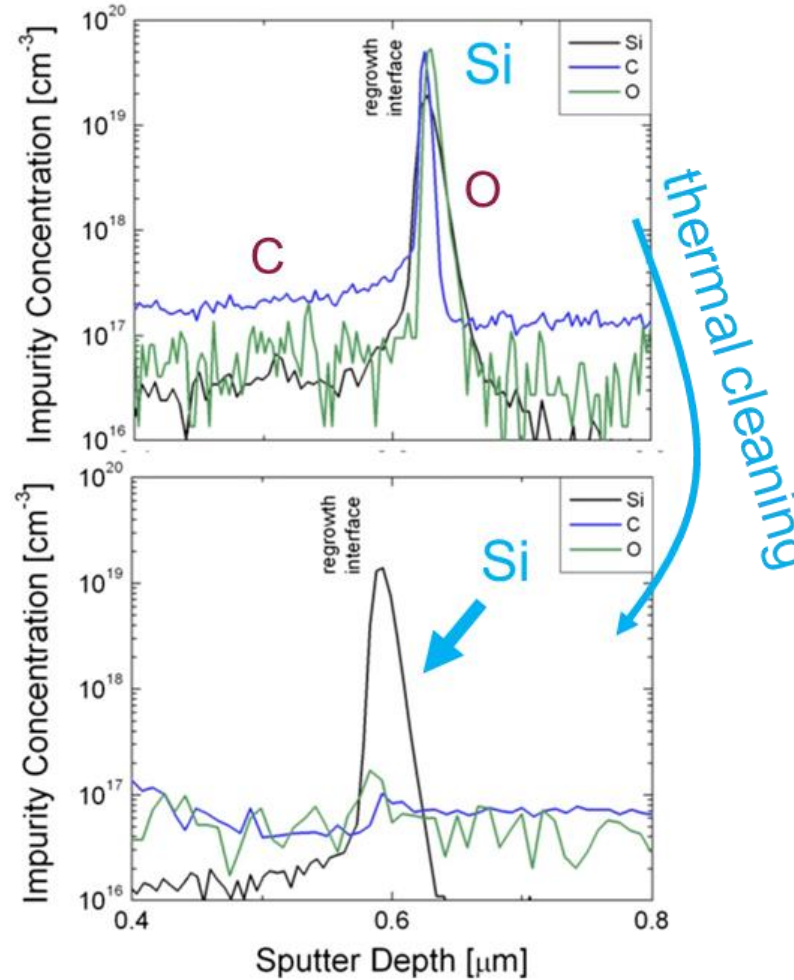
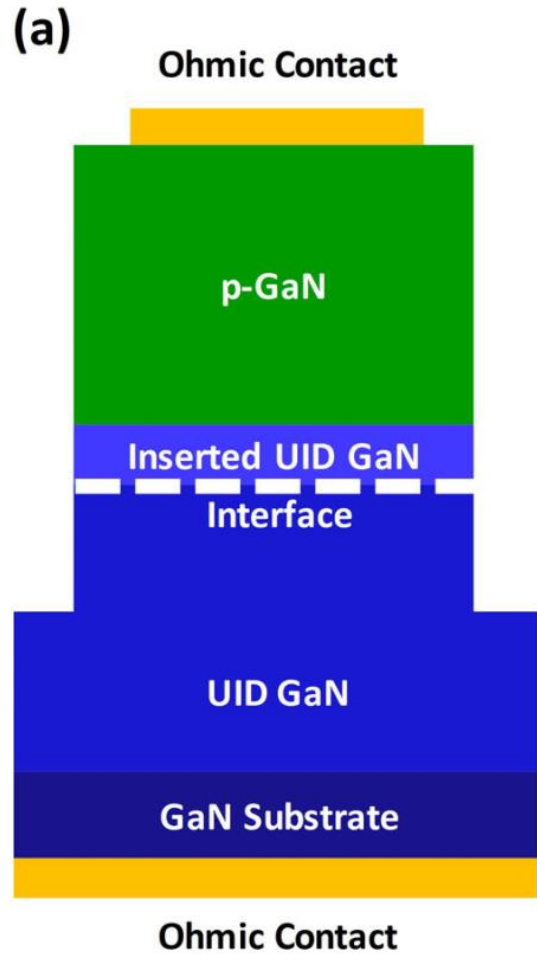
C. Chen, C. Song, J. Yang, F. Zeng, and F. Pan, "Oxygen migration induced resistive switching effect and its thermal stability in W/TaOx/Pt structure," *Appl. Phys. Lett.*, vol. 100, 2012

M. Wang et al., "Robust memristors based on layered two-dimensional materials," *Nat. Electron.*, vol. 1, 2018.

- ❑ Wide variety of material systems for RRAM, such as NiO, TiOx, CuOx, ZrOx, ZnOx, HfOx, TaOx, AlOx...
- ❑ Almost all reported < 200 °C

❑ 2D graphene/MoS<sub>2-x</sub>O<sub>x</sub>/graphene → 340 °C

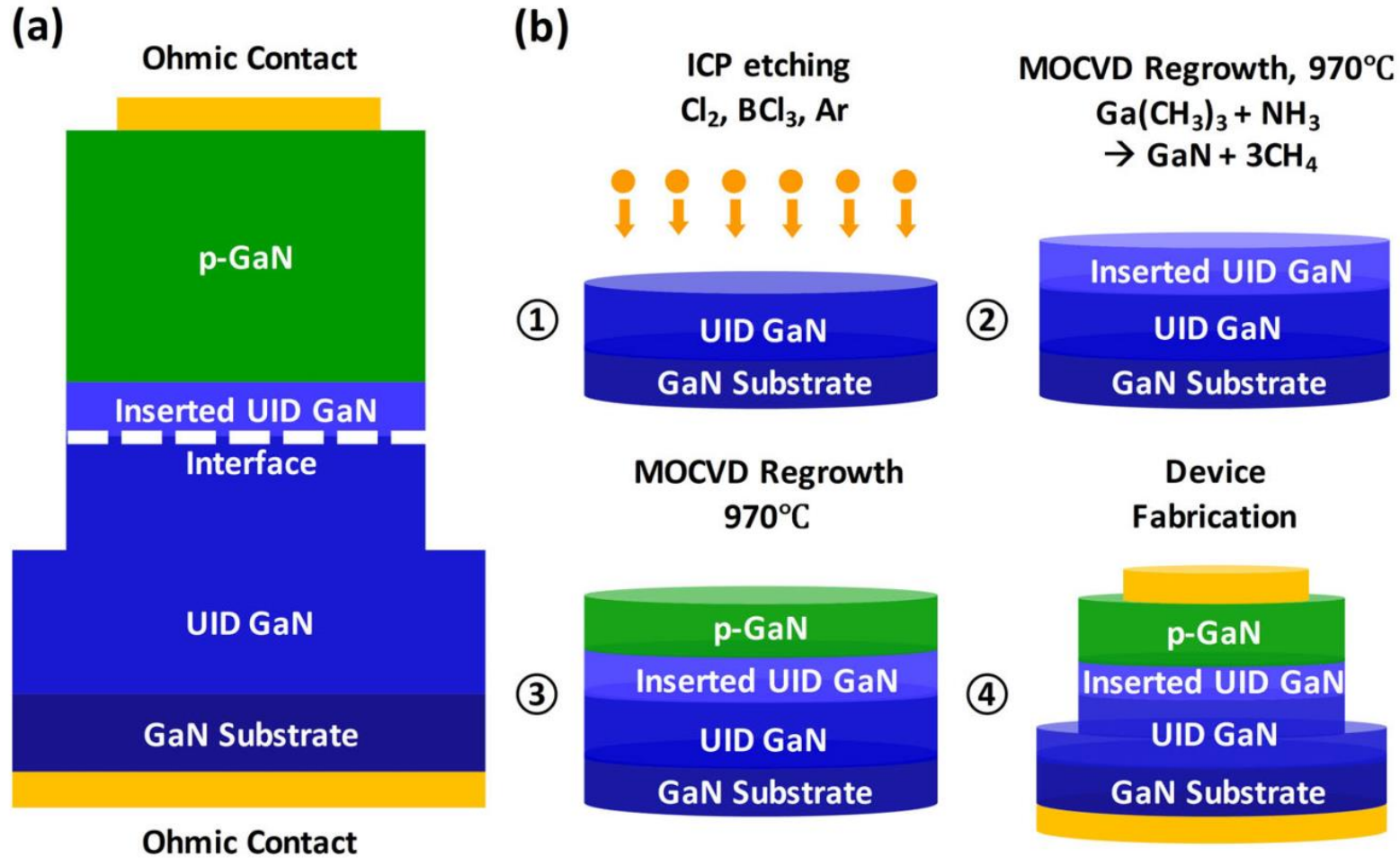
# Discovery of Memory Behavior in GaN p-n Diodes



G. Koblmüller, J. S. Speck, et al., Journal of Applied Physics, 107, 043527 (2010)

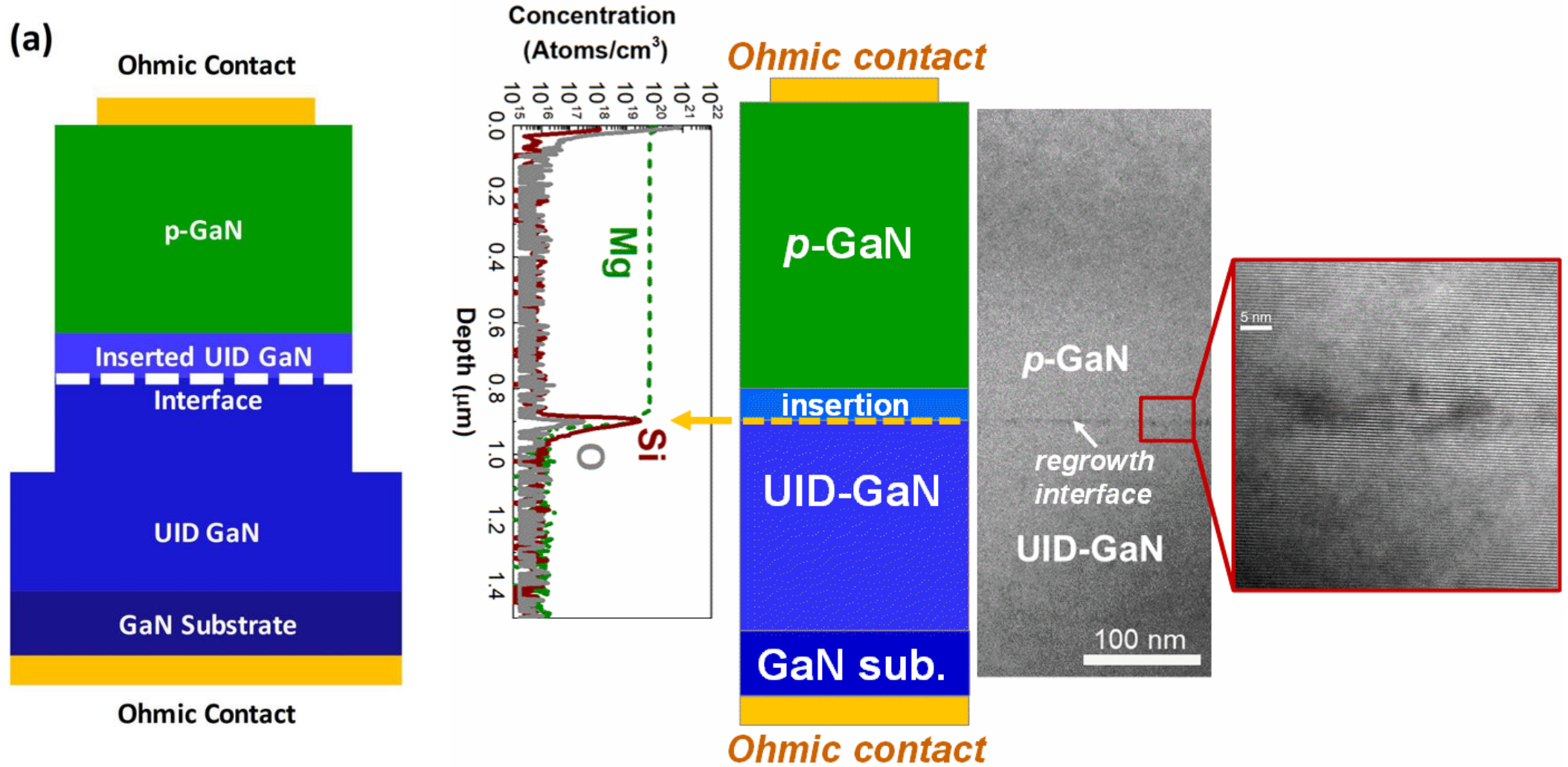
K. Fu, et al., IEEE Transactions on Electron Devices 71.3 (2023): 1641-1645.

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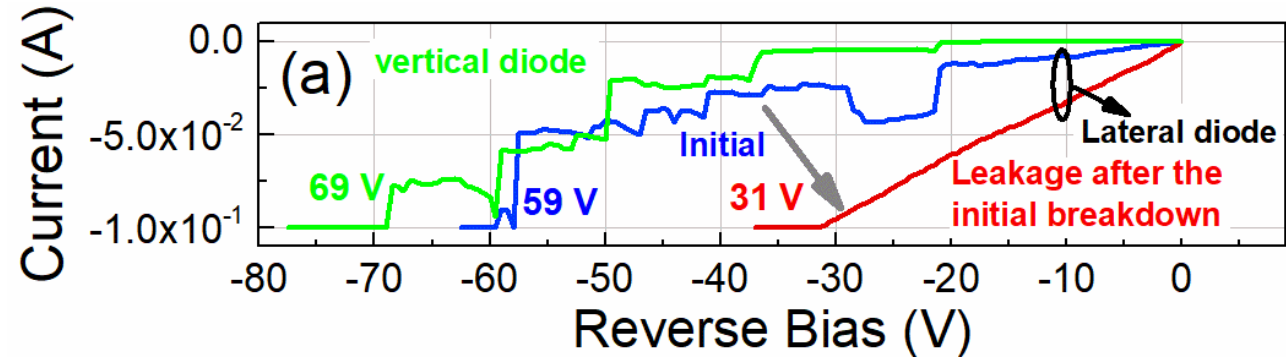
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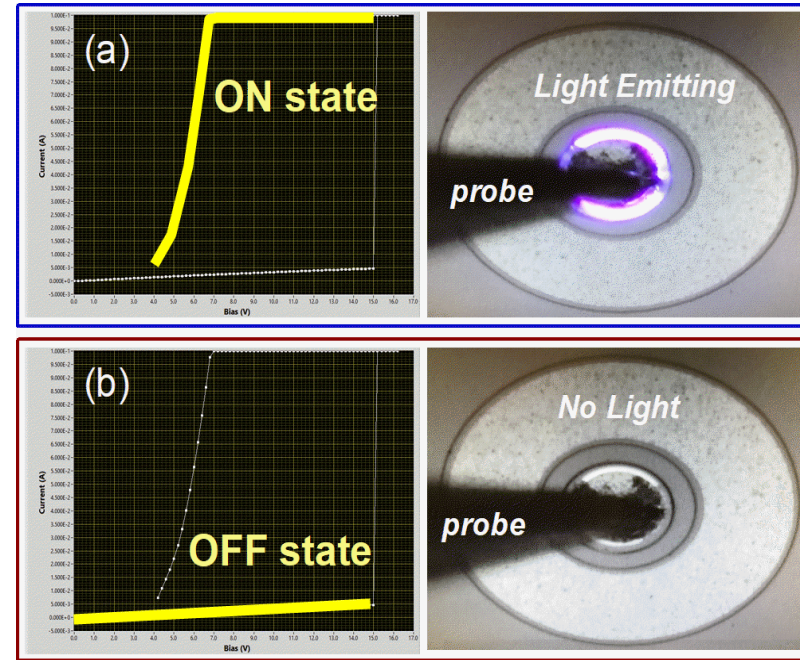
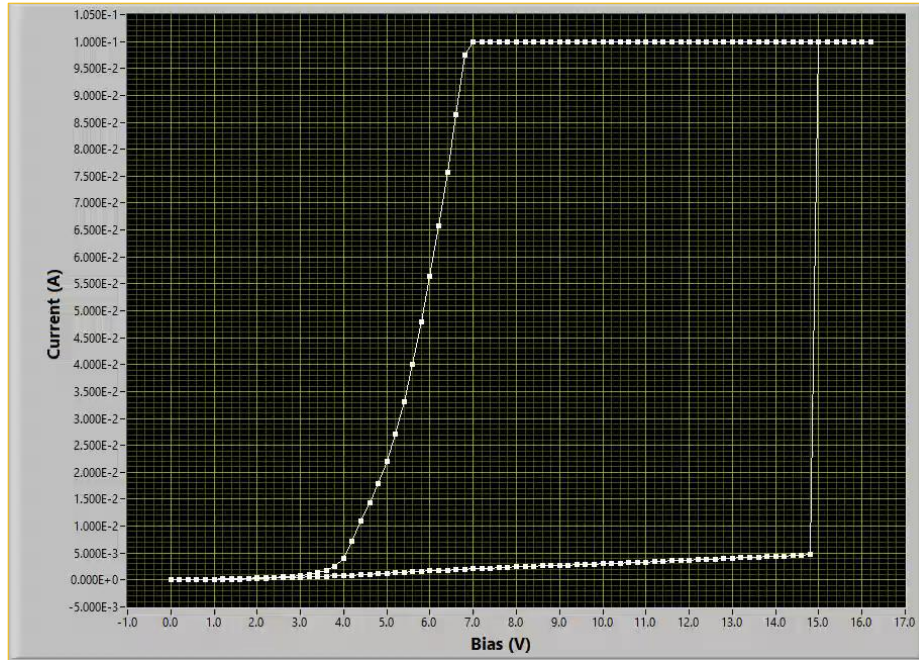
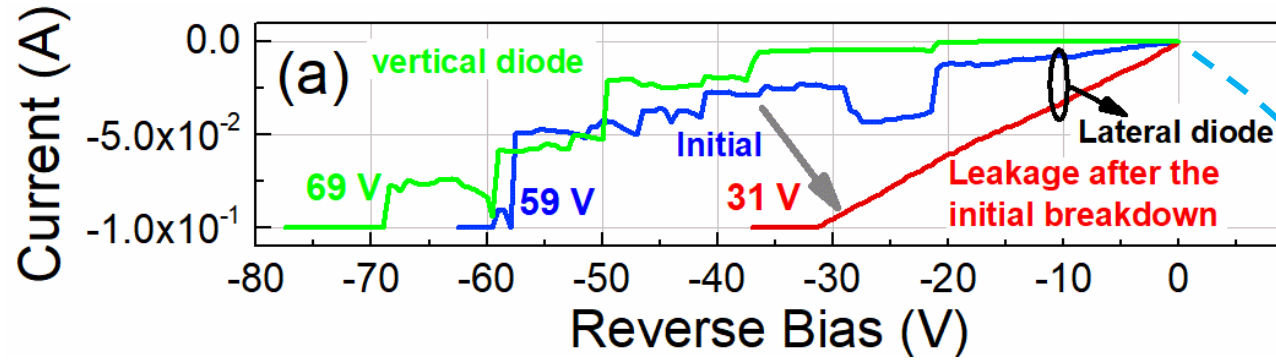
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K. Fu et al., *IEEE Electron Device Letters*, vol. 40, 2019.

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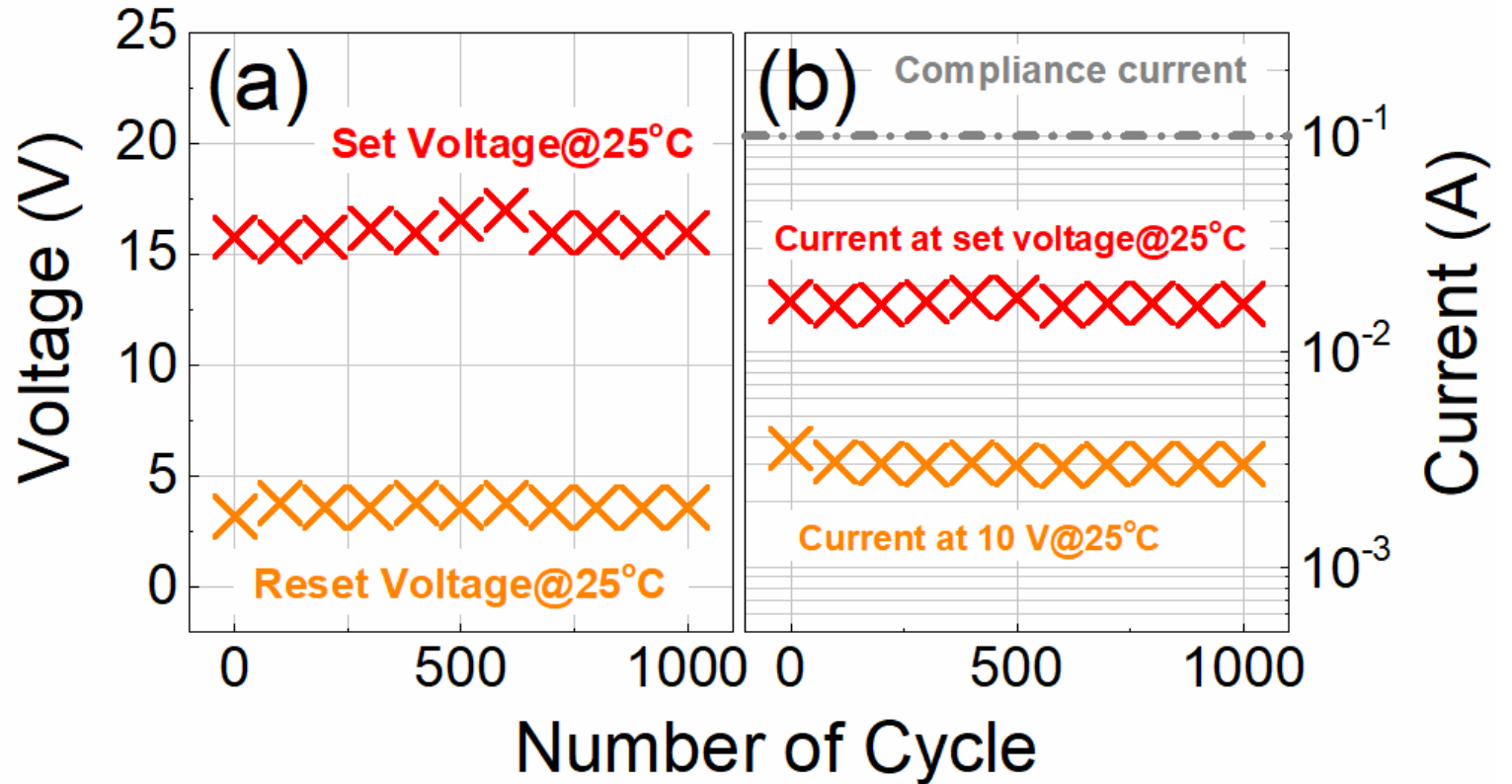
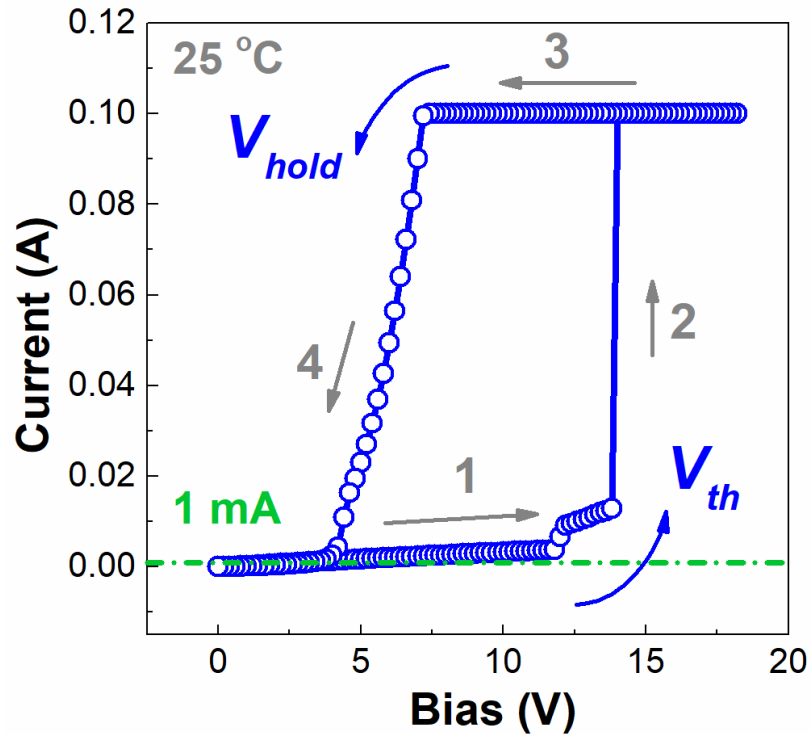


Reverse breakdown served as the forming process → resistive switching

K. Fu et al., IEEE Electron Device Letters, vol. 40, 2019.

# Discovery of Memory Behavior in GaN p-n Diodes

## ➤ Room temperature performance



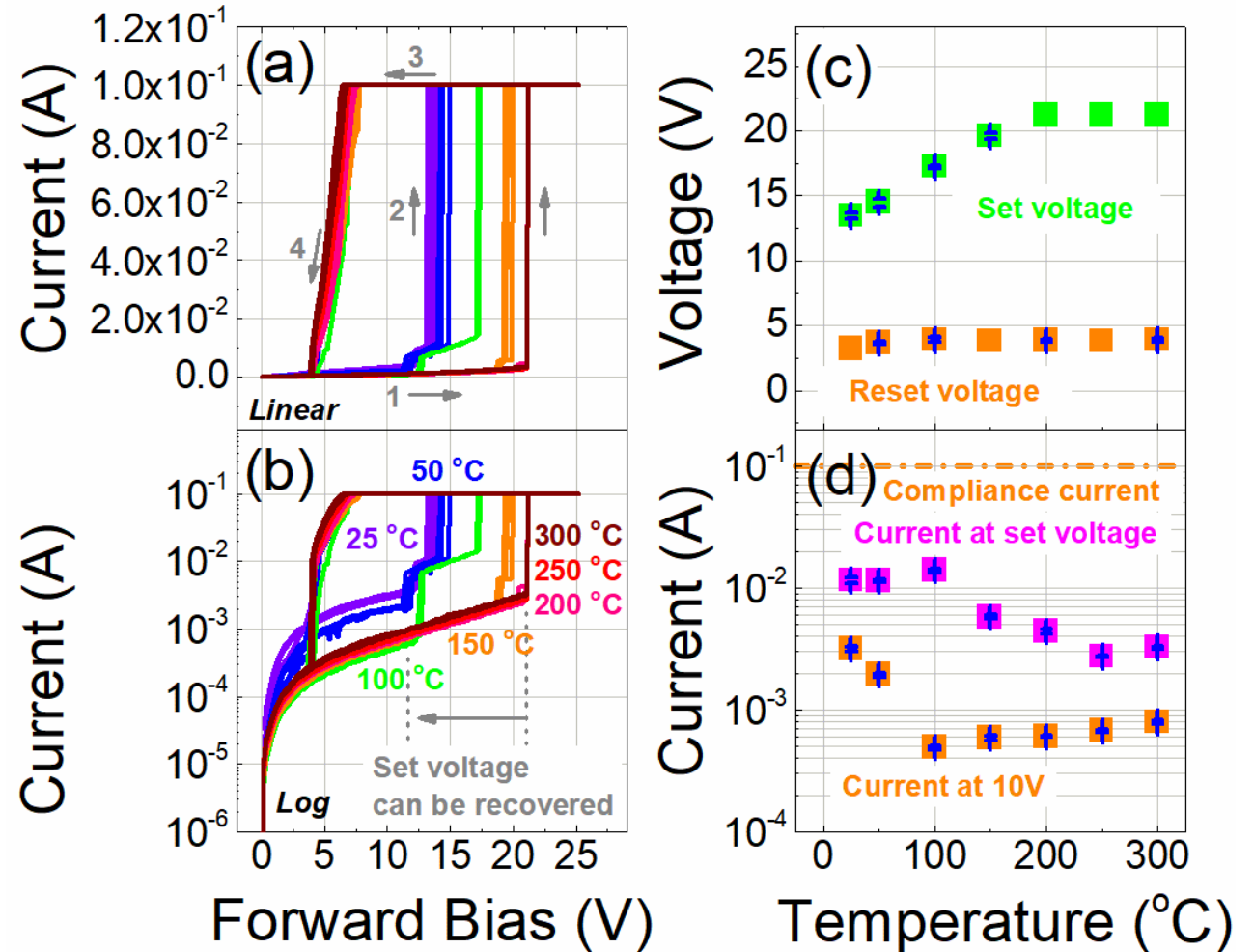
- ❑ Direct voltage scanning mode
- ❑ Reliably switched **more than 1000 cycles** at room temperature with **very small fluctuation** of the set voltage and the current at HRS

K. Fu et al., IEEE Electron Device Letters, vol. 40, 2019.

# Discovery of Memory Behavior in GaN p-n Diodes

## ➤ High temperature performance

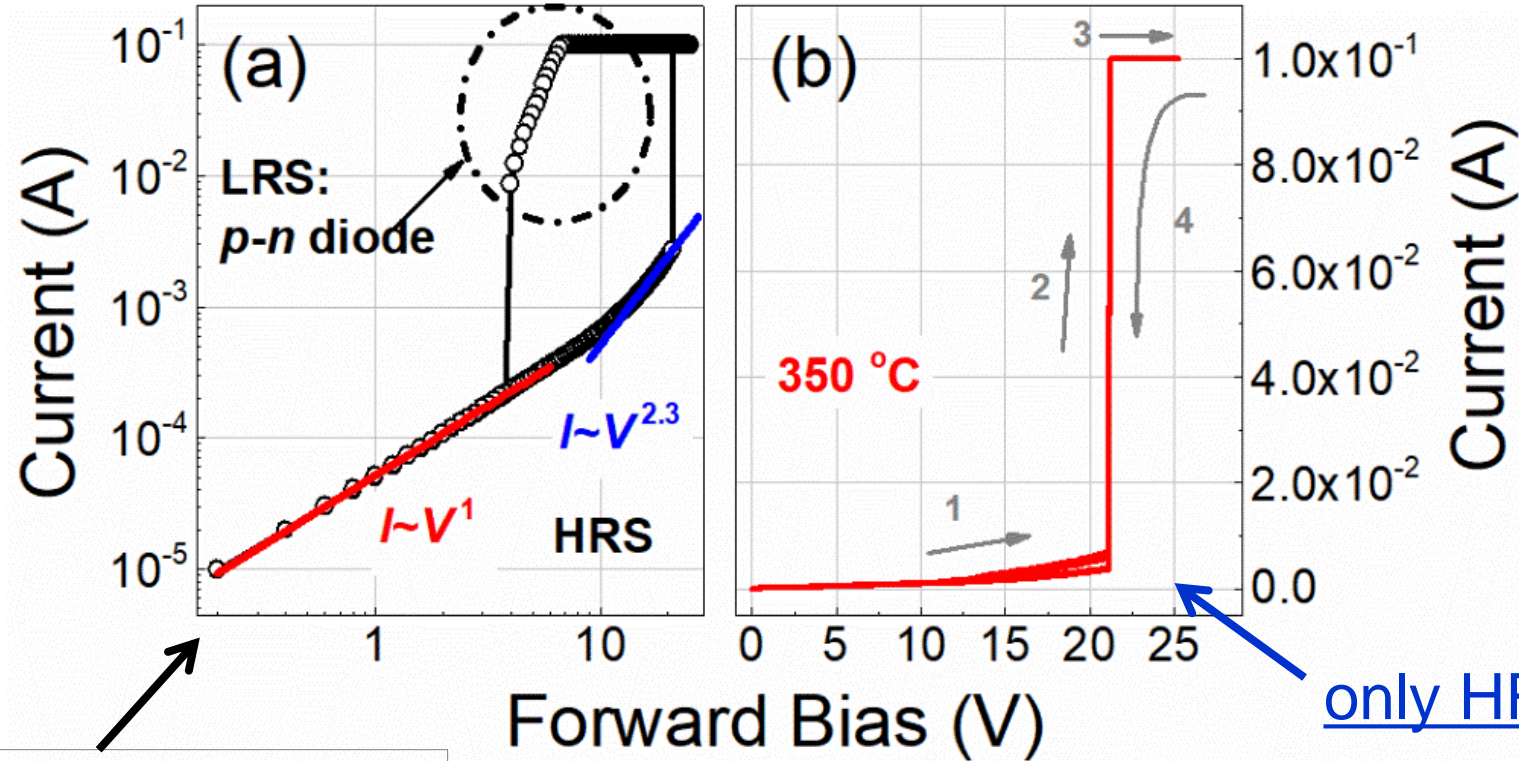
- ❑ The set voltage increases with temperature
- ❑ The device performance returns to its initial values as the temperature decreases to room temperature.



K. Fu et al., IEEE Electron Device Letters, vol. 40, 2019.

# Discovery of Memory Behavior in GaN p-n Diodes

## ➤ High temperature performance



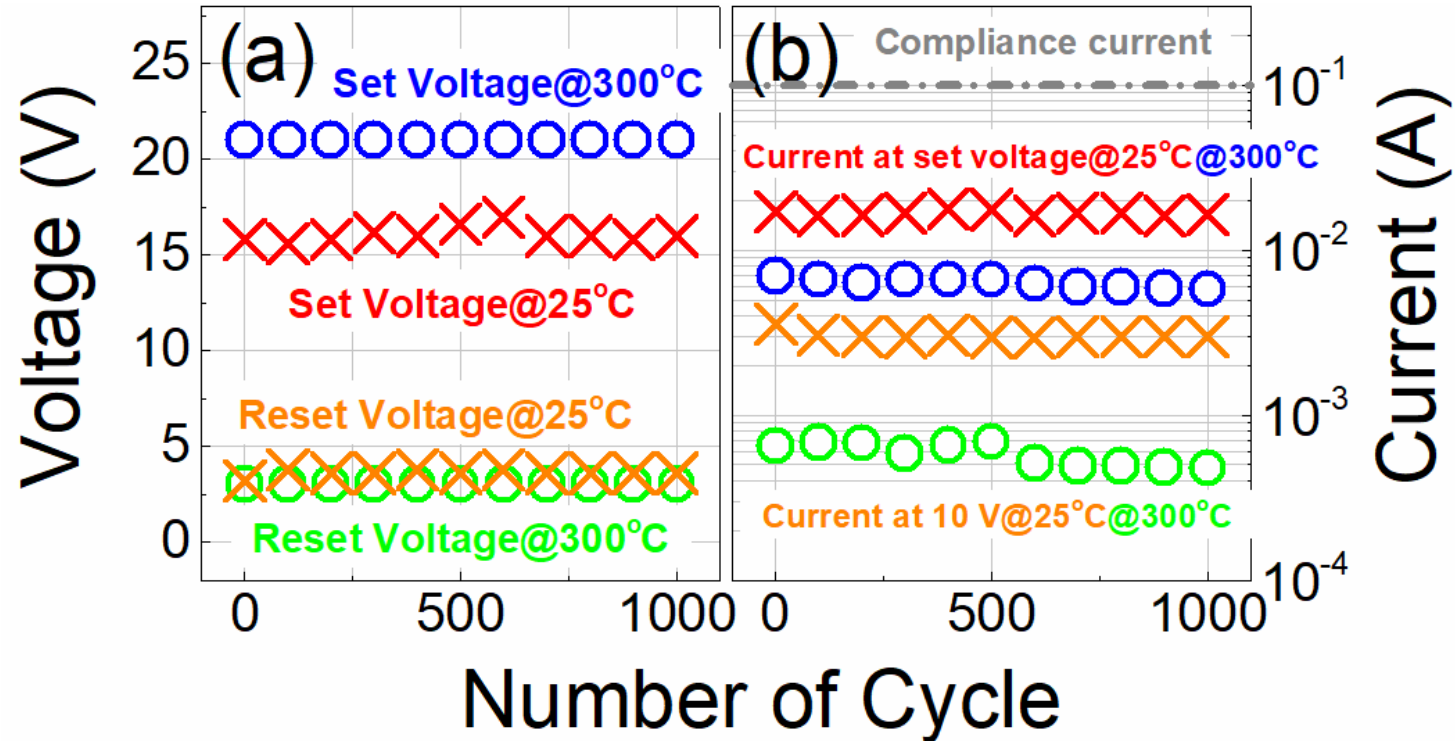
only HRS if > 300 C

HRS I-V curves: trap-assisted space charge limited current (**SCLC**) theory (the Ohmic region  $I \sim V$ , and the Child's square law region  $I \sim V^2$  followed by a steep increase in current)

K. Fu et al., IEEE Electron Device Letters, vol. 40, 2019.

# Discovery of Memory Behavior in GaN p-n Diodes

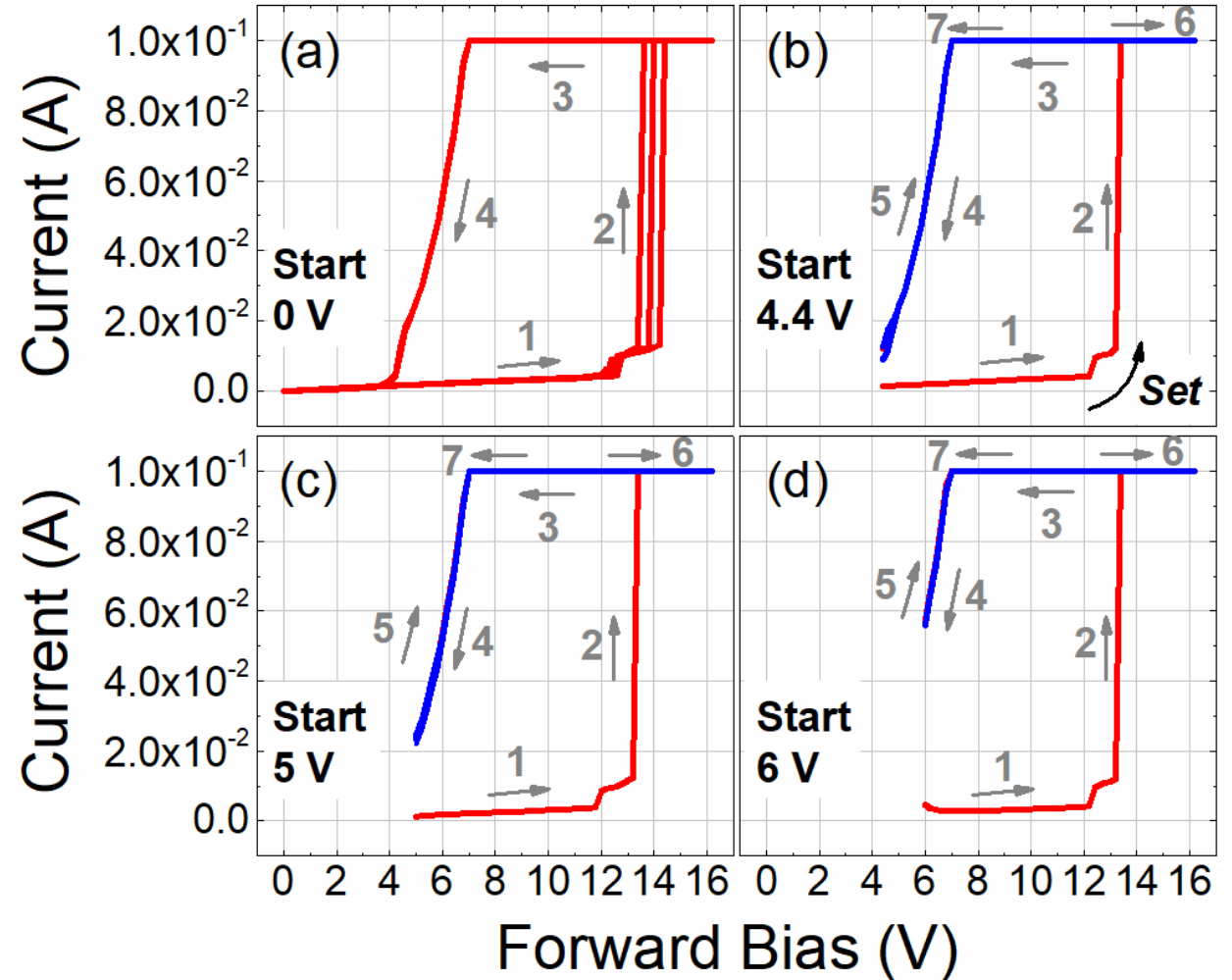
## ➤ High temperature performance



- ❑ Reliably switched **more than 1000 cycles at 300 °C** with **very small fluctuation** of the set voltage and the current at HRS
- ❑ The fabrication is **repeatable**

# Discovery of Memory Behavior in GaN p-n Diodes

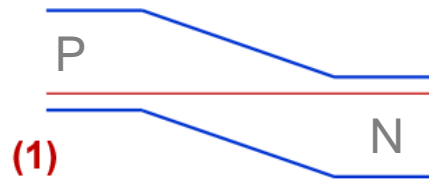
- The **traps-based conductive path could be maintained** when the **stop voltage** was a little higher than the turn-on voltage of the GaN p-n diode → Memory behavior, with high temperature stability!



K. Fu et al., IEEE Electron Device Letters, vol. 40, 2019.

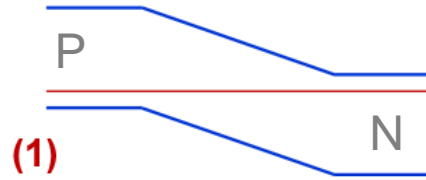
# Mechanism for Resistive Switching Behavior

0 V before breakdown

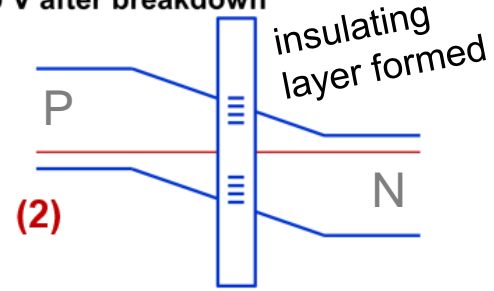


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0 V before breakdown

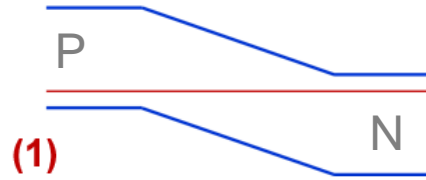


0 V after breakdown

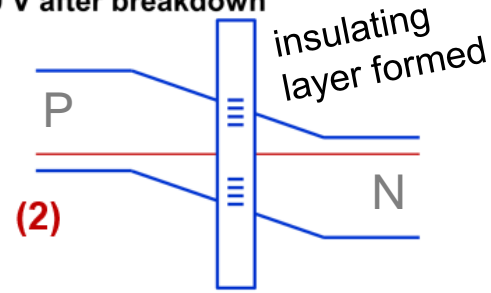


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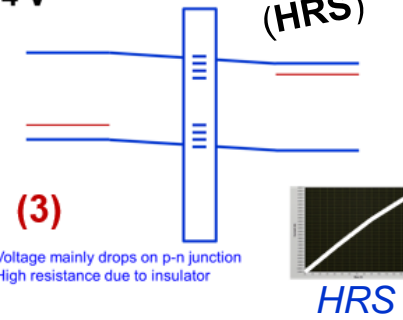
0 V before breakdown



0 V after breakdown

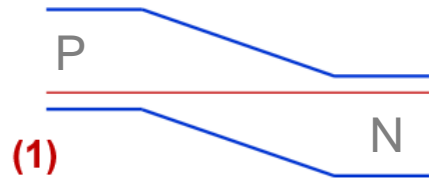


+4 V

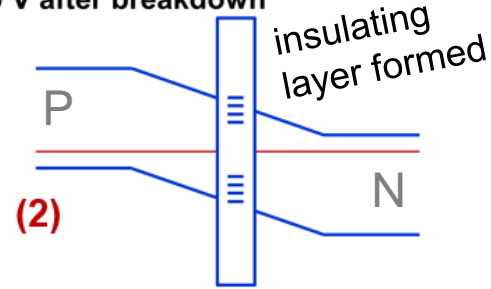


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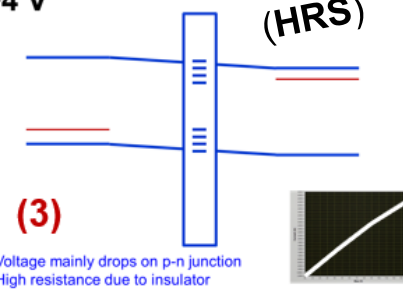
0 V before breakdown



0 V after breakdown

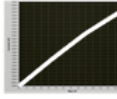


+4 V

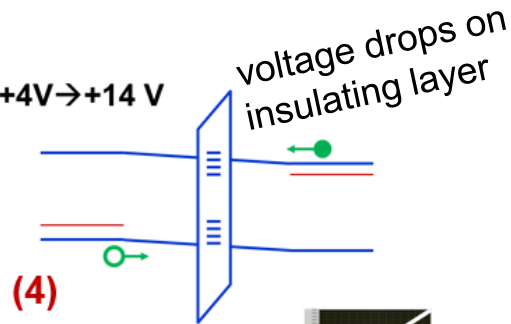


high resistivity state (HRS)

Voltage mainly drops on p-n junction  
High resistance due to insulator



+4V → +14 V

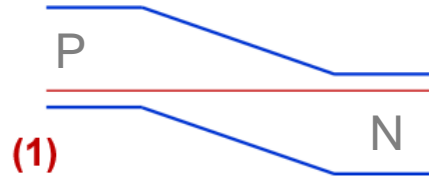


Voltage drops on insulator



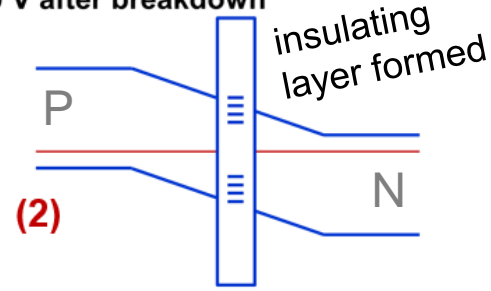
# Mechanism for Resistive Switching Behavior

0 V before breakdown



(1)

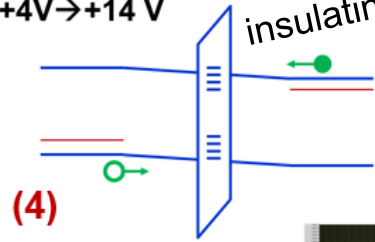
0 V after breakdown



(2)

insulating layer formed

+4V → +14 V  
voltage drops on insulating layer



(4)

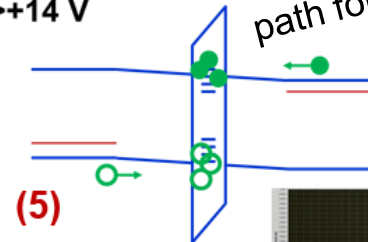
Voltage drops on insulator



HRS

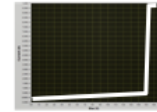
Insulator forms

>+14 V  
conduction path formed

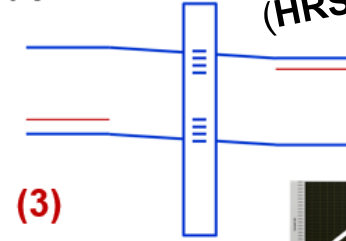


(5)

Electrons and holes fill the traps  
Conduction path forms

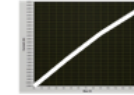


+4 V



(3)

Voltage mainly drops on p-n junction  
High resistance due to insulator

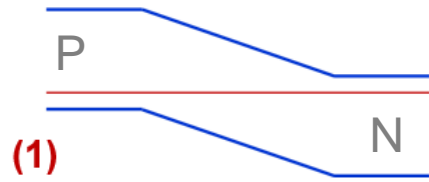


HRS

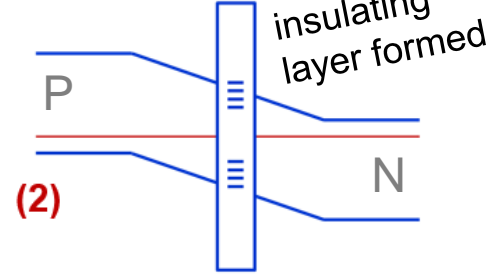
high resistivity state  
(HRS)

# Mechanism for Resistive Switching Behavior

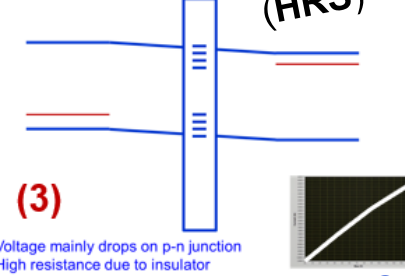
0 V before breakdown



0 V after breakdown



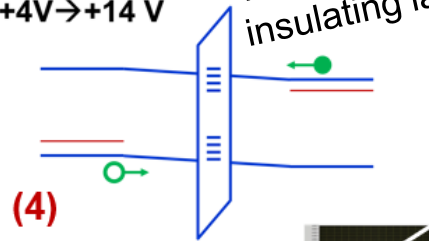
+4 V



Voltage mainly drops on p-n junction  
High resistance due to insulator

high resistivity state  
(HRS)

+4V → +14 V

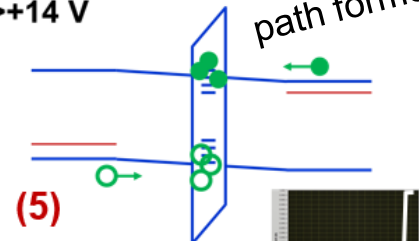


Voltage drops on insulator

voltage drops on insulating layer

HRS

>+14 V

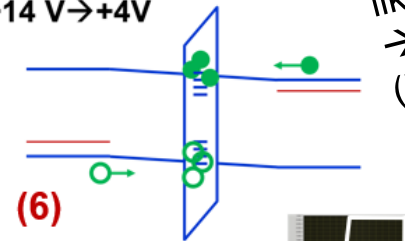


Electrons and holes fill the traps  
Conduction path forms

conduction path formed

like conventional diode  
→ low resistivity state  
(LRS)

+14 V → +4V

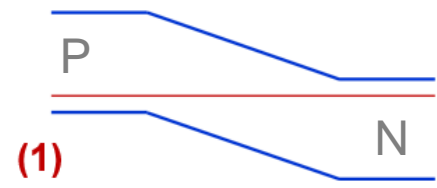


Just conventional p-n diode performance

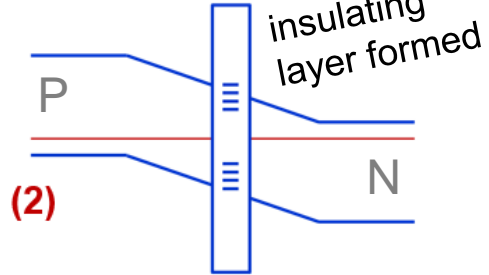
LRS

# Mechanism for Resistive Switching Behavior

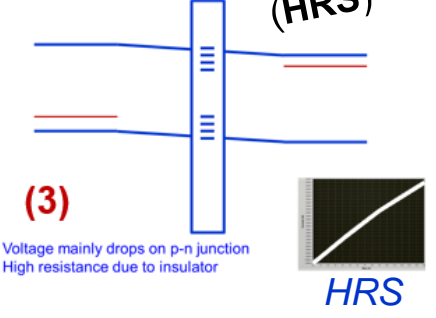
0 V before breakdown



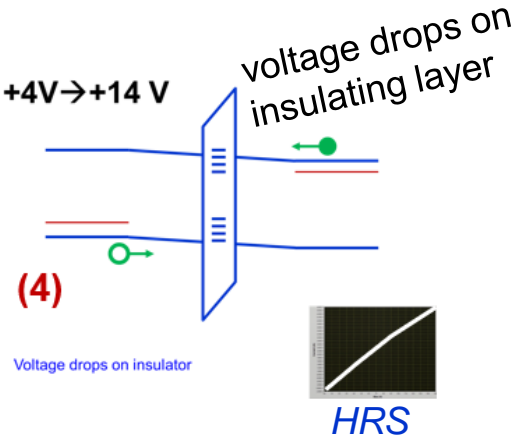
0 V after breakdown



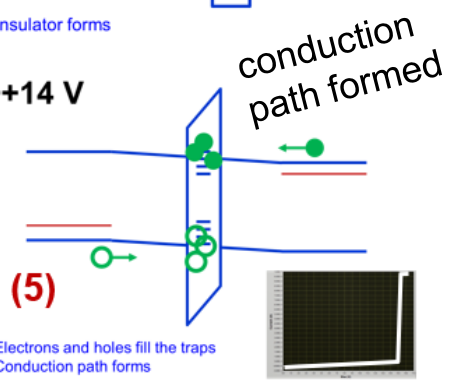
+4 V



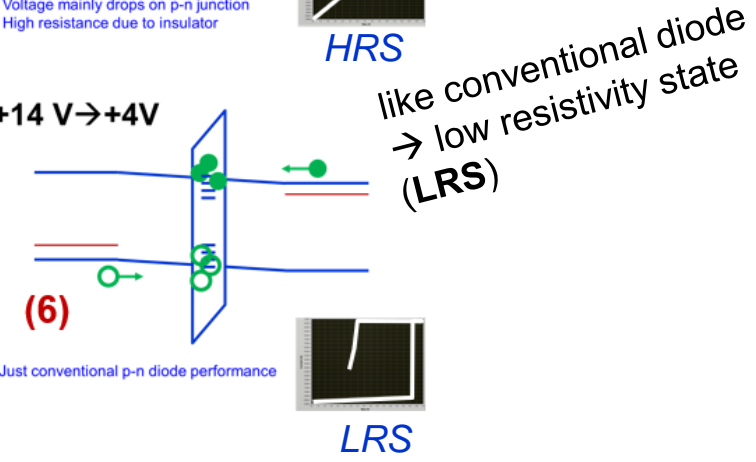
+4V → +14 V



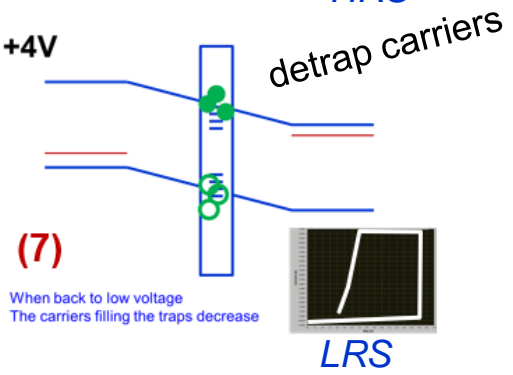
>+14 V



+14 V → +4V

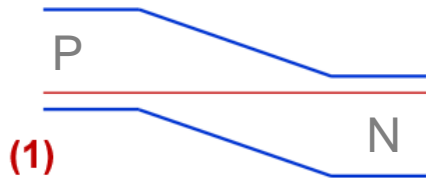


+4V

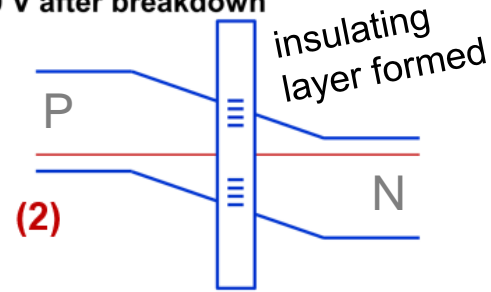


# Mechanism for Resistive Switching Behavior

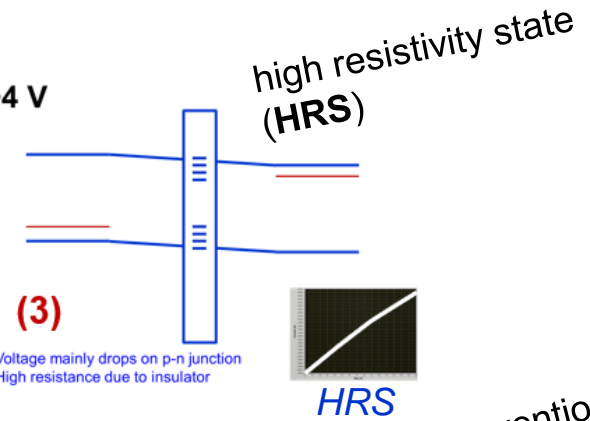
0 V before breakdown



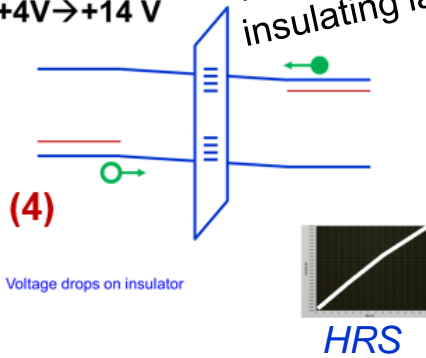
0 V after breakdown



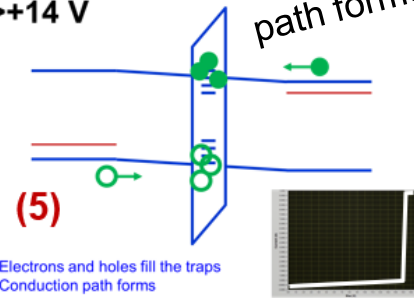
+4 V



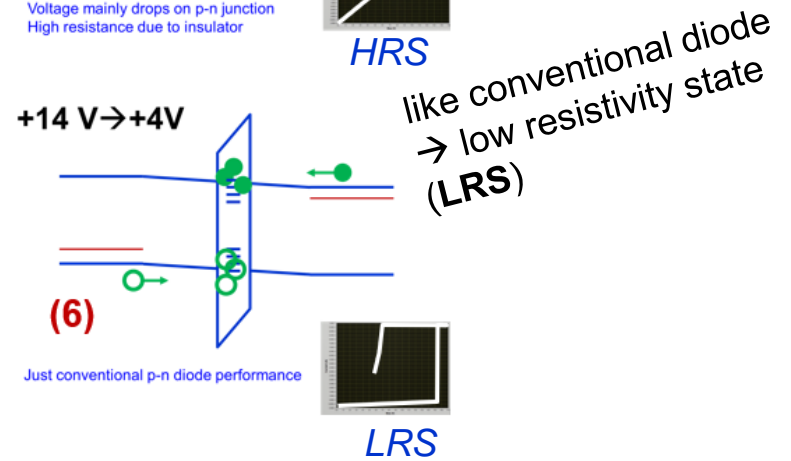
+4V → +14 V  
voltage drops on insulating layer



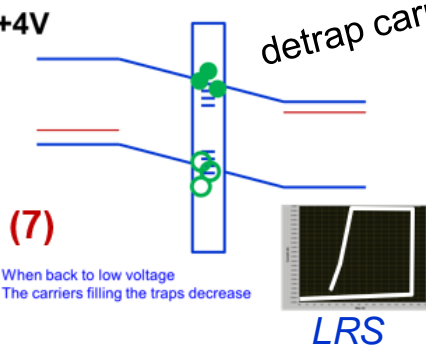
>+14 V  
conduction path formed



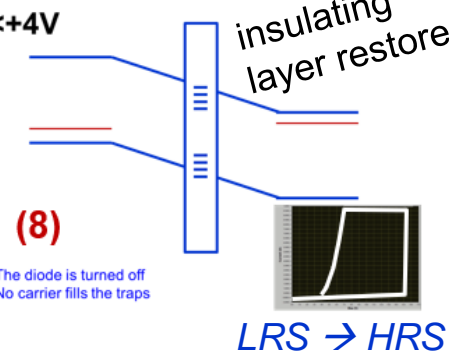
+14 V → +4 V



+4V  
detrap carriers

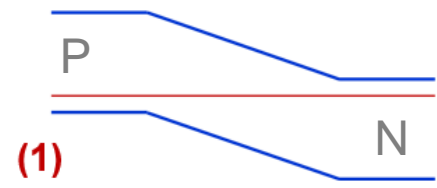


<+4V  
insulating layer restored

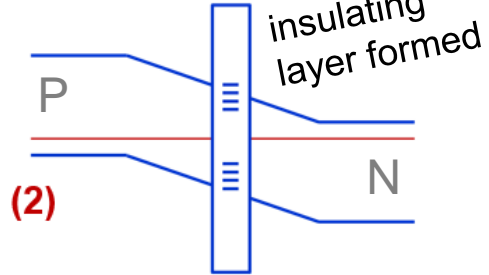


# Mechanism for Resistive Switching Behavior

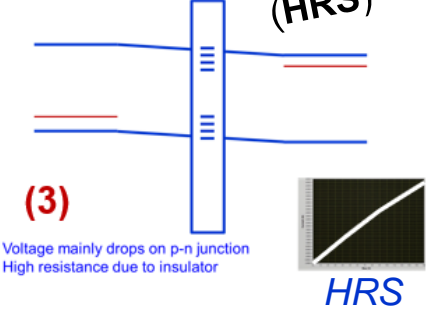
0 V before breakdown



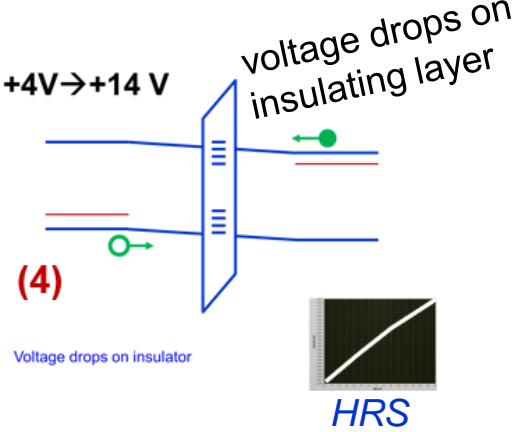
0 V after breakdown



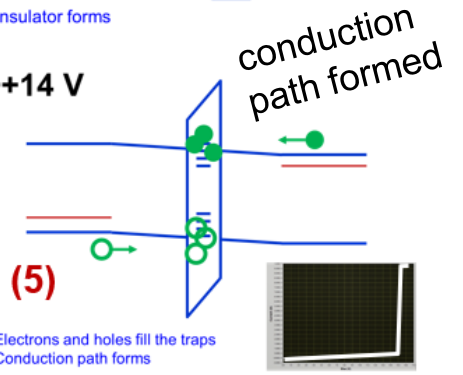
+4 V



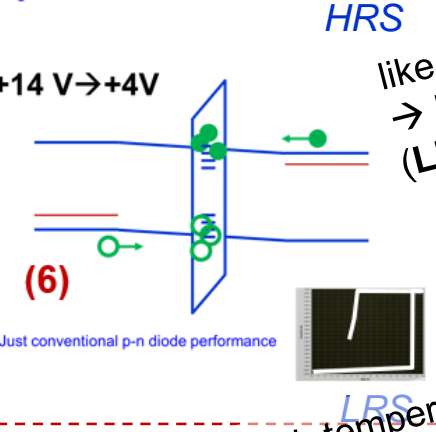
+4V → +14 V



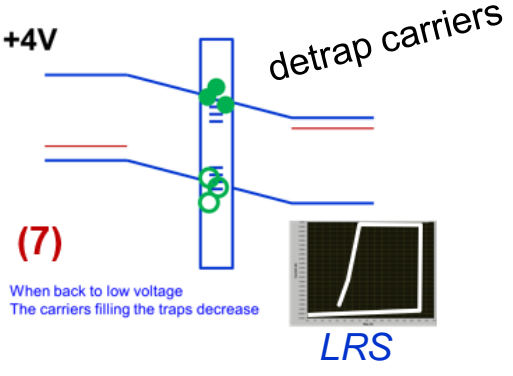
>+14 V



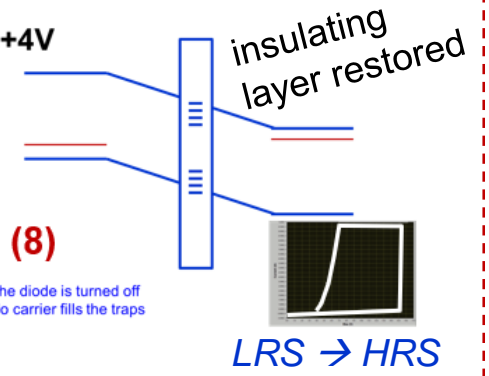
+14 V → +4V



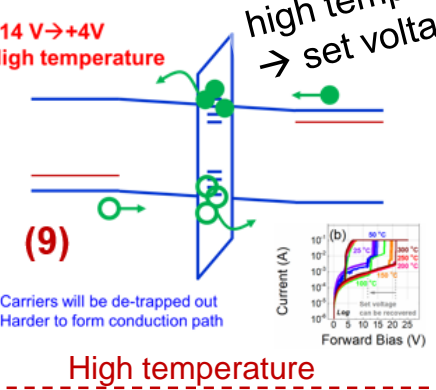
+4V



<+4V



+14 V → +4V



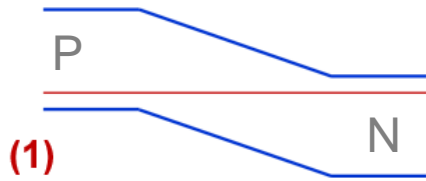
high resistivity state (HRS)

like conventional diode → low resistivity state (LRS)

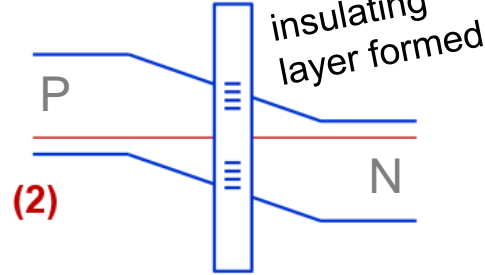
high temperature enhances de-trapping → set voltage shifts to higher value

# Mechanism for Resistive Switching Behavior

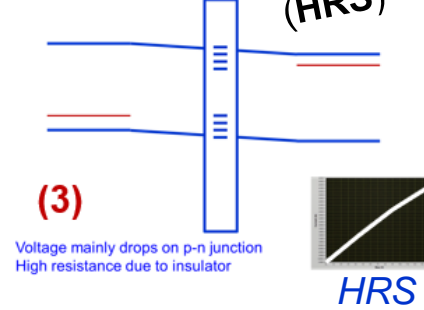
0 V before breakdown



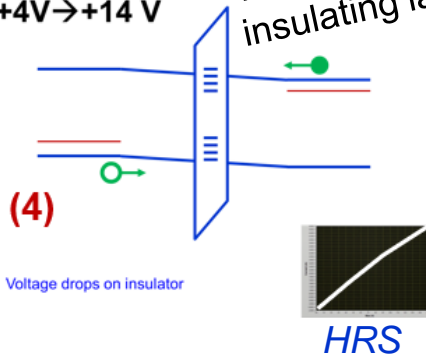
0 V after breakdown



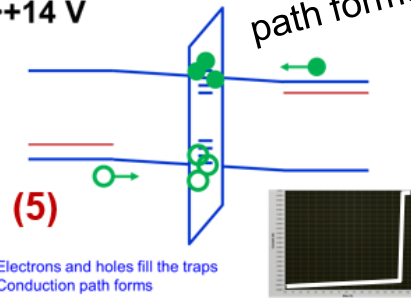
+4 V



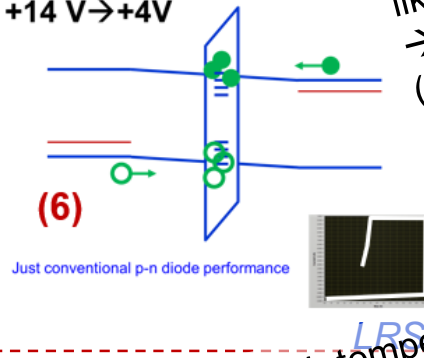
+4V → +14 V  
voltage drops on insulating layer



>+14 V  
conduction path formed

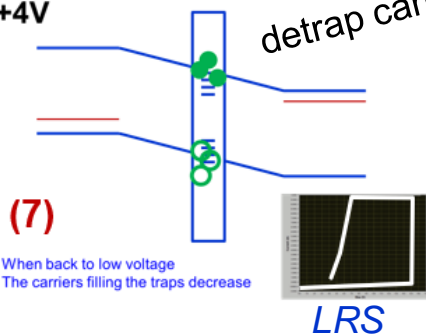


+14 V → +4 V

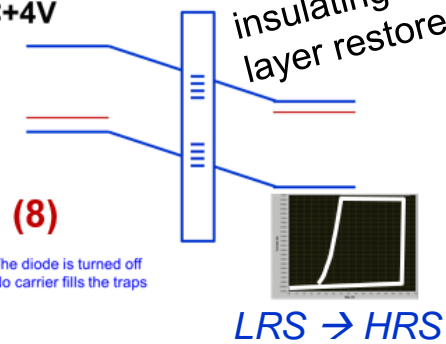


like conventional diode  
→ low resistivity state (LRS)

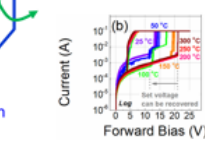
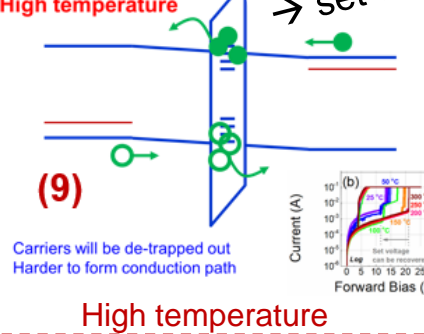
+4V  
detrap carriers



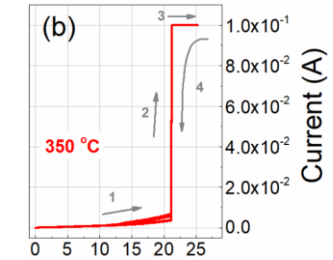
<+4V  
insulating layer restored



+14 V → +4 V



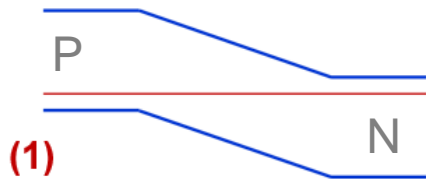
high temperature enhances de-trapping  
→ set voltage shifts to higher value  
too high → no threshold switching/only HRS





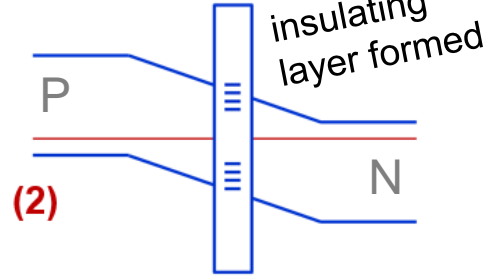
# Mechanism for Resistive Switching Behavior

0 V before breakdown



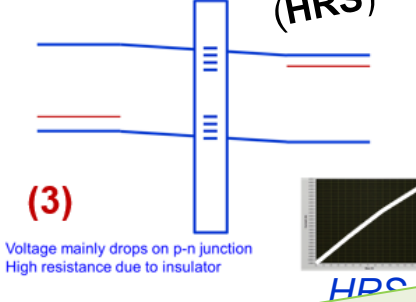
(1)

0 V after breakdown



(2)

+4 V



(3)

high resistivity state (HRS)

+4V → +14 V

voltage drops on insulating layer

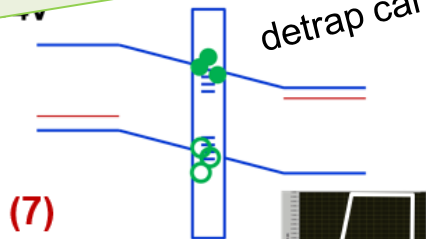


>+14 V

conduction path formed

**How to enhance the operation temperature based on the mechanism?**

detrap carriers

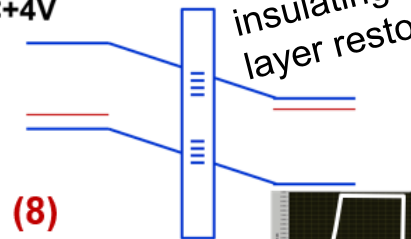


(7)

When back to low voltage The carriers filling the traps decrease

LRS

insulating layer restored

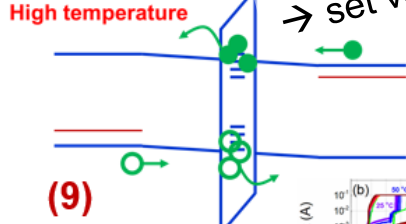


(8)

The diode is turned off No carrier fills the traps

LRS → HRS

+14 V → +4V



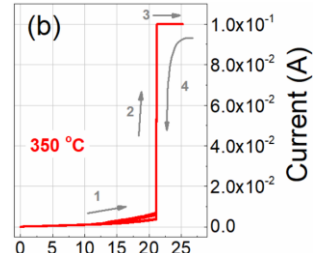
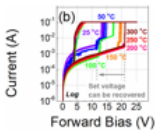
(9)

Carriers will be de-trapped out Harder to form conduction path

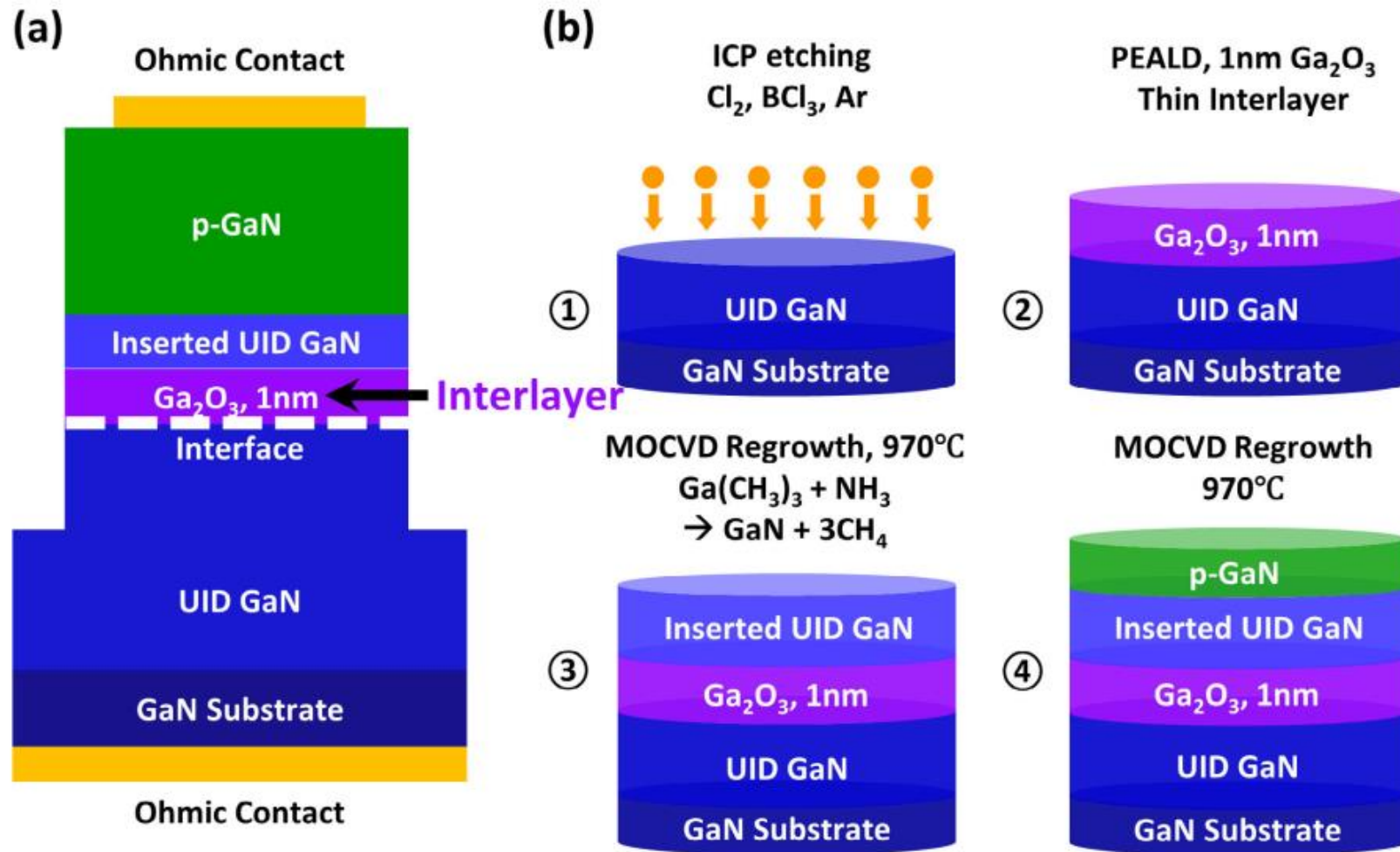
High temperature

high temperature enhances de-trapping → set voltage shifts to higher value

too high → no threshold switching/only HRS

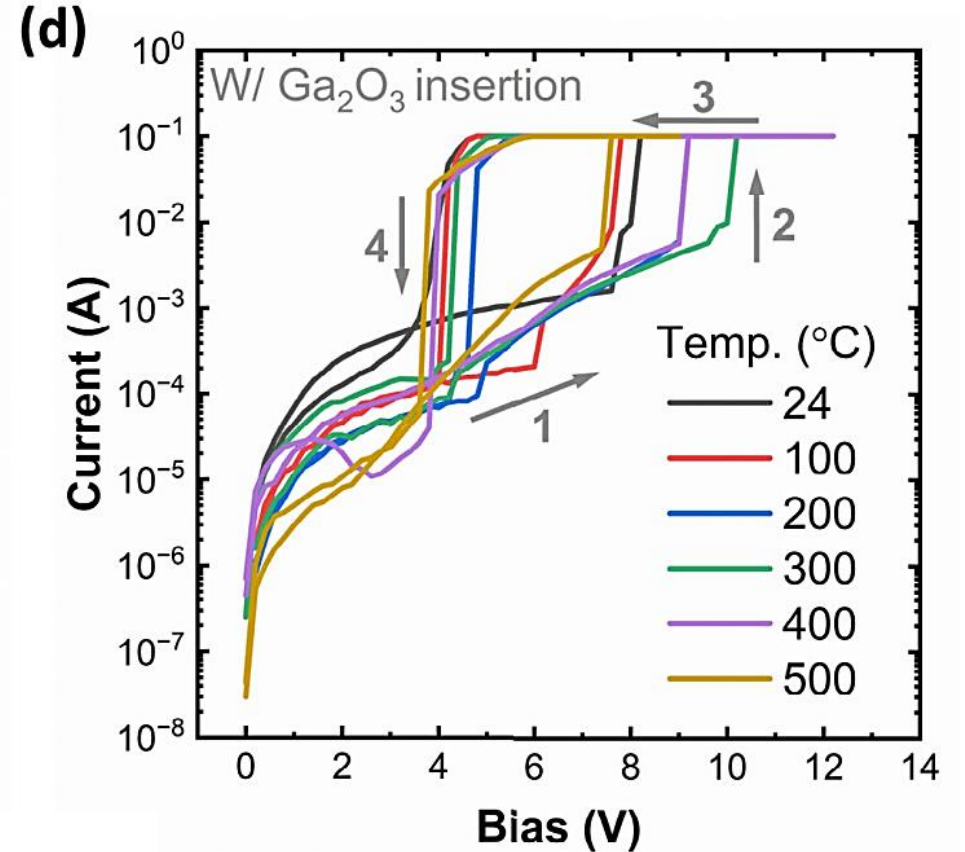
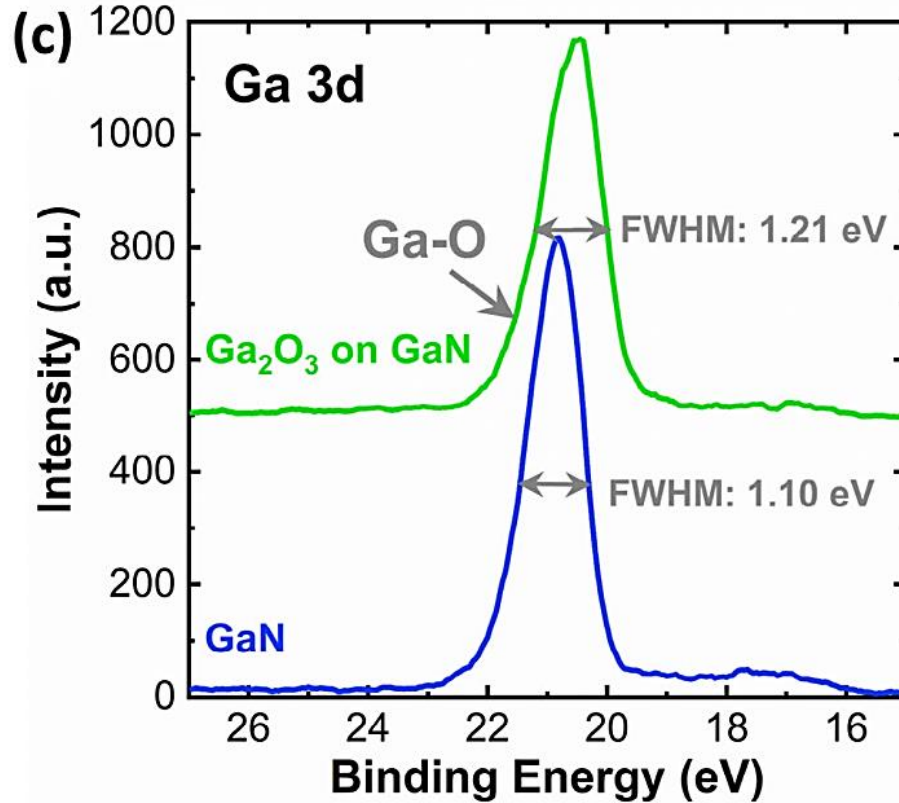
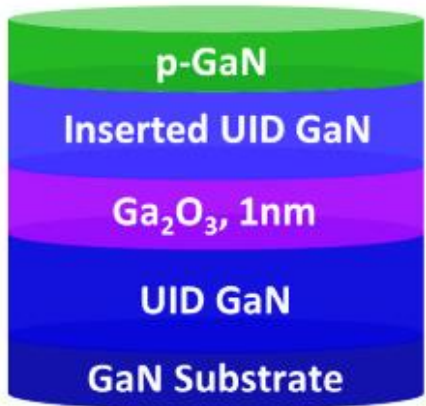


# Enhanced GaN Memory Behavior up to 500 C



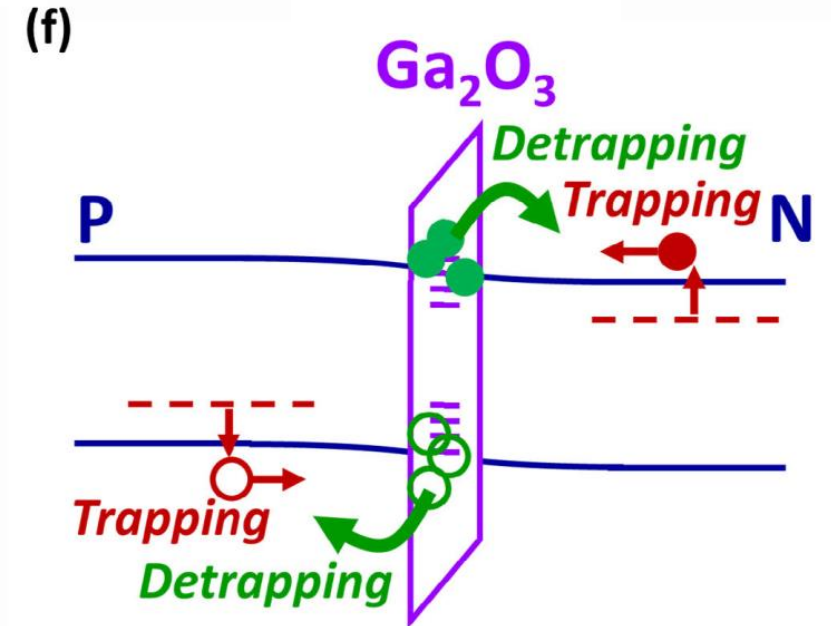
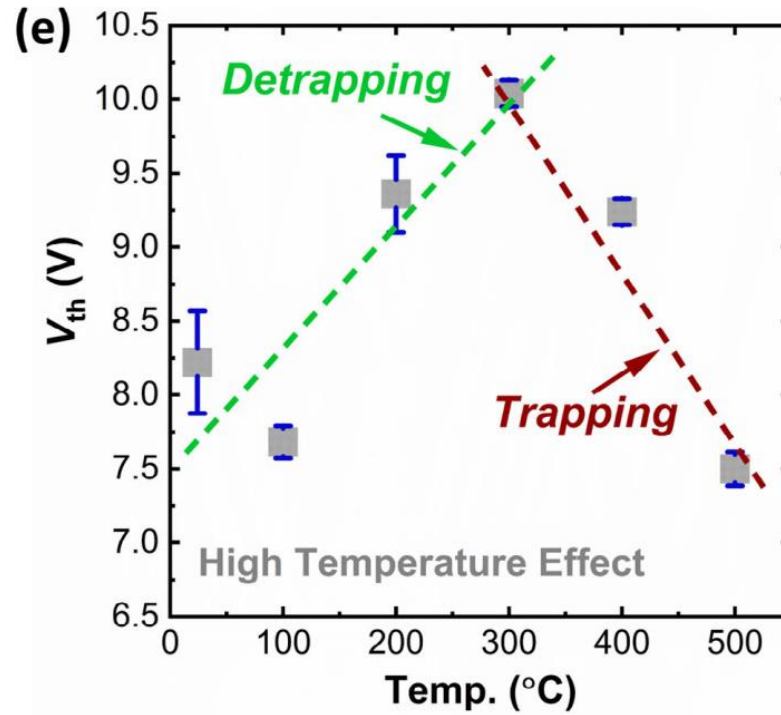
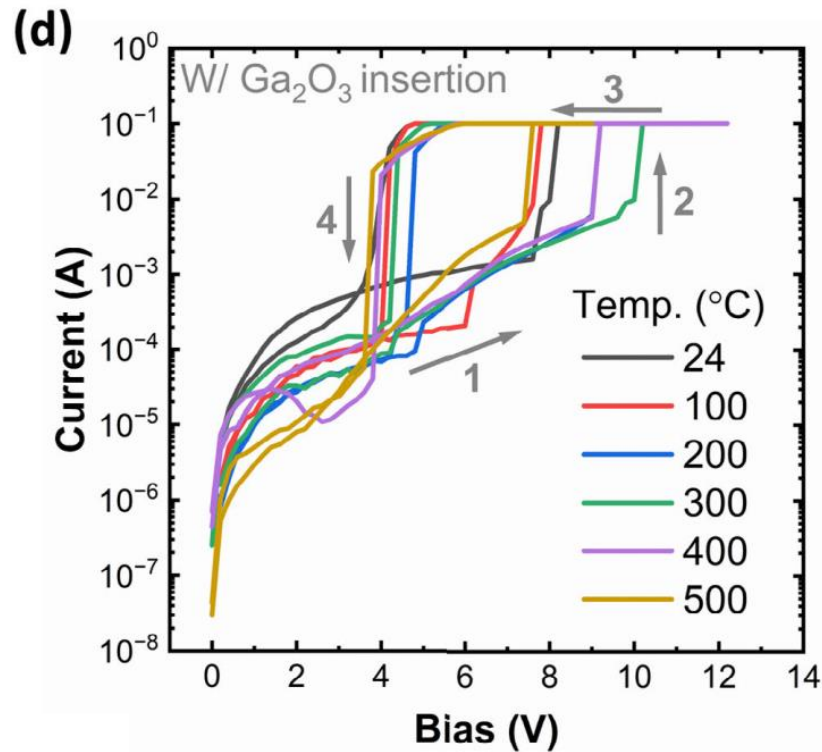
K. Fu, et al., IEEE Transactions on Electron Devices 71.3 (2023): 1641-1645.

# Enhanced GaN Memory Behavior up to 500 C



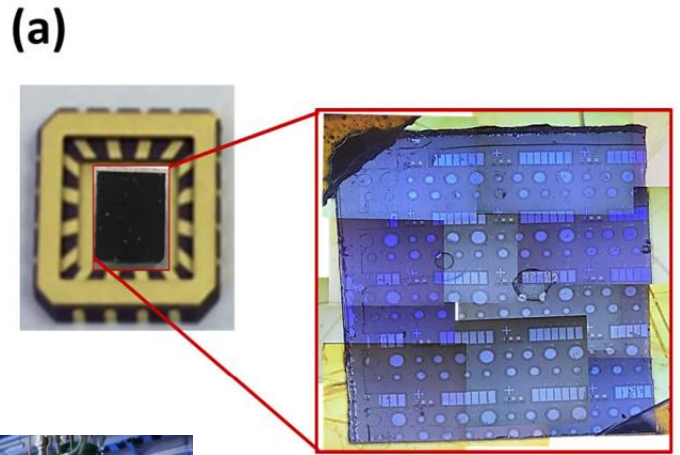
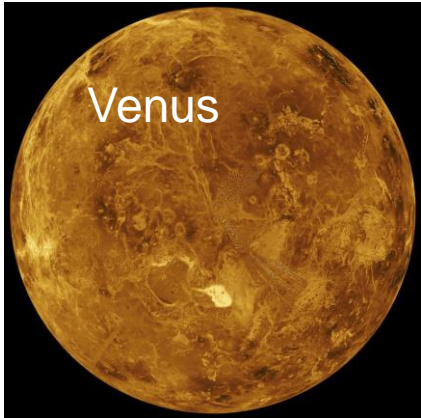
❑ The Ga<sub>2</sub>O<sub>3</sub> interlayer was found to be effective in improving the high-temperature performance up to 500 C, but...

# Enhanced GaN Memory Behavior up to 500 C

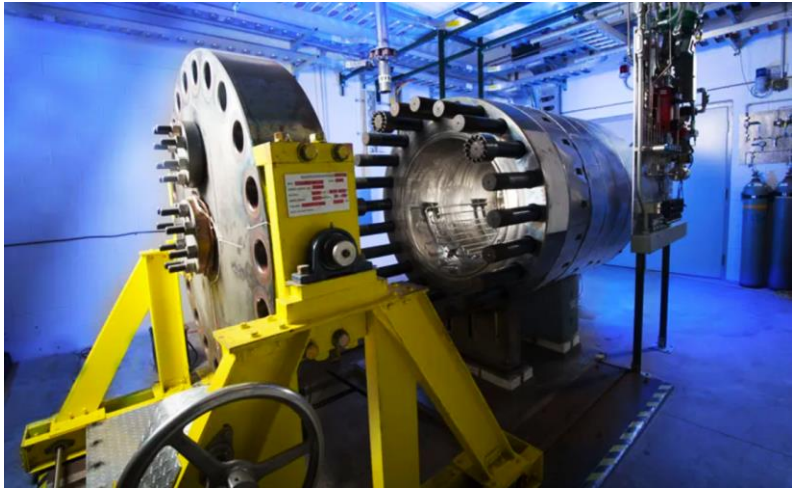


- ❑ 25 C–300 C: the detrapping from interfacial traps increased  $V_{th}$  at.
- ❑ 300 C–500 C: thermally activated intrinsic carrier densities in p-GaN and n-GaN increase. The **injection of thermal activation carriers** into traps could decrease the  $V_{th}$
- ❑ The device performance **returns** to its initial values as the temperature decreases to room temperature.

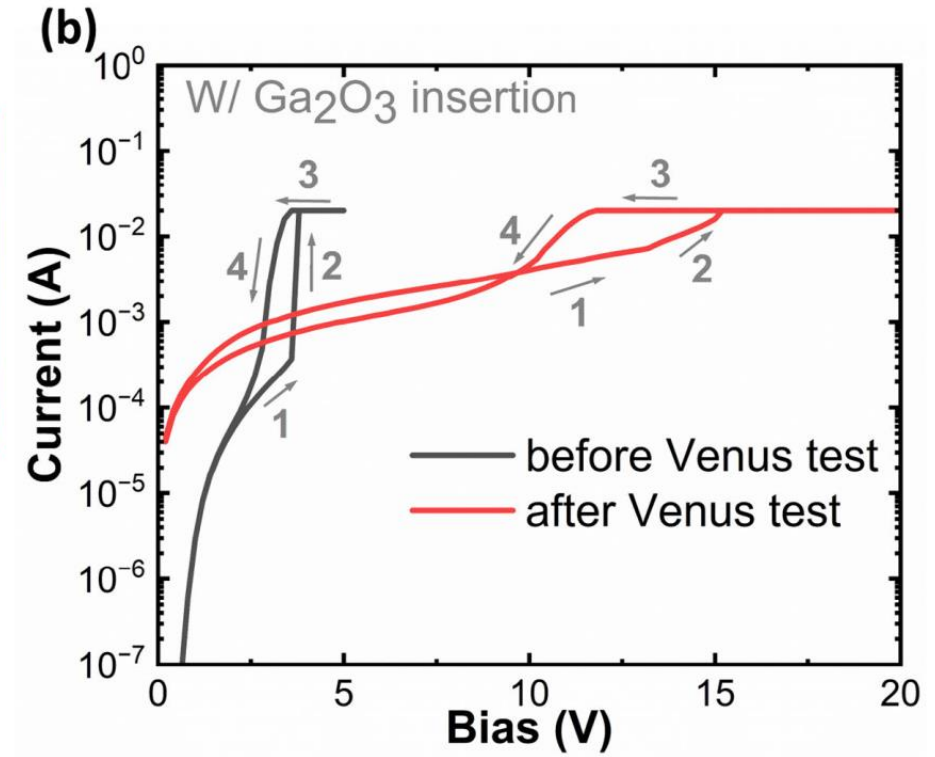
# Enhanced GaN Memory Behavior up to 500 C



*after 10 days*



**NASA Glenn Extreme Environments Rig (GEER) for Venus**  
(460 C, ~ 92 atm., containing CO<sub>2</sub>/N<sub>2</sub>/SO<sub>2</sub> etc.)

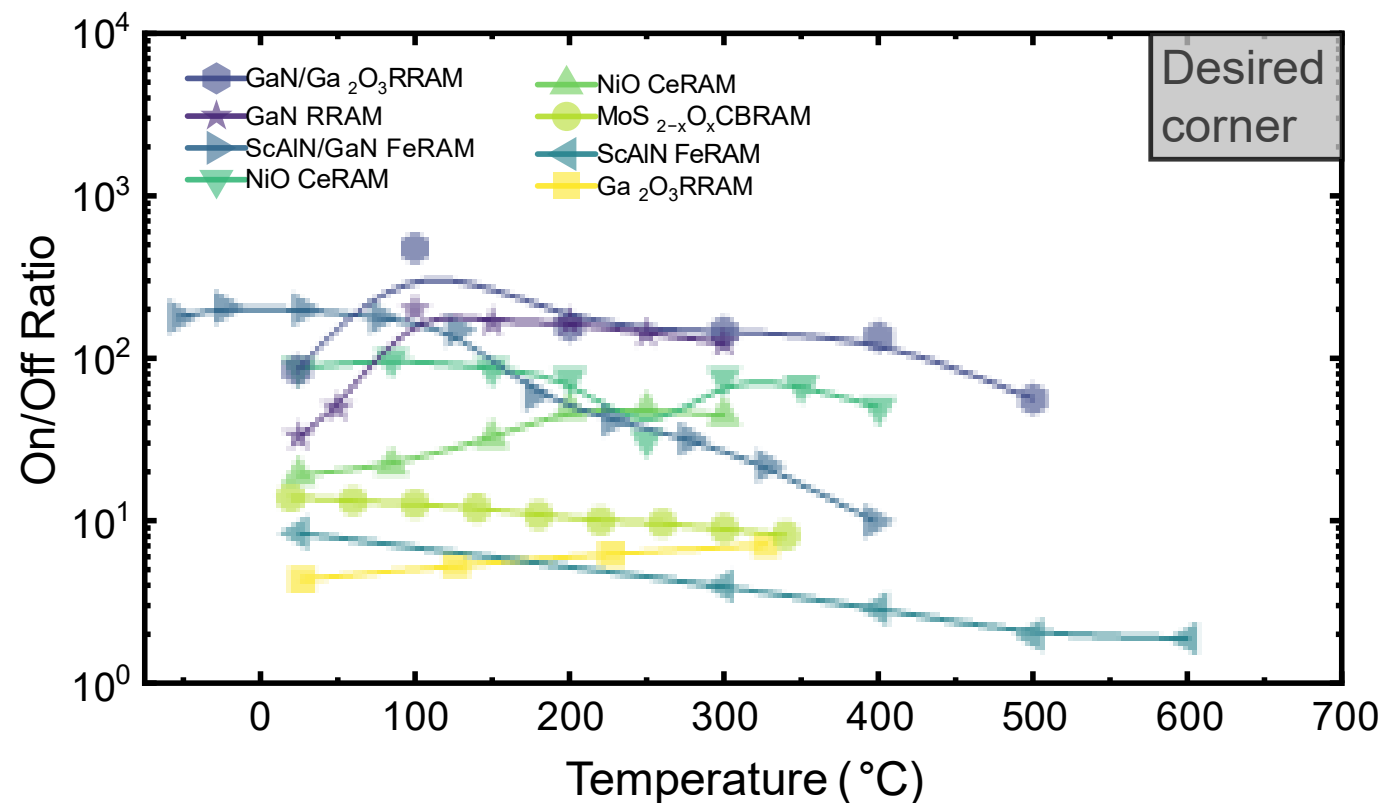


- Memory behavior;  $V_{th}$  and  $V_{hold}$  are significantly increased
- Possible reasons (no passivation): p-GaN conductivity degradation, surface damage, increased trapping density at the regrown interface, and/or electrode metal degradation

<https://science.nasa.gov/science-research/science-enabling-technology/hottech-attempts-to-tackle-venus/>

# Summary

- ❑ Observed resistive switching and memory behaviors in GaN p-n diodes with regrowth interface.
- ❑ Endurance and high temperature test: 1000 cycles; up to 300 C; small fluctuation.
- ❑ Mechanism: trapping vs de-trapping.
- ❑ Ga<sub>2</sub>O<sub>3</sub> insertion is effective to enhance the operation temperature up to 500 C.
- ❑ The GaN/Ga<sub>2</sub>O<sub>3</sub> memory survived in Venus environment for 10 days but shows severe degradation; passivation may improve the performance.
- ❑ New materials for high temperature...



## ***Rice / ASU***

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Xuanqi Huang  
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## ***MIT***

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Mengyang Yuan  
Qingyun Xie  
John Niroula



*NASA HOTTech Program  
(grant number 80NSSC17K0768)*



*ARPAe PNDIODES  
(grant number DE-AR0000868)*



*Looking forward to collaborating on UWBG*

