



Semiconductor
Research
Corporation

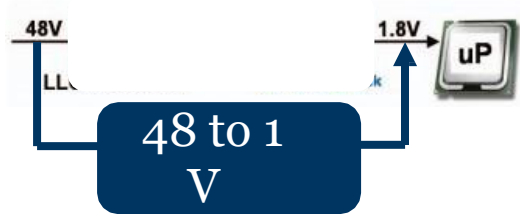
Design of a GaN-Based High Current Low Voltage Two-Stage Converter with 3D Heterogeneous Integration

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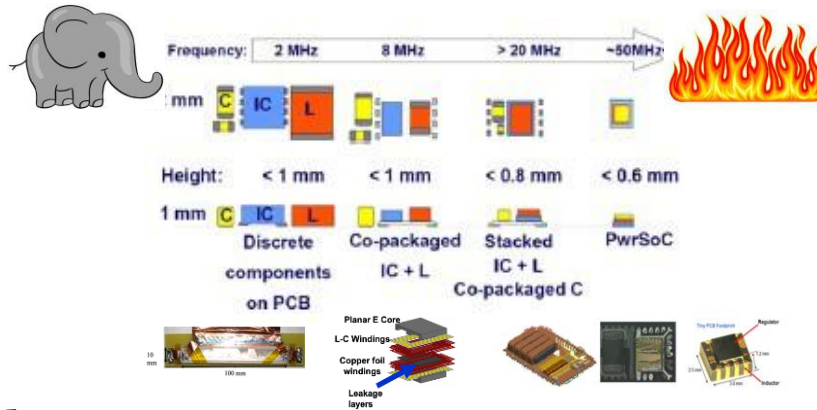
April 17, 2025

Background & Our Solution

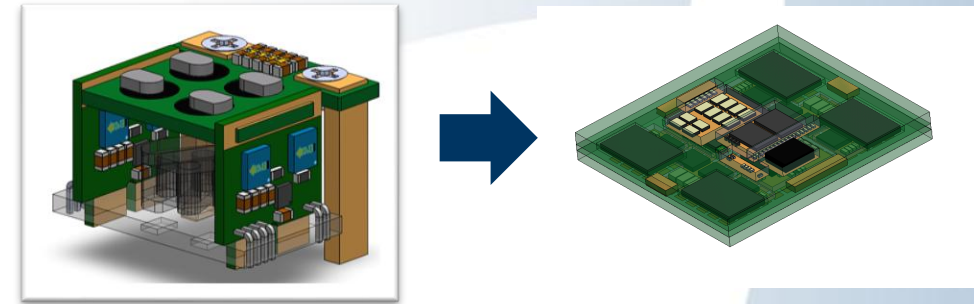
- State-of-the-Art



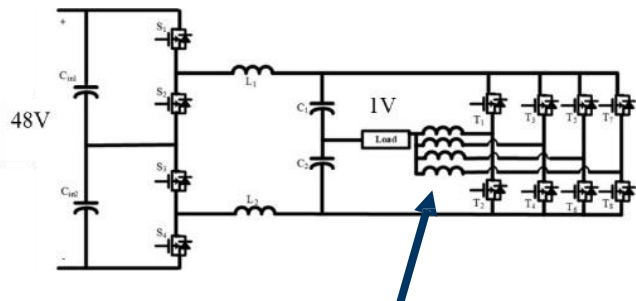
- Issues



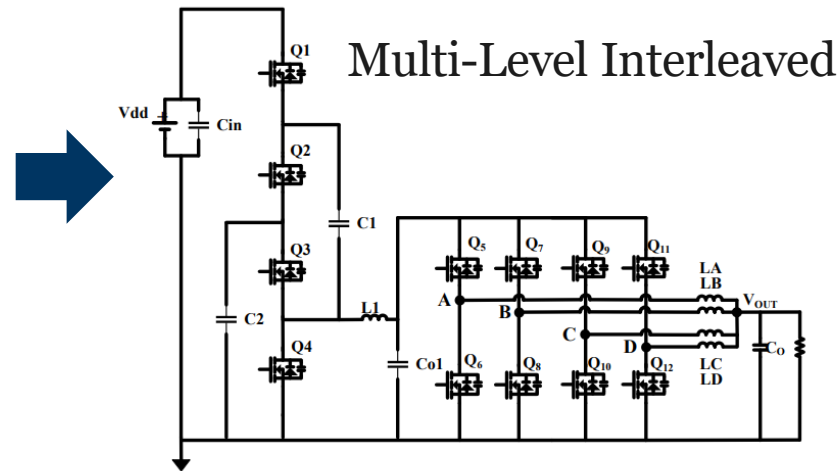
- Integration/ Pkg in this Task



- Topology(ies) in this Task



Soft-switching
Interleaved



Desired Objectives

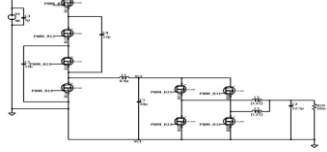
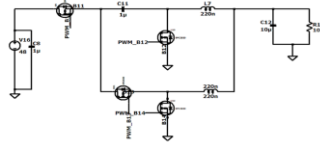
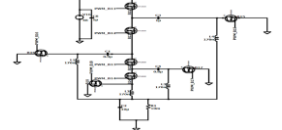
- Power density 10 A/mm² and efficiency > 92%
- Low-cost 2.5D package for VR PwrSiP
- New approaches for magnetic/module integration and fabrication

Topology Review and Selection

Objectives:

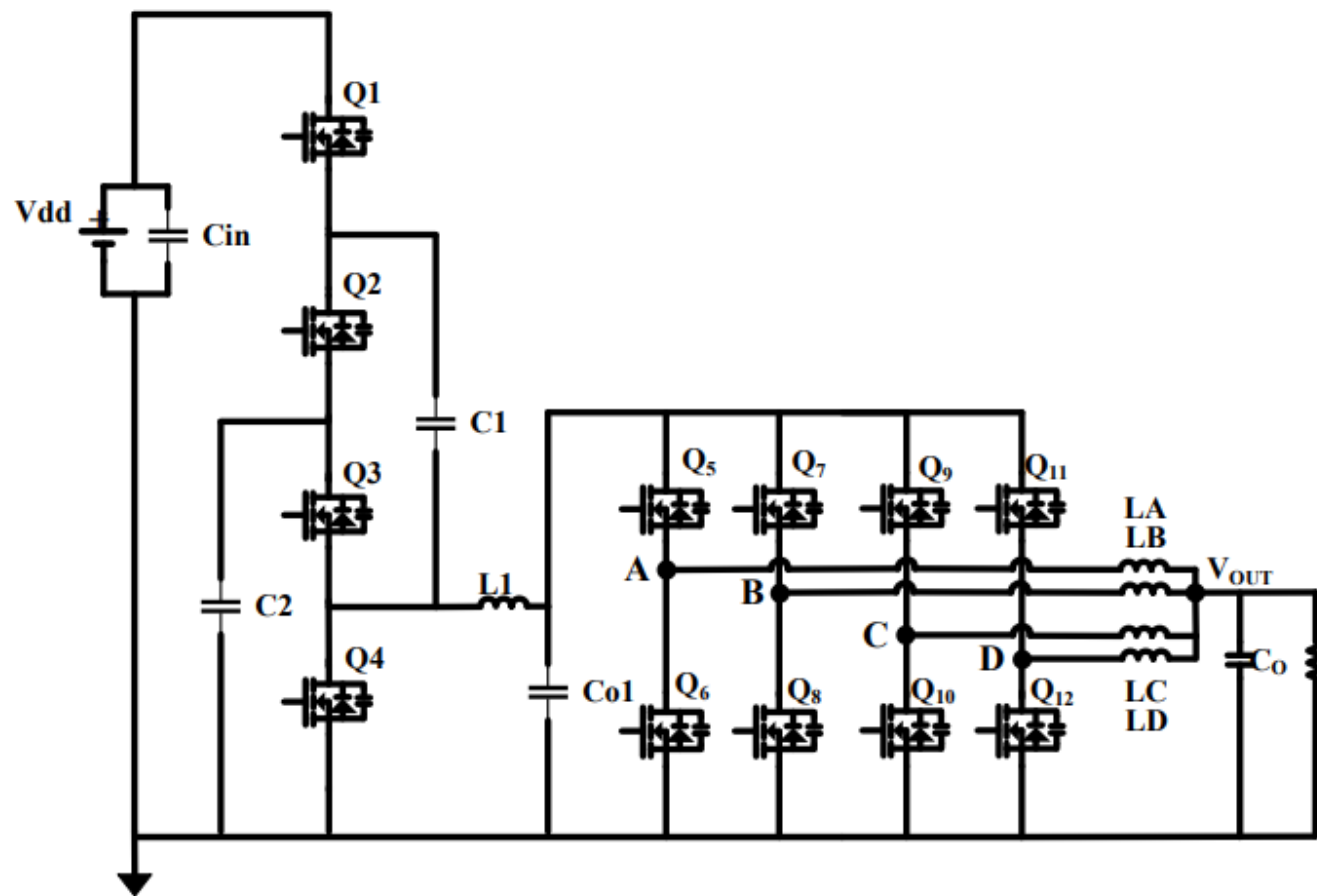
1. Review converter topologies best suited for high current.
2. Selection of appropriate topology, with high power density in mind.

High Current/Frequency Converters and Simulation

LTSpice simulation	Topology	Switch capacitor + multiphase buck 	Series capacitor buck 	Dual Phase Multi- Inductor Hybrid (DP-MIH) 
Topology details	Voltage conversion	48V- 1V	48V- 1V	48V- 1V
	Output current (A)	100	100	100
	Switching frequency (Hz)	1 M (both stages)	1 M	1 M
	Device in simulation	EPC 2020	EPC 2020	EPC 2020
	D in simulation	1 st stage: 0.25 2 nd stage: 0.31	0.095	0.15
	# of switches	8	4	8
	Value of inductors (<i>H</i>)	1 st stage: 0.4μ (×1) 2 nd stage: 0.05μ (×2)	0.22μ (×2)	0.17μ (×4)
	Value of capacitors (<i>F</i>)	1 st stage: 12μ (×2) Intermediate: 10μ (×1) 2 nd stage: Cout= 12.5μ (×1)	1μ (×1) Cout= 10μ (×1)	1μ/ 0.9μ/ 0.8μ (×1 for each) Cout= 10μ (×1)
	Voltage ripple	7.0% (Intermediate); 3.6% (Output)	1.6%	3.0%

Results of Topology Simulation:

- Switch capacitor Hybrid + Multiphase buck



	Switching Sequence
First Stage	Q_1Q_3, Q_2Q_4
Second Stage	$Q_5/Q_7/Q_9/Q_{11}, Q_6/Q_8/Q_{10}$ Q_{12} (Interleaved)

- ✓ High Step-down ratio and high efficiency
- ✓ Current ripple cancelation.
- ✓ Low component count
- ✓ Coupling inductor capable.

✓ Initial Current Target of 100A @ 1V

Multi-phase Interleaved Converter

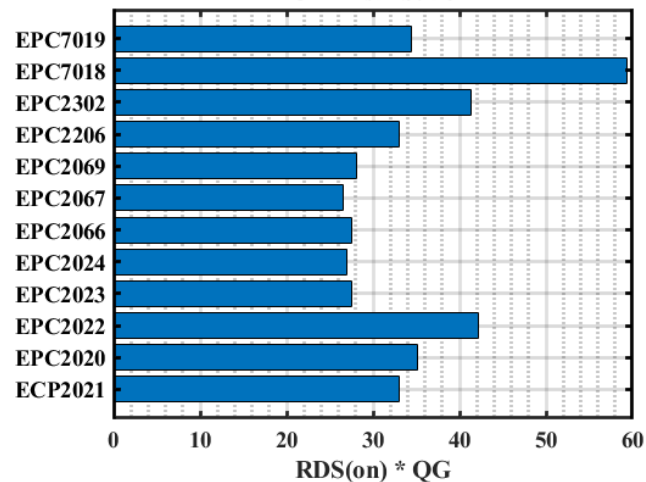
Objectives:

1. Optimization of device/phase/surface area for high frequency operation.
2. GaN PCB Optimization for high frequency.
3. High frequency Operation verification.

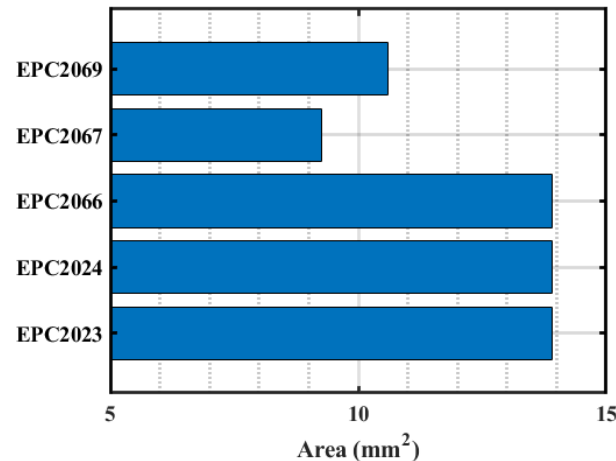
Multiphase Buck Power Distribution

- Phase/Efficiency vs. Surface Area

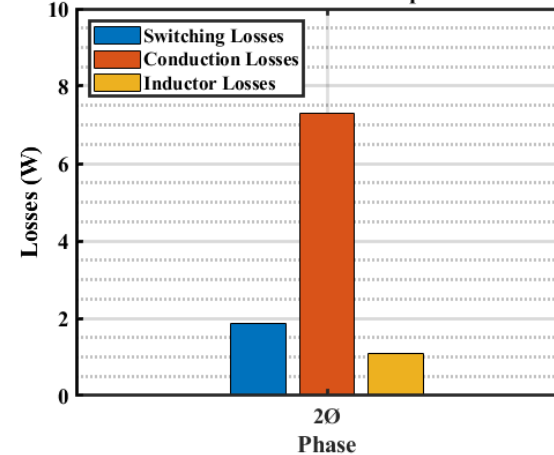
FOM Distribution



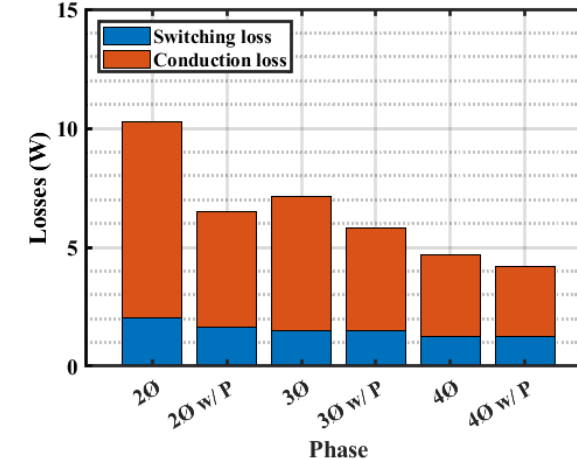
Area Distribution



Loss distribution for 2 phases



Power Losses vs Phase



Lessons Learned

- ✓ Conduction losses dominate the majority of the loss at this stage.
- ✓ EPC GaN HEMT devices offer the smallest $R_{ds(on)} * Q_G$ FOM relative to surface area.

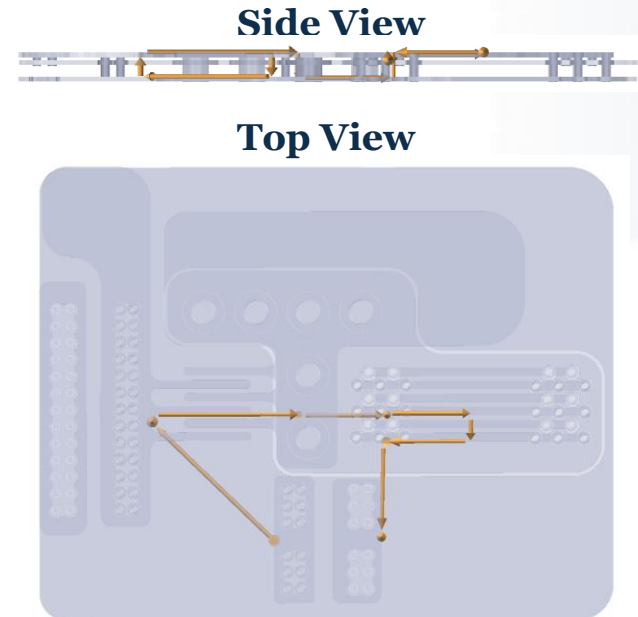
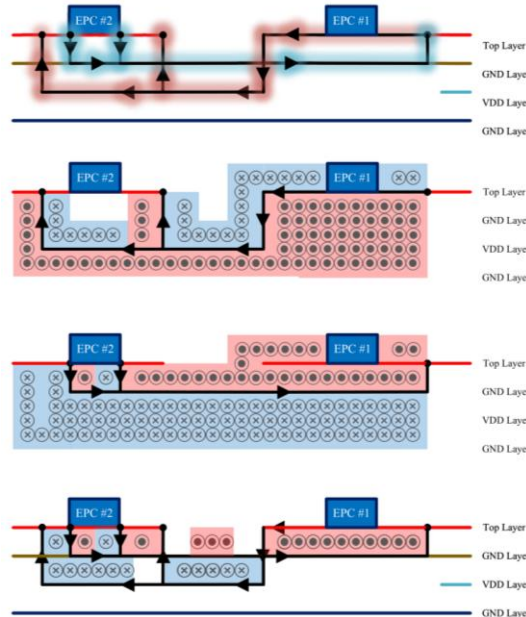
To what degree to do multiphase operation offer diminishing returns?

- ✓ At MHz range, 4 phases operation is the crossing point where switching losses become sizeable to conduction losses.
- ✓ Paralleling devices offers little reduction in conduction losses pass 4 phases.

Initial Testing Conditions	
HEMT Results	Inductor Results
$I_{peak} = 65 \text{ A}$	$L_{1,2} = 50 \text{ nH}$
$V_{peak} = 12 \text{ V}$	$I_{avg} = 51.806 \text{ A}$

GaN Power Stage Layout and Optimization

- Reaching MHz operation



Extracted Inductance	DC R [mOH M]	DC L [nH]
L_{p1}	0.0220 5	0.06737
L_{p2}	0.0933 5	1.14042
L_{p3}	0.1267 7	0.68224

- ✓ 1 nH range and Sub 1 nH vertical loop parasitic inductance requires exploiting flux cancelation both vertical and lateral through the PCB board.
- ✓ FEA simulation predict obtain 1.9 nH implementing the proposed layout.

Verification of the proposed layout through hardware results is needed to verify the prediction of the FEA simulation

High Frequency Operation at Different Phases.

- ✓ 4 Phase operation was verified at low current.
- ✓ 1.8 nH vertical inductance was derived from the operating waveforms; validating FEA prediction.

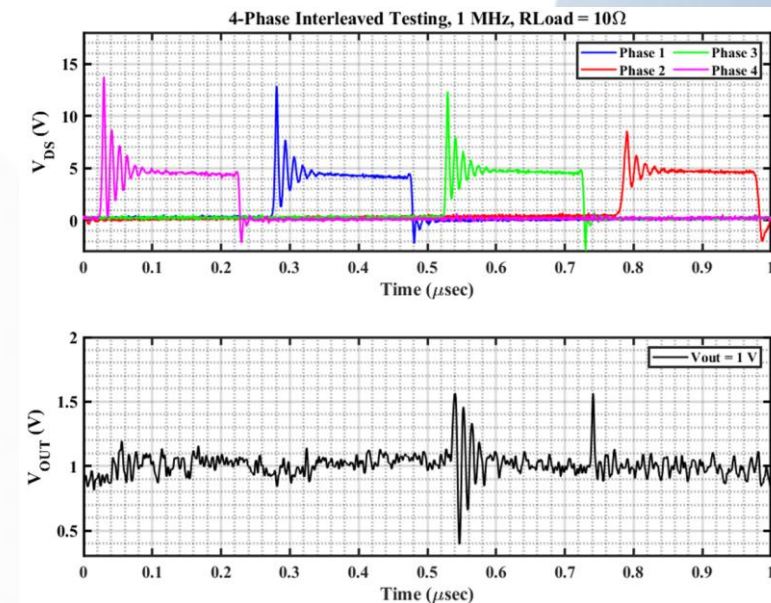
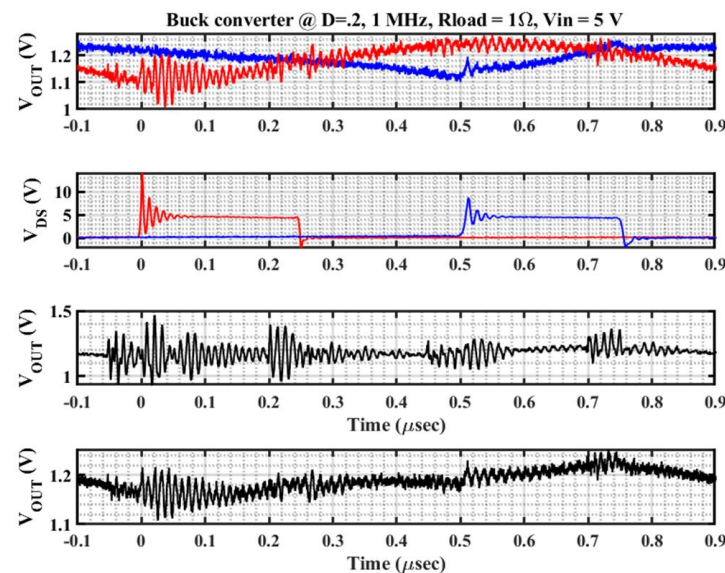
Single Half Bridge



4 Phase Implementation



Package size limits top side cooling limiting full current operation.
Regulation of this stage would help with current balancing of each inductor.

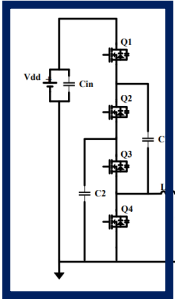
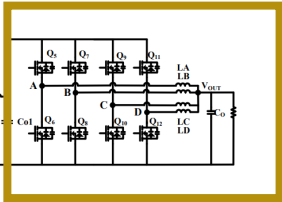


Magnetic/Module Design

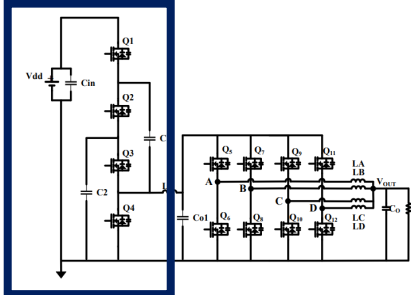
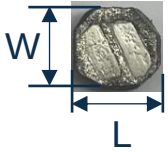
Objectives:

1. Flux Optimization of Magnetic prototype.
2. Comparison of Magnetic prototype to Commercial Designs
3. 1st Iteration of Packaging Model.

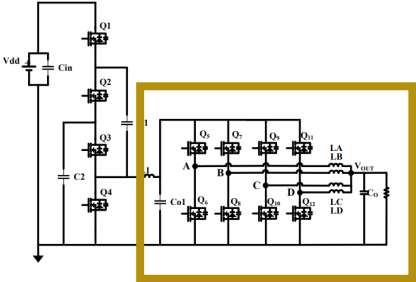
Inductors Characteristic Summary

1st stage  2nd stage 	1st stage: 48 V- 5 V Top Bottom Side  L x W x H: 11 x 10 x 7 (mm)	2nd stage: 5 V- 1 V Top/Bottom Side  D= 5 mm; H= 3 mm
Basic Information	Core: Laminated IFL16 (TDK) Winding: Cu litz wire # of turns: 2	Core: Laminated IFL16 (TDK) Winding: Ag ink Cu litz wire # of turns: 1
Targeted Inductance (nH) (LTspice)	400	25
Simulated Inductance (nH) (Maxwell @ 1MHz)	488	53.1
Tested Inductance (nH) (VNA @ 1MHz)	454	37
DCR (mΩ) (Four-point method)	0.51	0.11
DC Current Carrying Capability (DC power supply; thermal camera)	Up to 30A, continuously for 15 mins Body temp: 55°C (ΔT= 30°C)	Printed Ag winding: Up to 30A, continuously for 15 mins Body temp: 66.6 °C (ΔT= 41.60°C)
Proposed Integration Method	Surface Mount	Embedded

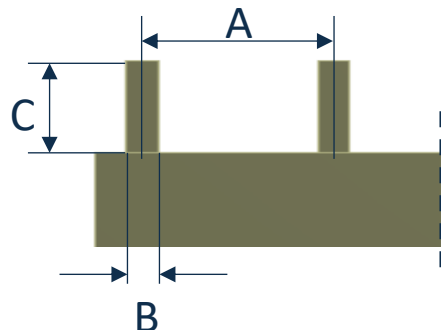
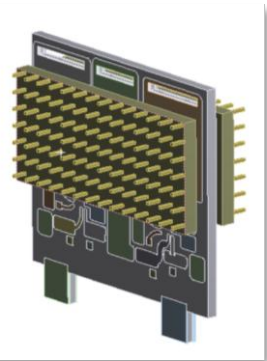
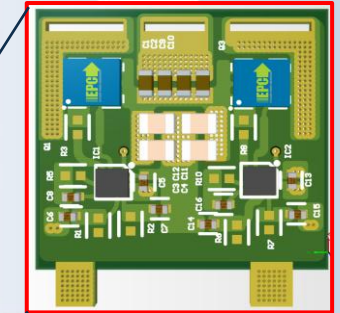
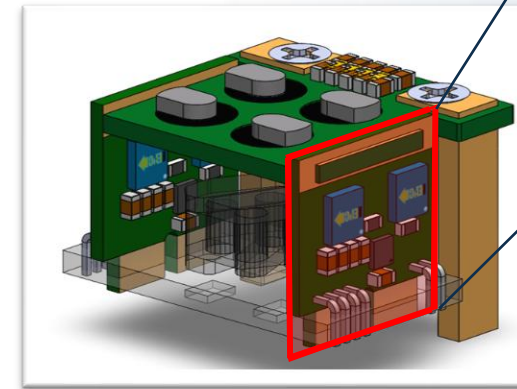
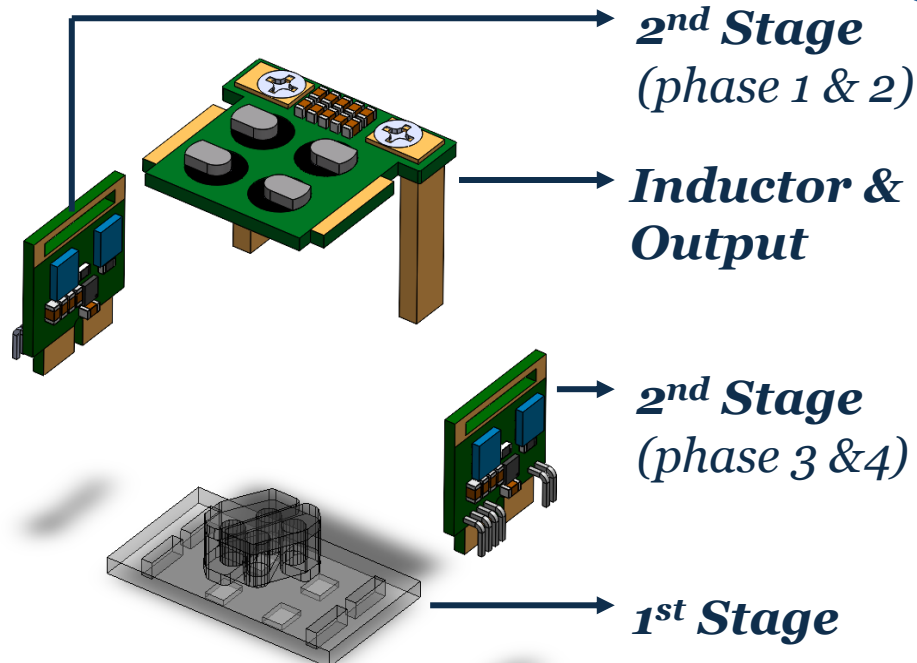
Comparison of Magnetic prototype to Commercial Designs

Inductor for 1st stage: 48 V- 5 V		
1st stage 	Würth Elektronik (744355147)  L x W x H: 13 x 12.8 x 6.5 mm	TopBottomSide  L x W x H: 11 x 10 x 7 (mm)
Basic Information	Core: N/A Winding: Cu # of turns: N/A	Core: Laminated IFL16 (TDK) Winding: Cu litz wire # of turns: 2
Tested Inductance (nH) <i>(Impedance Analyzer @ 1MHz)</i>	470	454
Inductance/Volume (nH/mm ³)	0.43	0.59 (37% ↑)
DCR (mΩ) <i>(Four-point method)</i>	0.67	0.51

Comparison of Magnetic prototype to Commercial Designs Pt. 2

Inductor for 2nd stage: 5 V- 1 V		
 2nd stage	Würth Elektronik (744340300025)  L x W x H: 5 x 3.1 x 3 mm	Top/Bottom Side   D= 5 mm; H= 2.5 mm
Basic Information	Core: N/A Winding: Cu # of turns: N/A	Core: Laminated IFL16 (TDK) Winding: Cu litz wire # of turns: 1
Tested Inductance (nH) <i>(Impedance Analyzer @ 1MHz)</i>	25.9 (27.0/ 23.2/ 27.5)	40.5 (38.2/ 37.0/46.5)
Inductance/Volume (nH/mm ³)	0.55	0.82 (48% ↑)
DCR (mΩ) <i>(Four-point method)</i>	0.27	0.11
Proposed Integration Method	SMT	Embedded

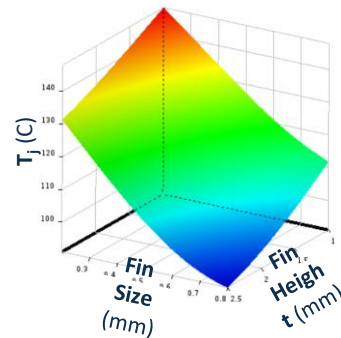
1st Iteration for Packaging Integration



Fin-to-fin pitch: $A = 1.2 \text{ mm}$ (constant)

Fin width: $B = 0.2\text{-}0.8 \text{ mm}$ (variable)

Fin height: $C = 1\text{-}2.5 \text{ mm}$ (variable)



- ✓ Initial Design allows for double sided cooling of both devices and inductor
- ✓ Min $T_{j,\text{max}}$ is 91°C @ $B=0.8\text{mm}$ and $C=2.5\text{mm}$
- ✓ Easy to manufacture

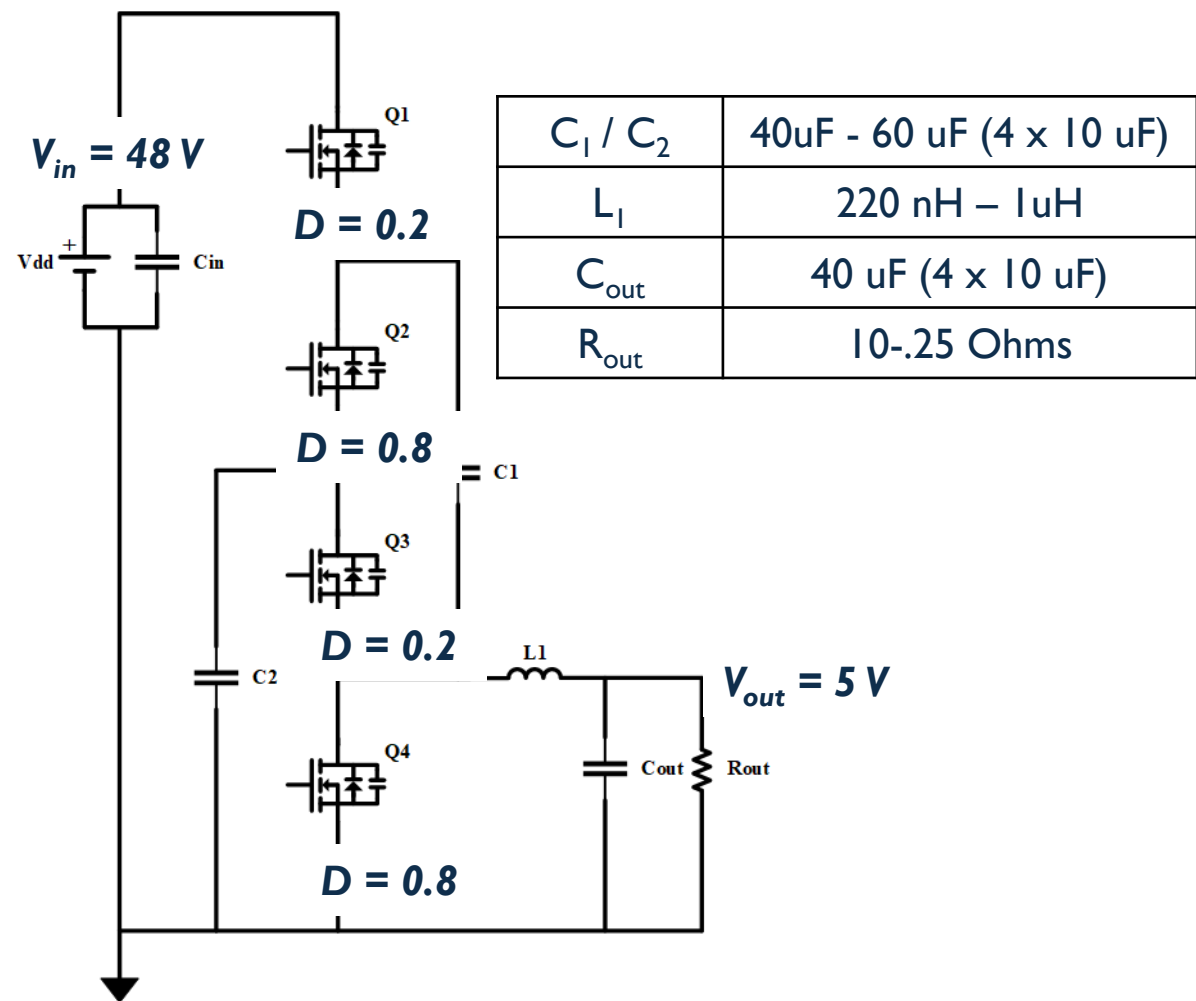
Not optimized in terms of the power density which considers the thickness.

Switched Capacitor Hybrid Converter

Objectives:

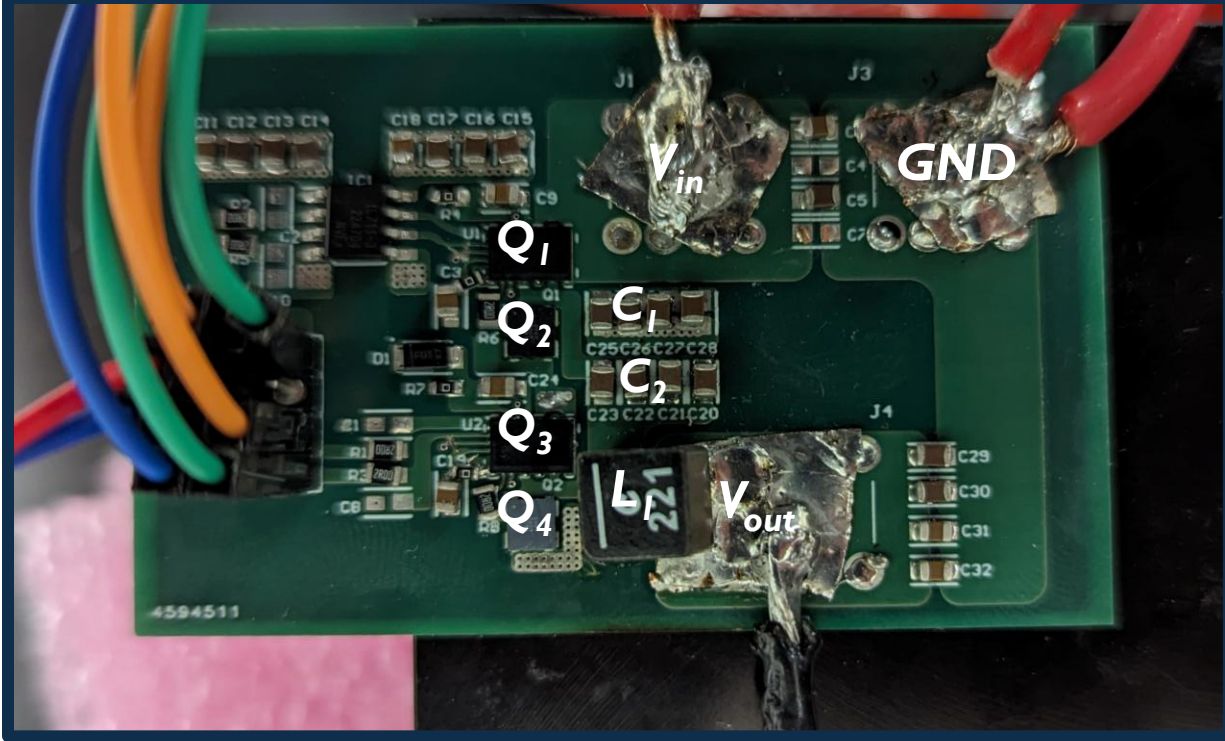
1. Initial Prototype based on lowest surface area.
2. Thermal Analysis.
3. Low Power Operation.
4. Challenges and Optimization with small components

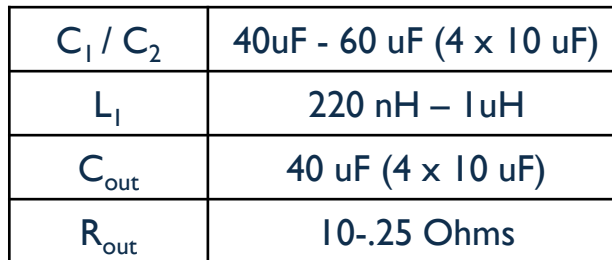
48v to 5v stage: Discrete Version of Switched Capacitor Buck Converter



C_1 / C_2	40uF - 60 uF (4 x 10 uF)
L_1	220 nH – 1uH
C_{out}	40 uF (4 x 10 uF)
R_{out}	10-.25 Ohms

Switched Capacitor Buck Converter Prototype





	I_{RMS} (A)
Q1	2.5736
Q2	1.2703
Q3	2.5736
Q4	10.096

$P_{\text{total Q4}} = 0.1784 \text{ W}$ | $T_{\text{Q4}} = 33.6 \text{ C}$

EPC 2067's
 $R_{DSon} = 1.5 \text{ m}\Omega$

	I_{RMS} (A)
Q1	6.4052
Q2	1.2703
Q3	6.4052
Q4	25.272

$P_{\text{total Q4}} = 1.063 \text{ W}$ $T_{\text{Q4}} = 76 \text{ C}$

Low Current Thermal Analysis @ $R_{load} = 10$ and 1Ω

$R_{load} = 10 \text{ Ohm}$



Temperature of L = 44.6 °C

Temperature of Q_4 = 39.9 °C

$R_{load} = 1 \text{ Ohm}$

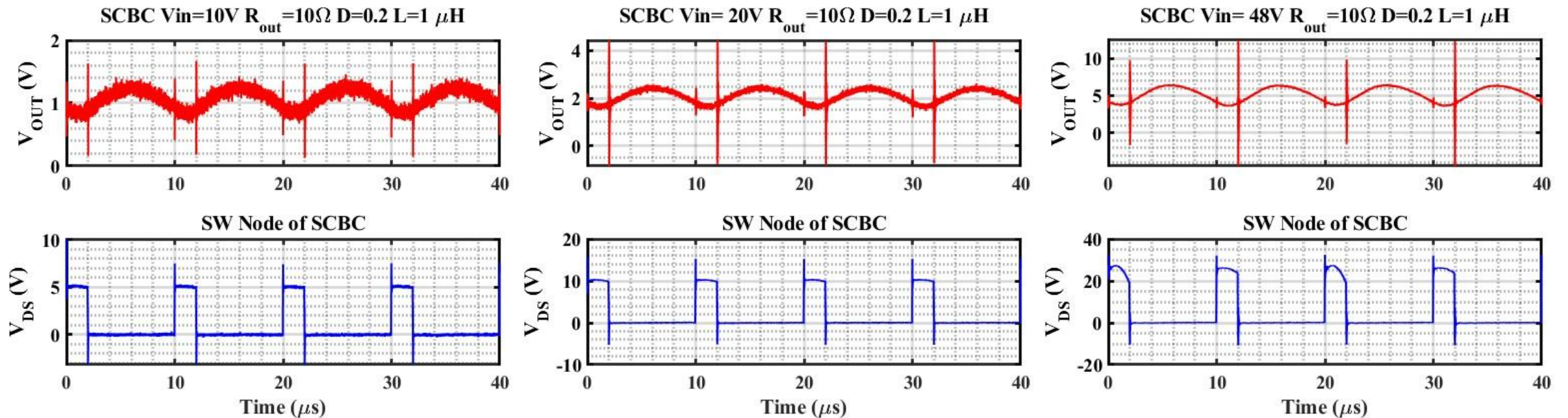


Temperature of L = 96.1 °C

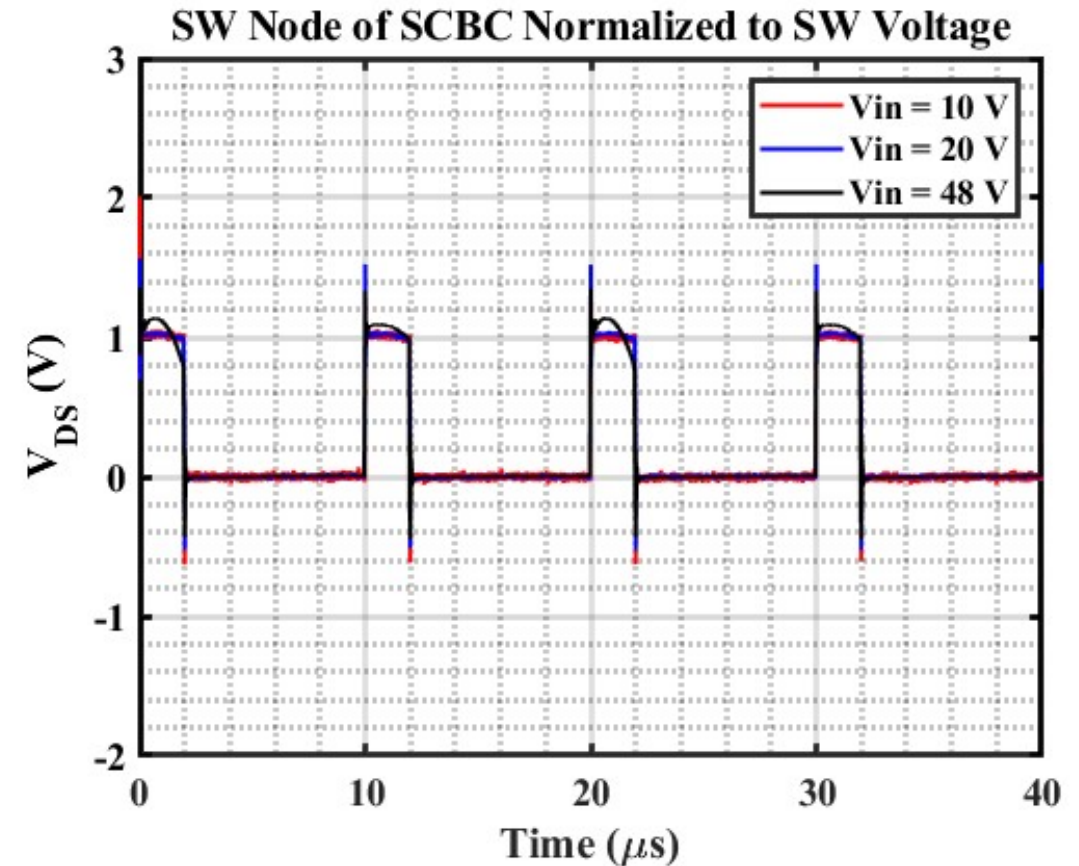
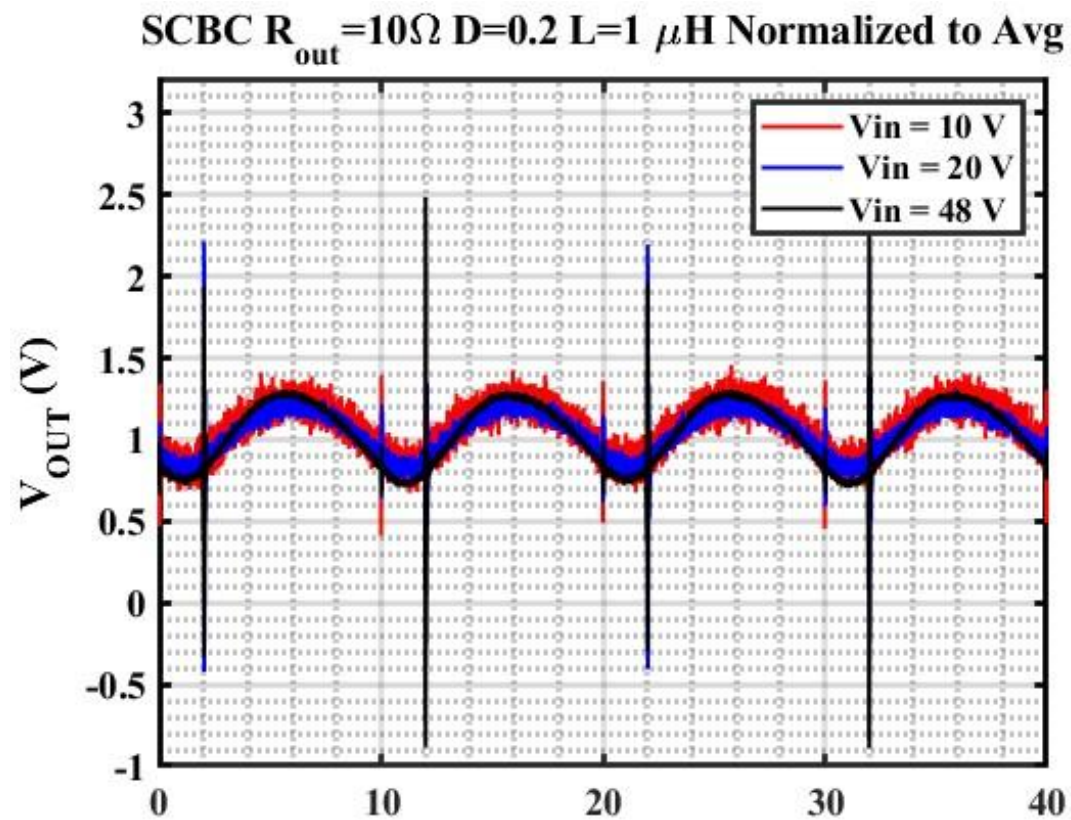
Temperature of Q_4 = 79.9 °C

Low Voltage & Current Operation @ $R_{load} = 10$ and 1Ω

- The L_2 value kept high to idealize the inductor as a constant current source.
- Higher V_{in} caused discharging at the switch node which varied over time.

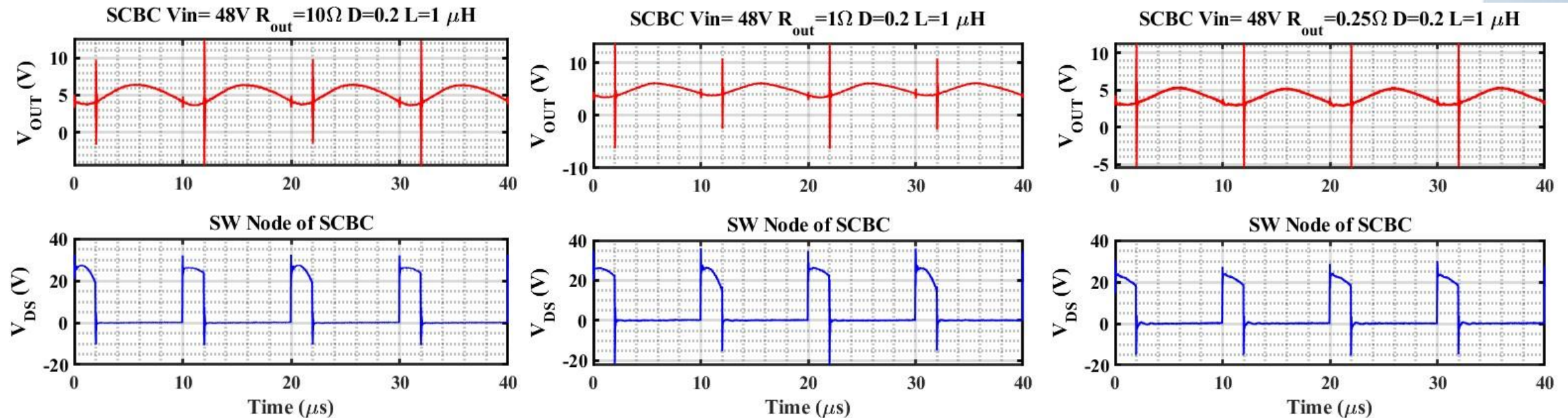


Low Voltage & Current Operation @ $R_{load} = 10$ and 1Ω

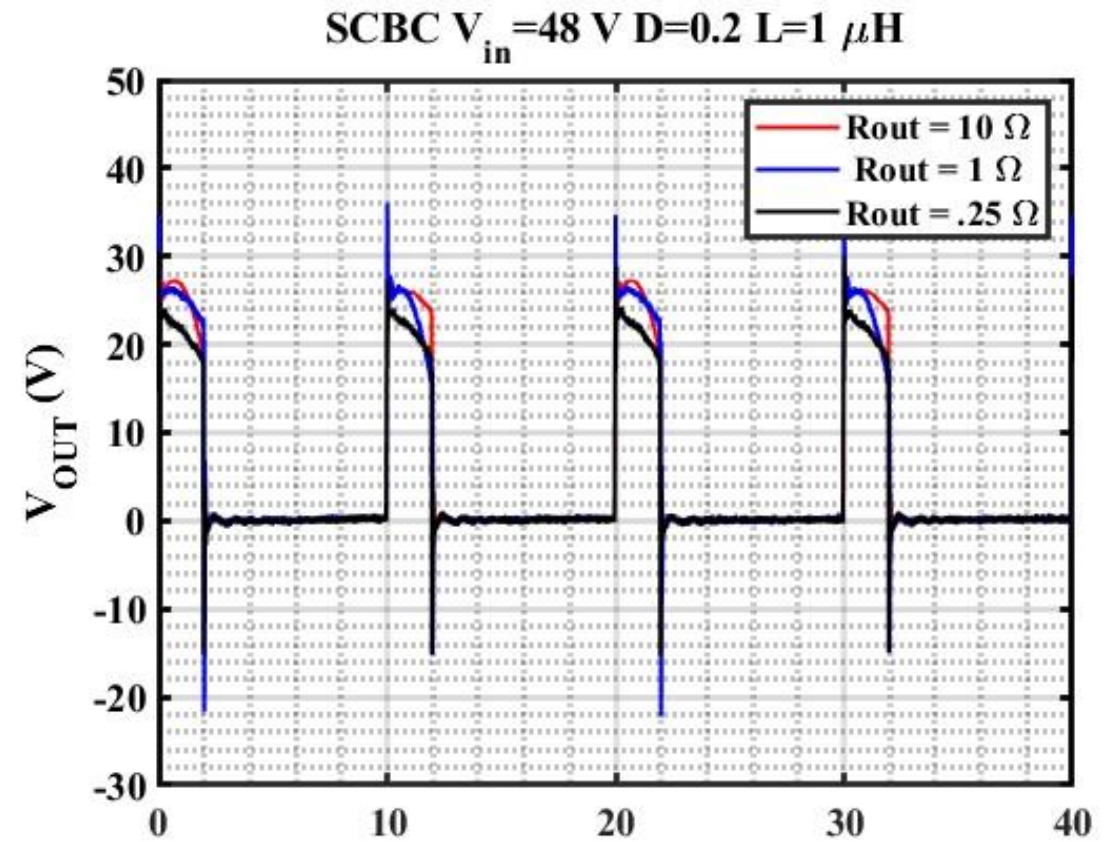
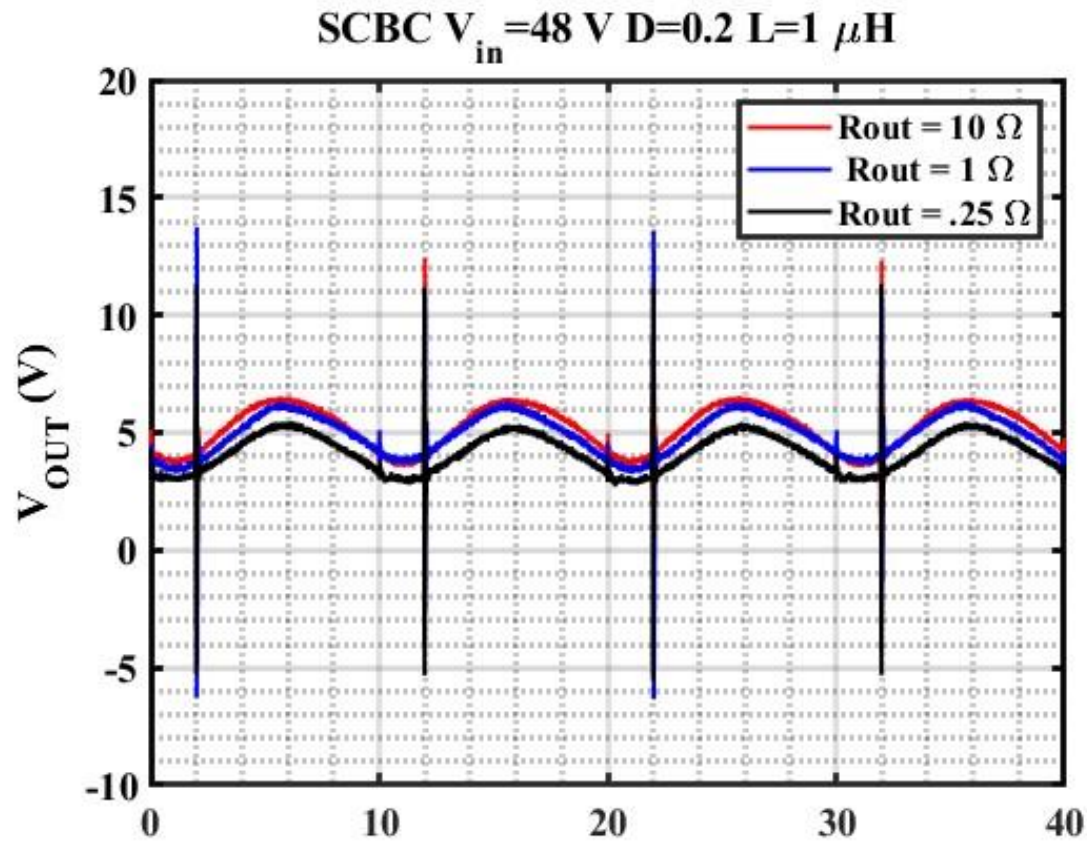


High Current Operation @ $R_{load} = 10-.25 \Omega$

- At 48V and full operation of $.25\Omega$ shows that this non-linear effect becomes worse as the load demand increases.
- This effect decrease the average V_{sw} causes changes to the output voltage.



High Current Operation @ $R_{load} = 10-.25 \Omega$



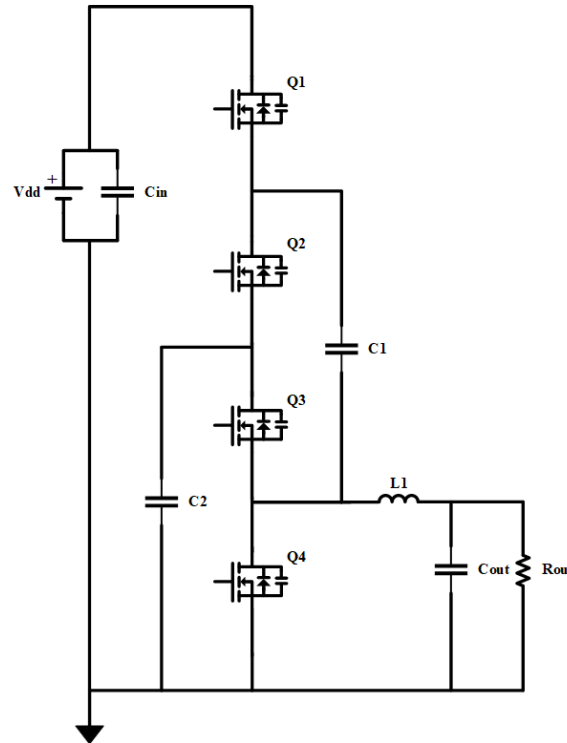
DC Bias Capacitance Change for MLC capacitors

Given $L1 = 1\mu\text{H}$, $C1/C2 = 40\mu\text{F}$:

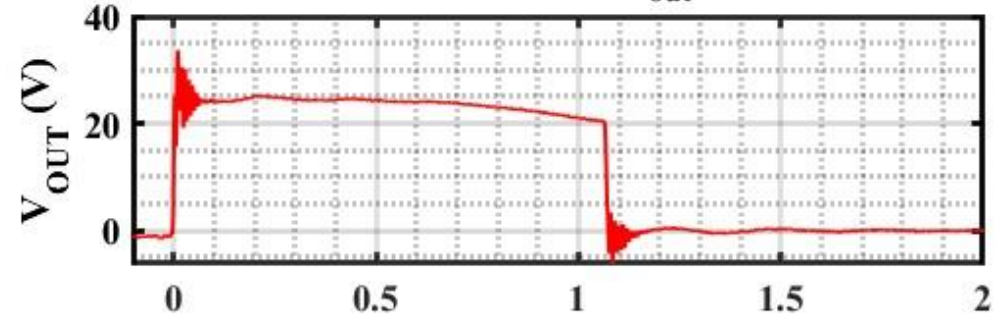
$$f_{\text{sw}} = 25.164 \text{ kHz}$$

This value is 10 times less than the current switching frequency of 200 kHz

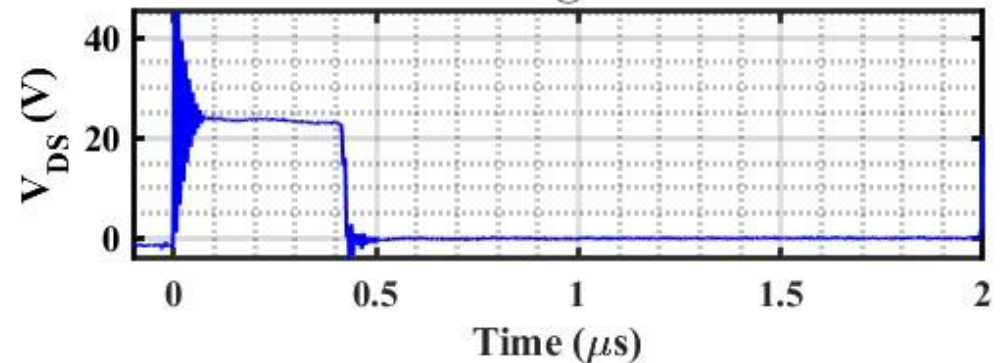
$$f_{\text{sw}} = \frac{1}{2\pi\sqrt{L1*\left(\frac{C1+C2}{2}\right)}}$$



SCBC SW @ 200 kHz $V_{\text{in}}=48\text{V}$ $R_{\text{out}}=10\Omega$ $D=0.2$ $L=1\mu\text{H}$



SW Node @ 500 kHz



o603 or lower MLCC case sizes can't be used given such a high reduction in capacitance change @ 24V

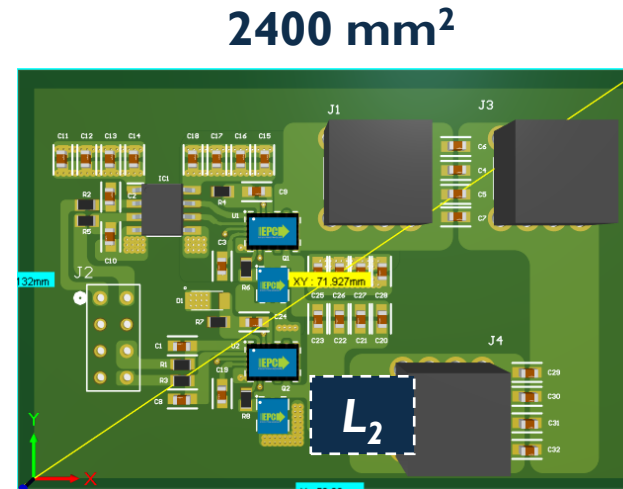
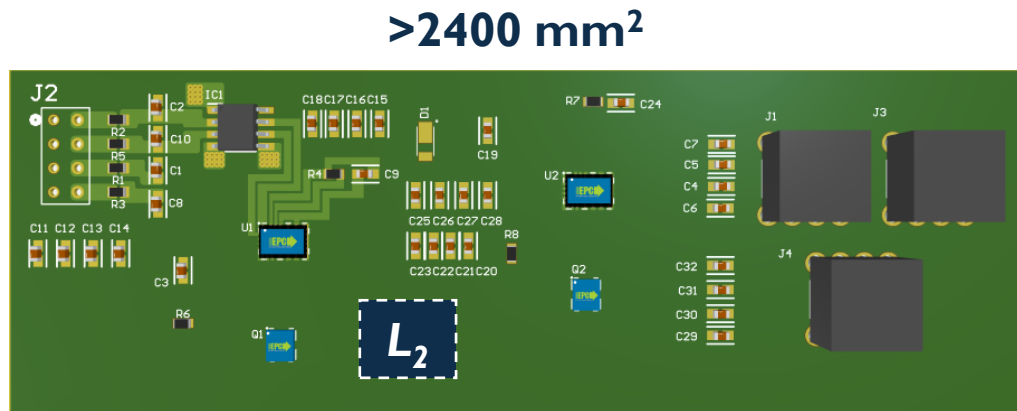
3D Heterogeneous iteration of Packaging Module

Objectives:

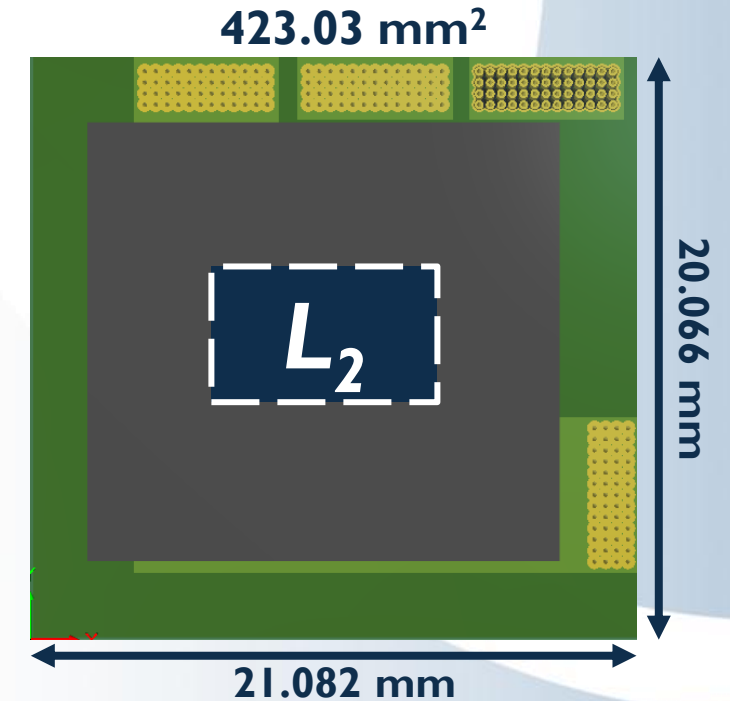
1. Optimization with Surface Area.
2. Optimization in Thickness.
3. Vertical “Active Substrate” Implementation

Optimization of Surface Area

- L_2 is the largest single element and is the limiting component in terms of area.
- L_2 is decided to be 400-600 nH due to the capabilities of the lab-made inductor.
- The goal is to try to fit entire switching components under this inductor.

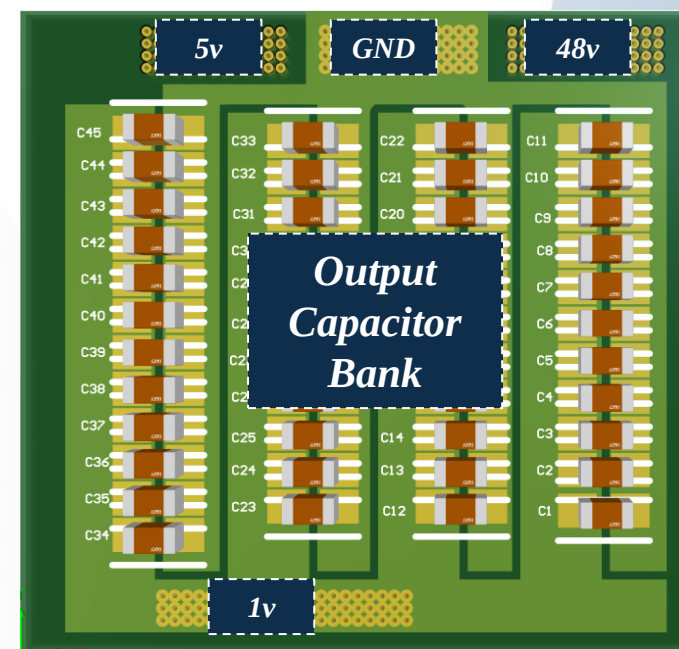
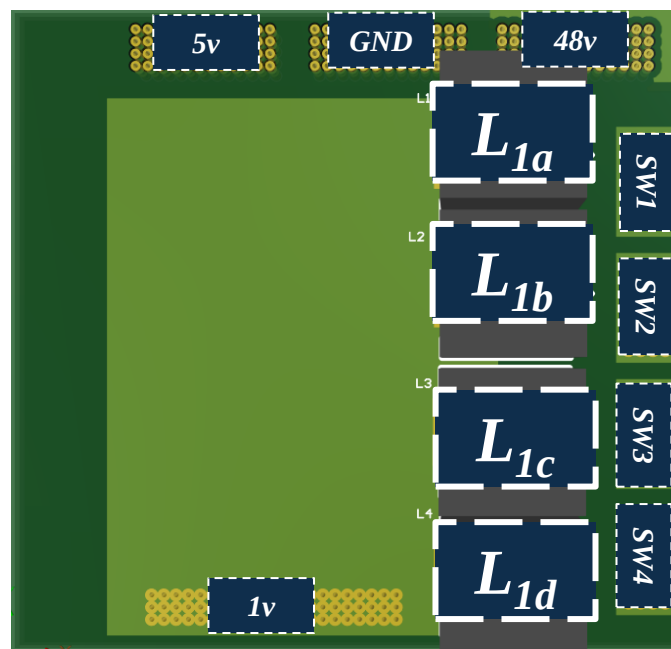
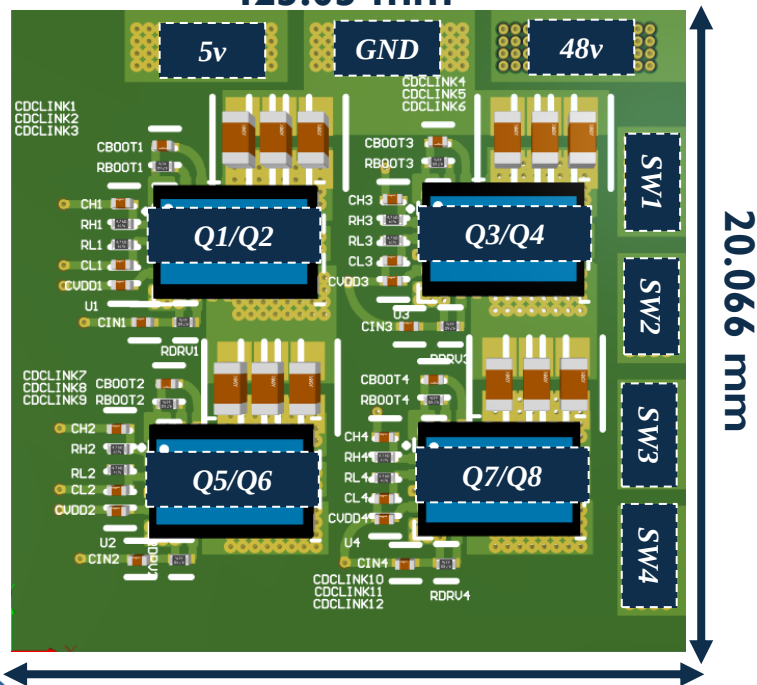
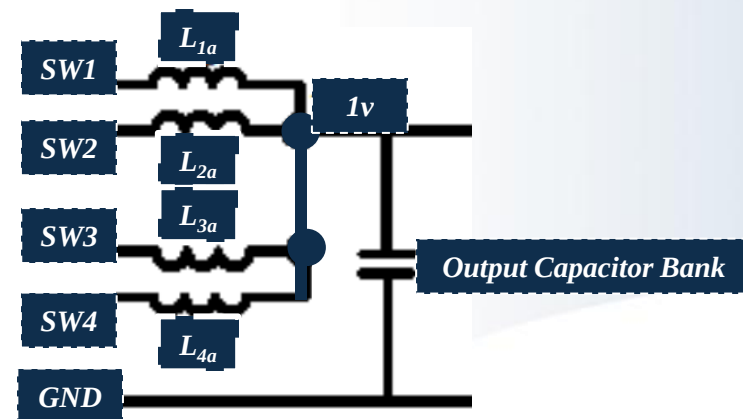
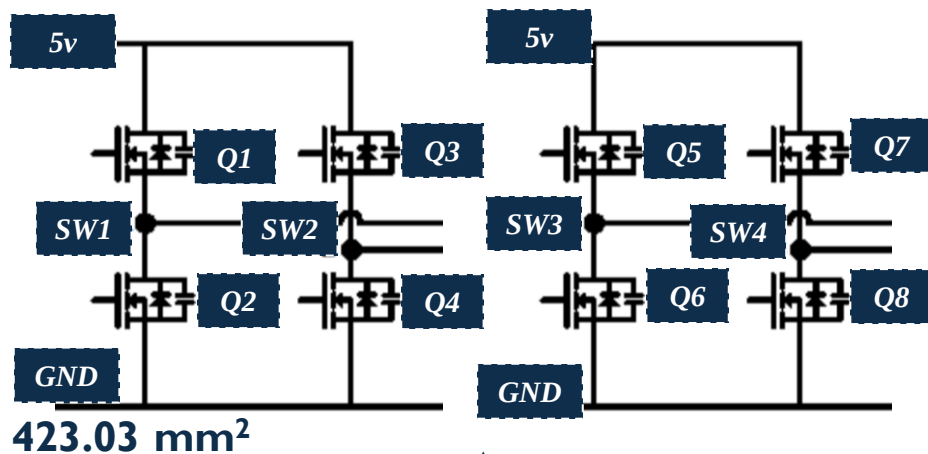


**Discrete
Version Tested**

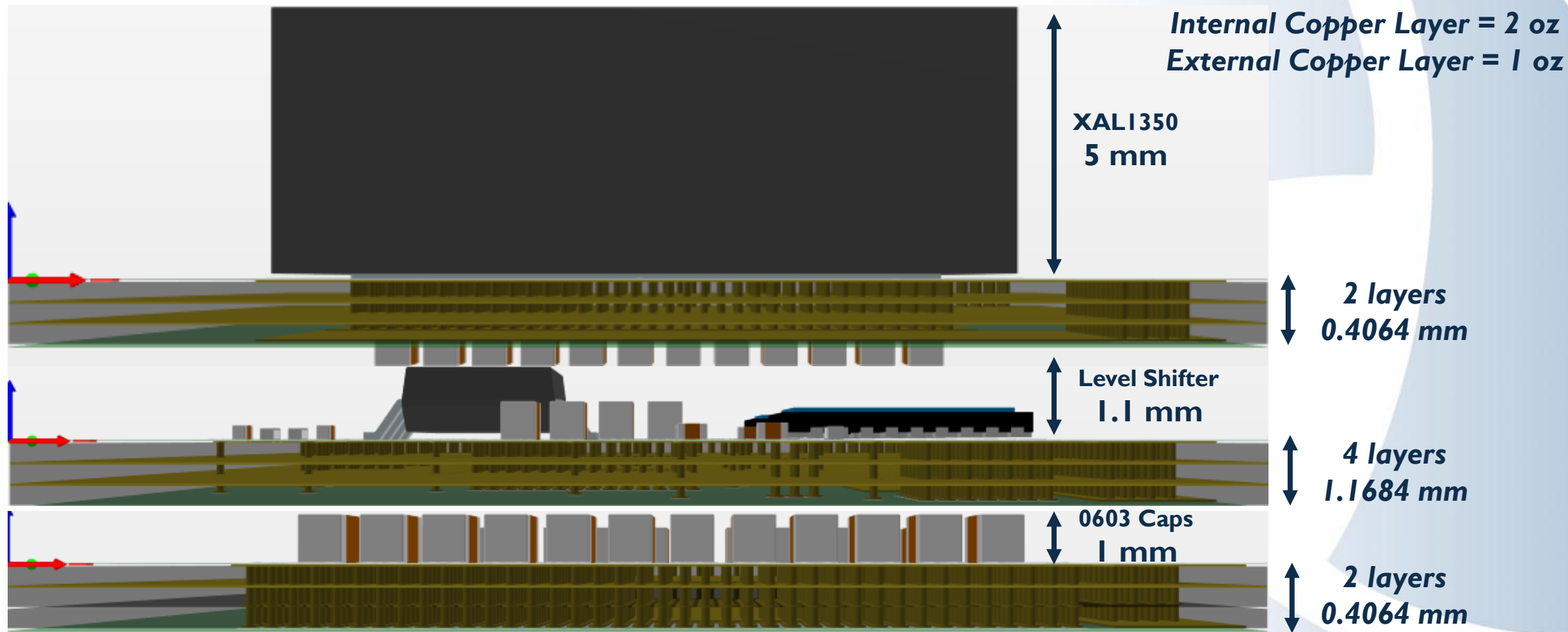




Optimization of Surface Area



Optimization of Thickness



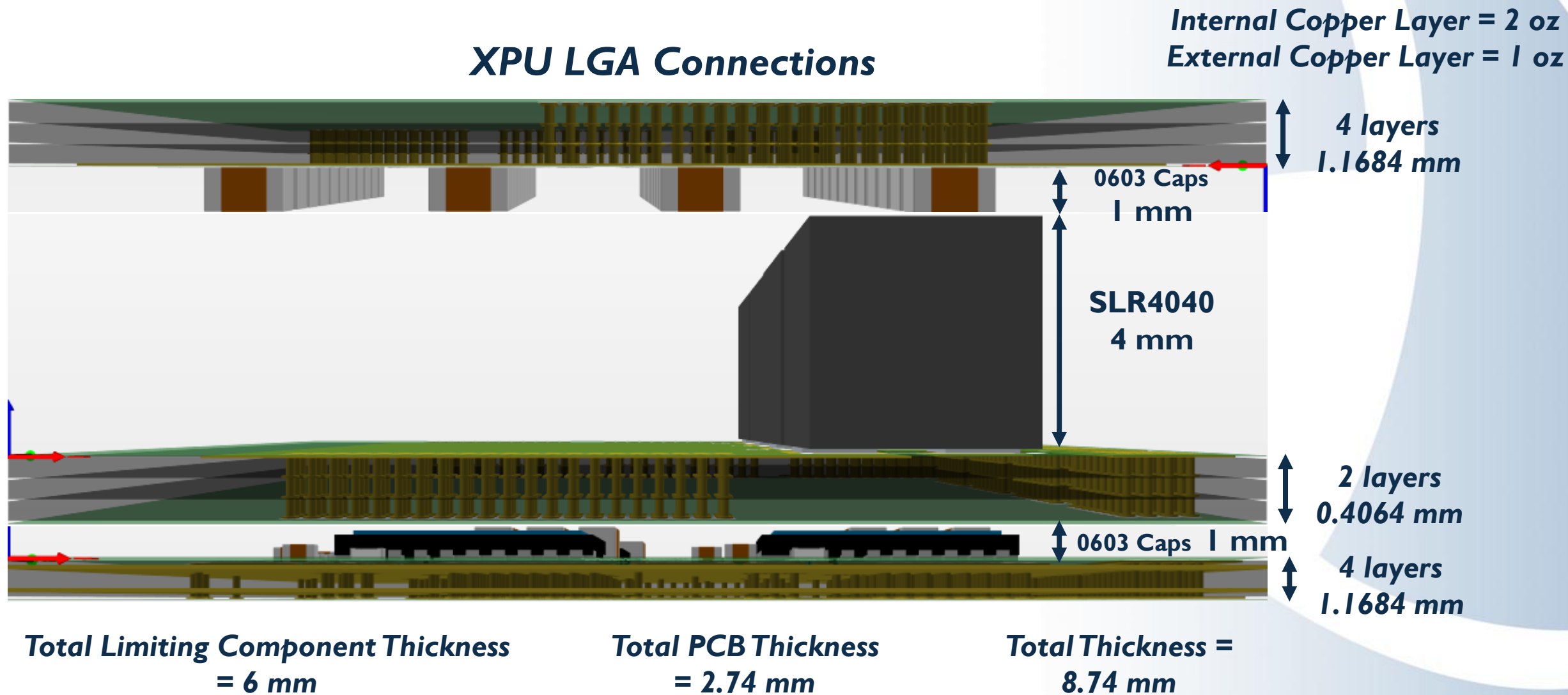
Total Limiting Component Thickness
= 7.1 mm

Total PCB Thickness
= 1.98 mm

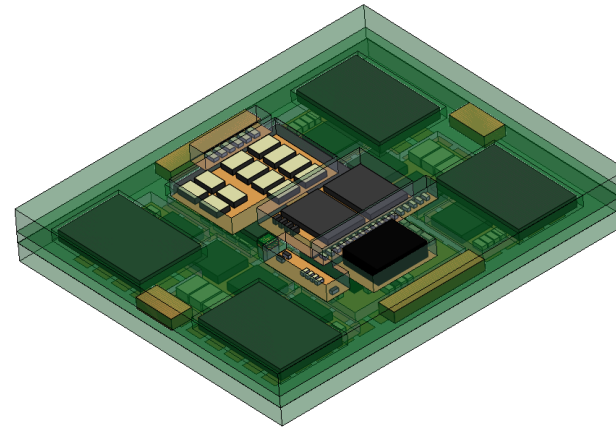
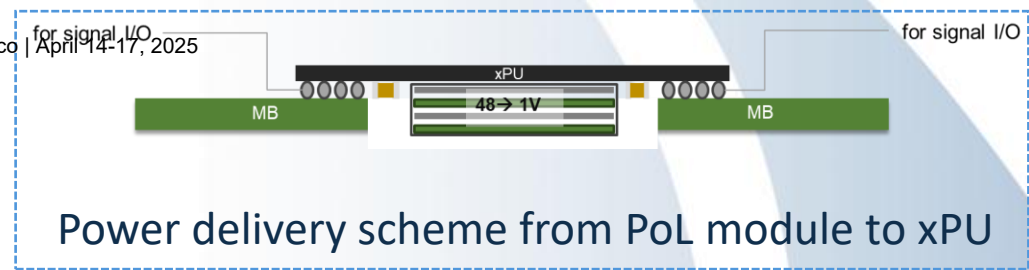
Total Thickness
= 9.08 mm

Optimization of Thickness

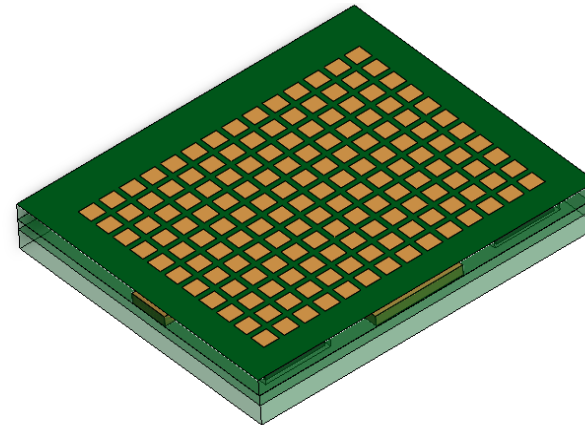
XPU LGA Connections



Packaging Integration Updates



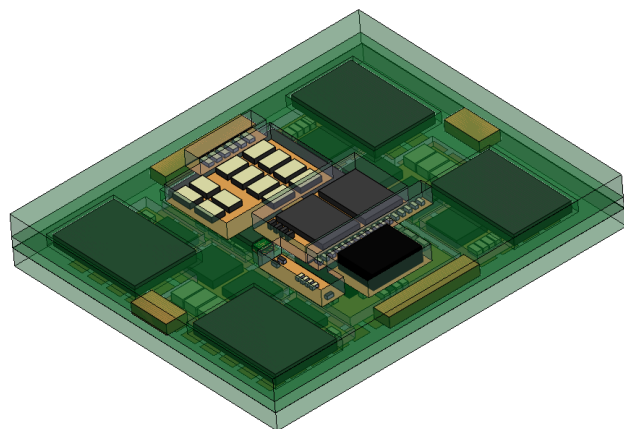
Top View



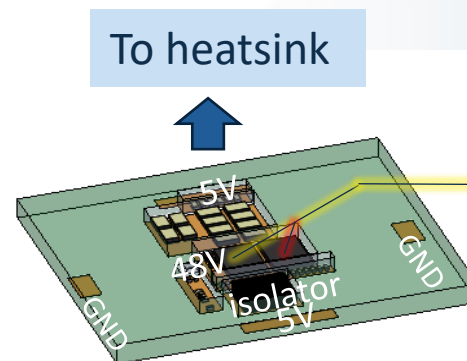
Bottom View
(LGA package)

- Vertical power delivery
- 3D fully embedded LGA package
- Self-designed planar inductors

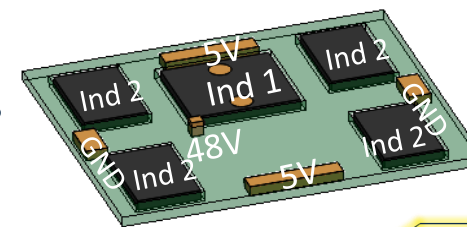
Packaging Integration Updates- cont'd



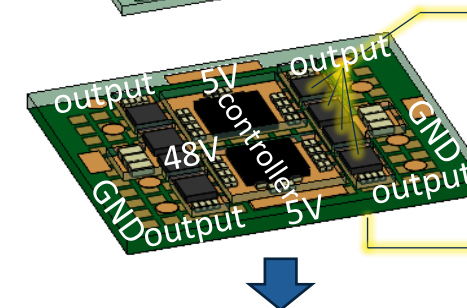
**1st Stage
(48-5V)**



**Inductor substrate
for both stages**



**2nd Stage
(5-1V)**



LGA side to xPU

Exploded View

Future Work

- **Issues currently being addressed**

- Manufacturing a fully embedded PCB.
- Thermal optimization of the current layout at higher loads.
 - Better material for the PCB: Metal Core, Ceramic, etc.

- **Final Objective**

- The active power socket implementation fully combines the rest of the motherboard and the power module into one PCB.

Thank You!