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AFRL

Survivability of AlGa_N/Ga_N HEMTs made with WN_x- and Pt-based Gate Metal Stacks above 500 °C

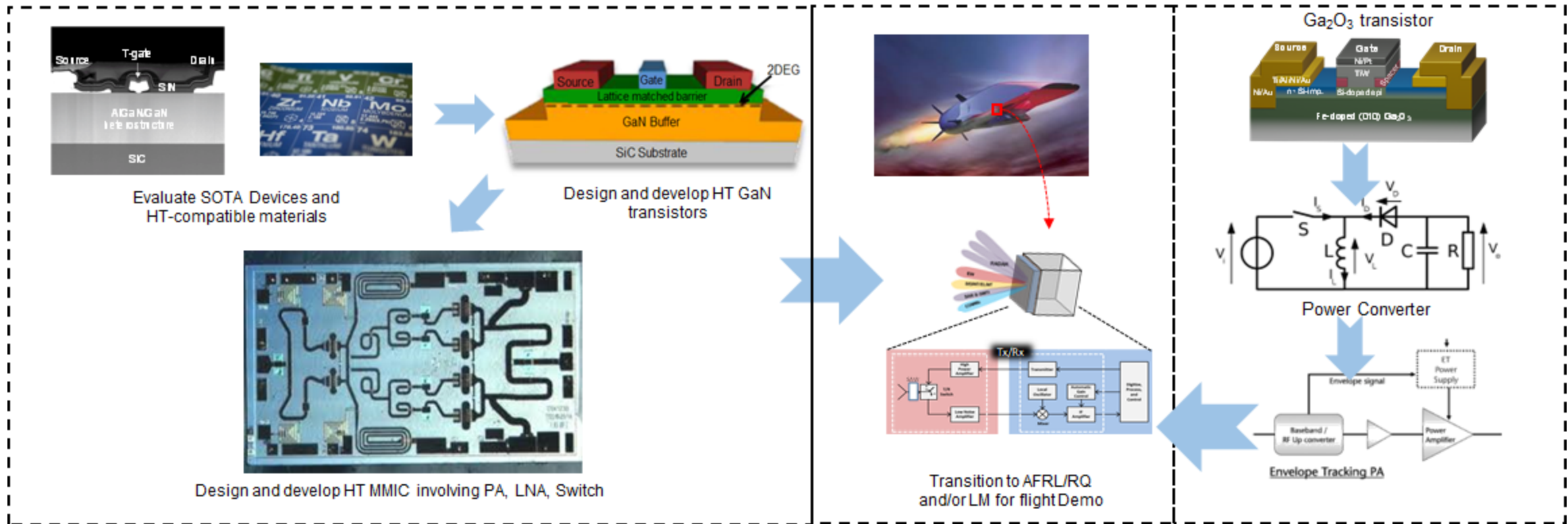
Nicholas P. Sepelak, Micheal J. Harrington, Weisong Wang, Akilesh Srikanth, Timothy Prusnick, Stefan Nikodemski, Kevin Leedy, Biddut Sarkar, Kyle J. Liddy, Branen Bussey, Ahsan Mian, Andrew J. Green, and
Ahmad E. Islam,



Contents

- High-temperature scope of work at AFRL Sensors Directorate
 - Measurement challenges
 - Testing capabilities up to 500 °C and beyond
- Motivation of work
 - Revelations from previous high-temperature studies (GaN and Ga₂O₃)
 - Diffusion barrier down selection
- High-temperature DC test of WN_x/Pt/Au gated HEMT
 - Device Fabrication
 - High-temperature DC results
 - Pre/Post device metrics

Thermally Hardened Electronics for RF and Power: Overview

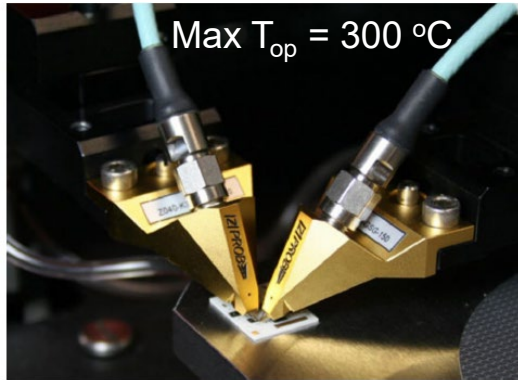


- ❑ Improve device performance/stability at $> 300\text{ }^{\circ}\text{C}$
 - Design and develop HT GaN MMIC
 - Design and develop $\beta\text{-Ga}_2\text{O}_3$ transistor and power converter

- ❑ Device/Circuit research internally funded till FY28
- ❑ Exploring external opportunities for system level demonstrations

HT RF measurement challenges

Device testing



Source: FormFactor.com

Max T_{op} = 500 °C



AFRL/MicroXact/NASA

Max T_{op} = 125 °C



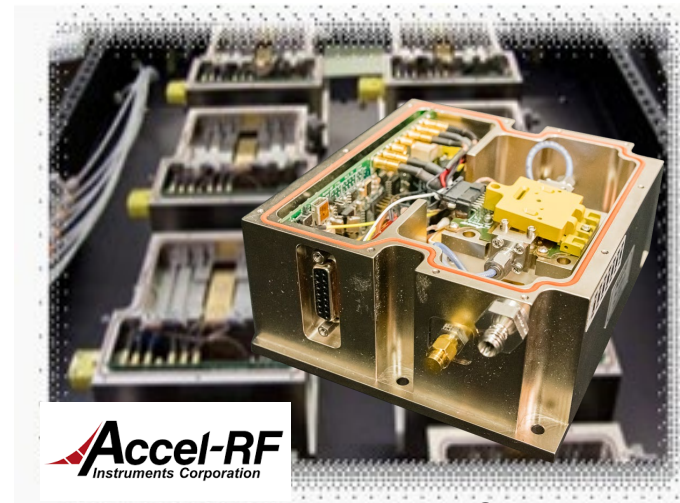
Max T_{op} = 300 °C (connector)
= 1000 °C (cable)



MMIC testing

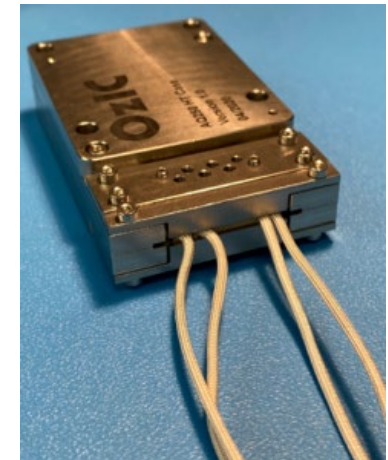


Max T_{op} = 125 °C



Max T_{op} = 300 °C

Furnace testing



DC-1MHz

Upto 500 °C DC/RF testing capabilities

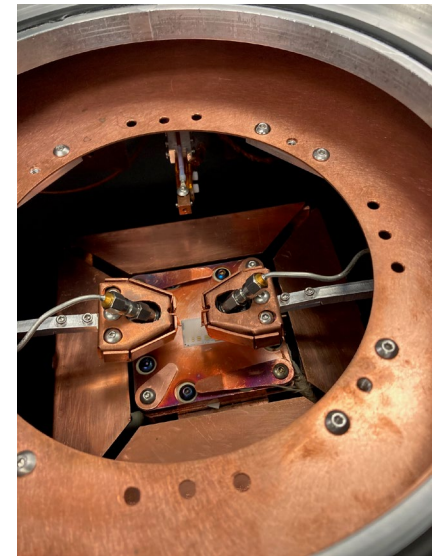
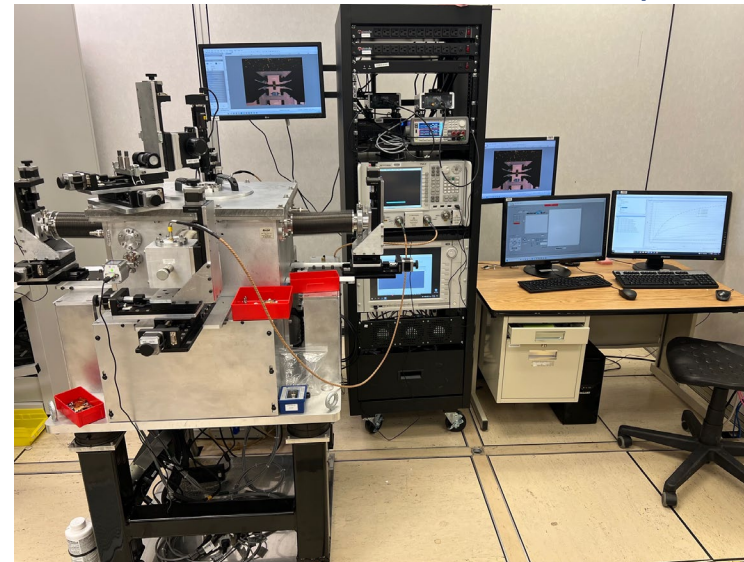
❑ COSMOS Probe station

- 4" semi-automated
- DC & RF (0.5-40/50GHz)
- Up to 300 °C
- Pulse IV tests for AC-DC dispersion studies



❑ MicroXact Probe Station

- 2" semi-automated
- DC (650 °C), RF (500 °C, 10 MHz - 40 GHz)
- Vacuum (~1 mTorr); in future, N₂/Ar ambient
- Has Pulse IV capability
- Introduce surface temp measurement: kSA-BandIT



1000+ °C testing capabilities

❑ Nextron Micro Probe Raman DC System

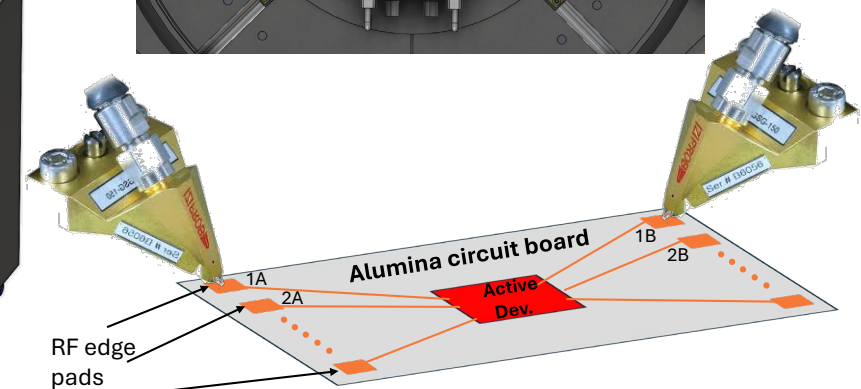
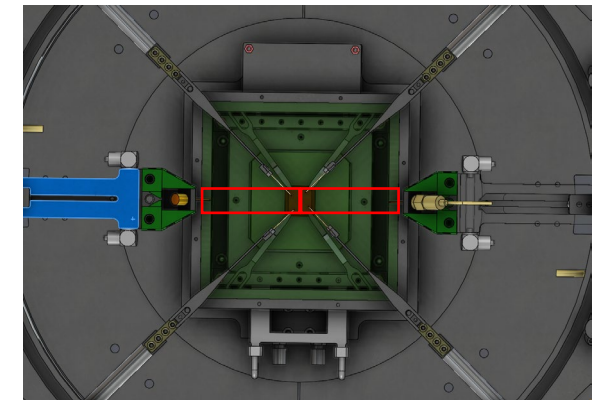
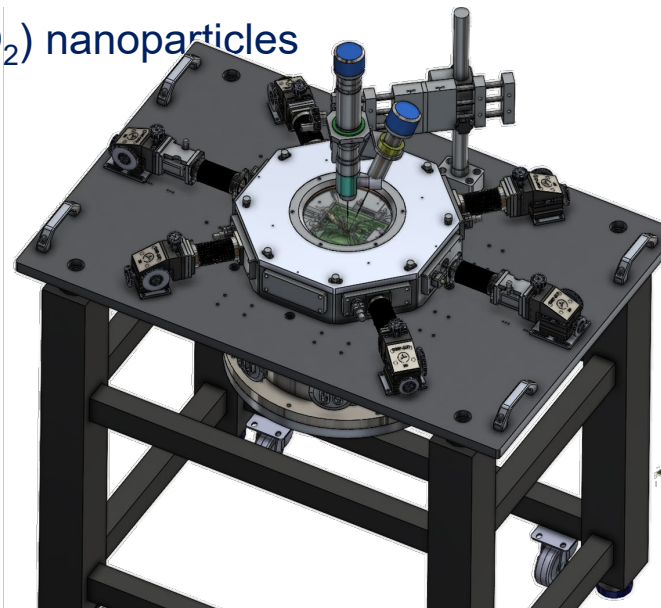
- DC (1000 °C); 5 mm x 5mm
- Vacuum, Ar/N₂, variable pres. (up to atm)
 - Air: oxidation of Rh probes at T > 800 °C
- Surface temp measurement: Raman
 - Higher spatial resolution using (TiO₂) nanoparticles

Renishaw Raman System: Raman, PL

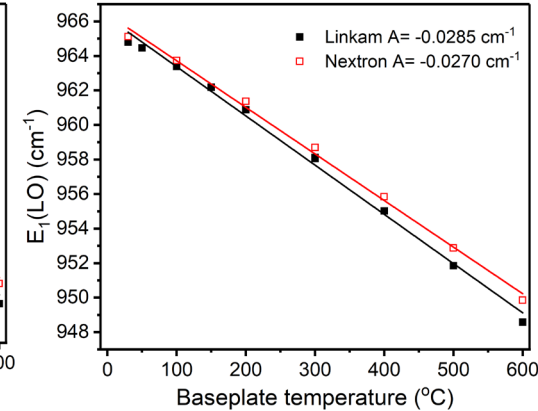
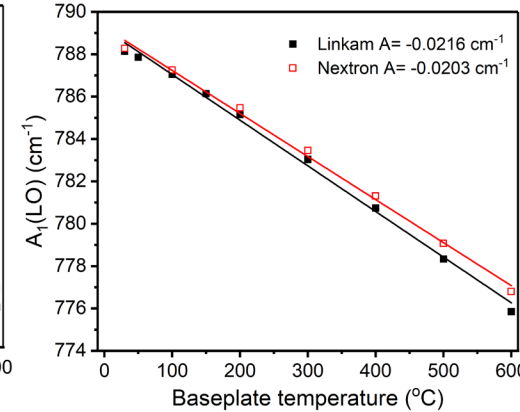
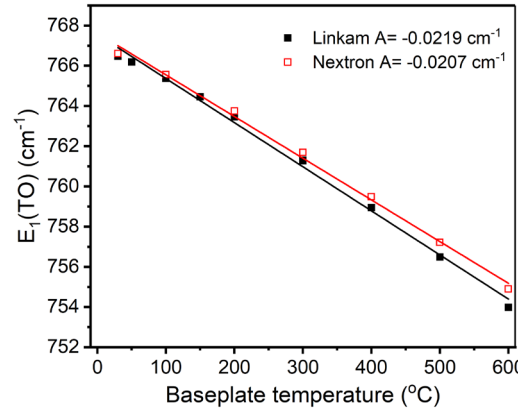
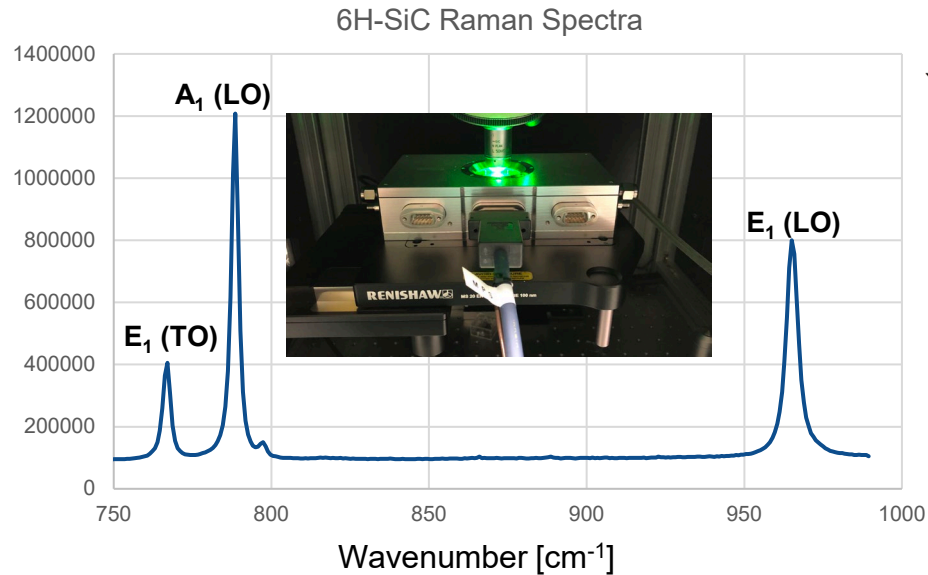


❑ INSTEC HP1000V-MP DC/RF System

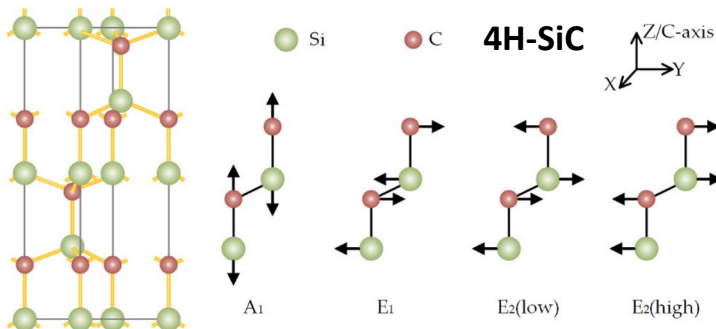
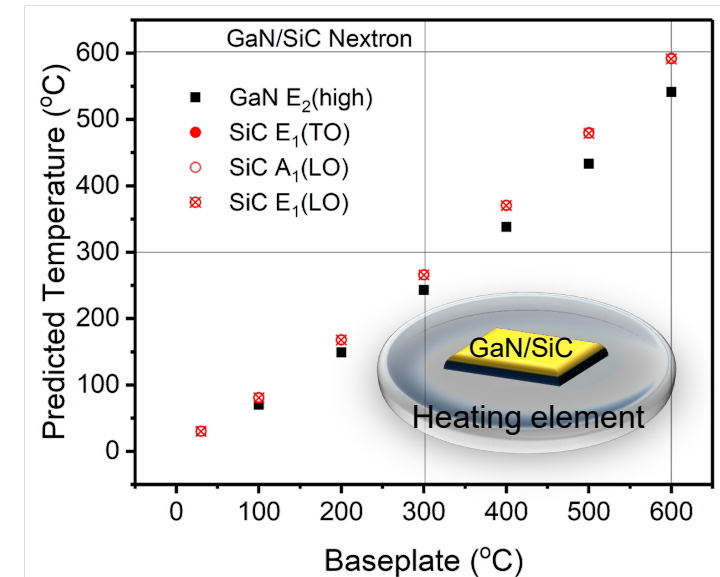
- 2" semi-automated
- DC (1000 °C), RF (≥ 800 °C, 9 kHz - 40GHz)
- Vacuum, Ar/N₂/Air, variable pres. (up to atm)
- Surface temp. measurement: kSA BandIT



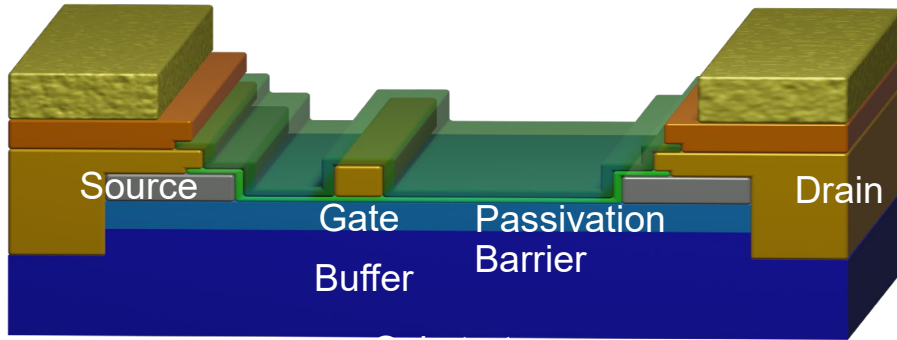
Surface temperature measurement: Raman spectroscopy



- Generate calibration plots for SiC and GaN using thermally equilibrated bulk samples
- Used calibration plots to estimate surface temperature
- Effect of change in strain with Temp. ignored; $\omega = \omega_0 + A \cdot T + B \cdot \epsilon$
- Need better estimation for $T > 500 \text{ }^{\circ}\text{C}$

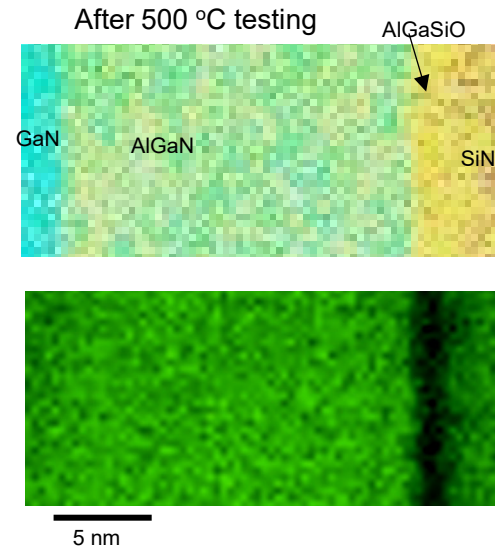


Device-level challenges



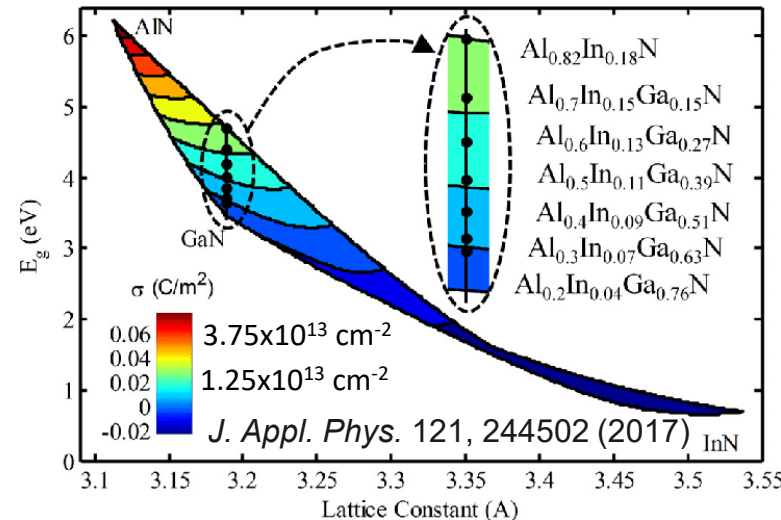
Gate leakage:

- Gate: Ni/Au $\rightarrow$ Ni/X/Au, Y/Au, Y/X/Au
 - X: Pt; Y: Pt, Pd, Ir, WN, TaSi₂, TaSiN
- Gate oxide: Al₂O₃ (600°C), SiO₂ (>1000°C)



Passivation Leakage:

- Current passivation scheme is designed for low dispersion at high frequency
- A new passivation may be needed for HT RF



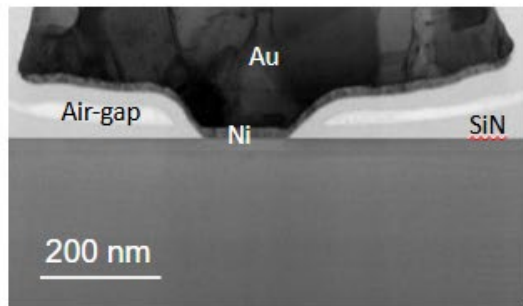
Buffer leakage:

- Reduced dislocation
- Lattice-matched barrier with GaN
 - AlScN with 12-14% Sc (Cornell)
 - InAlN with ~18% In (E. Kohn, 2006-2012; Jessen et al., EDL 2007)

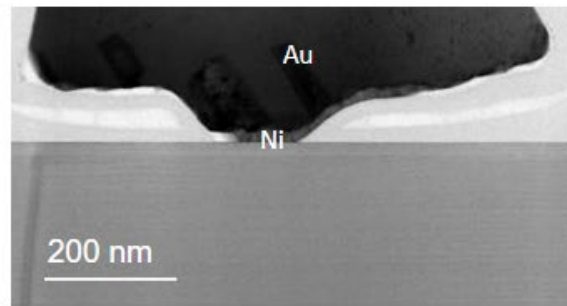
Nickel Bad?

- On GaN HEMTs tested at HT, the Ni layer diffused with the Au, reducing the barrier height and has effectively become absent from the GaN/gate metal interface.
- On Ga₂O₃ devices test at HT, the Ni layer diffused with the Au and intermixed with the Al₂O₃ dielectric and passivation layer

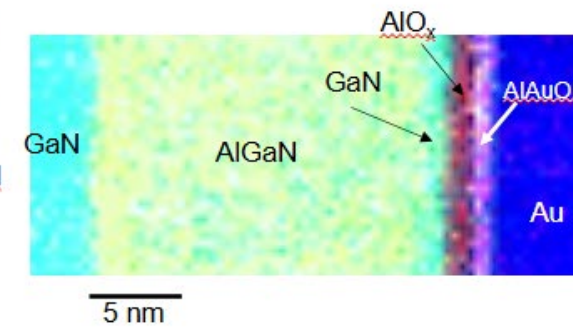
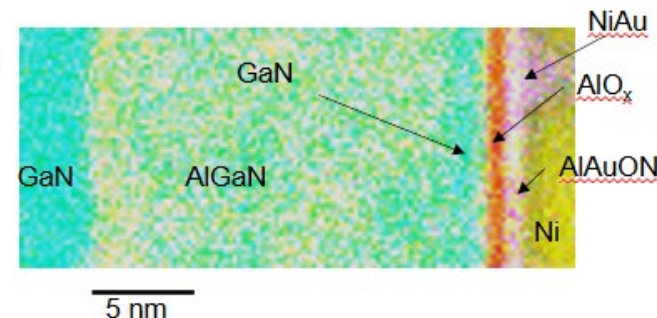
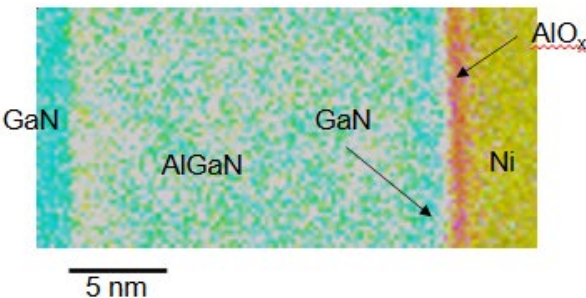
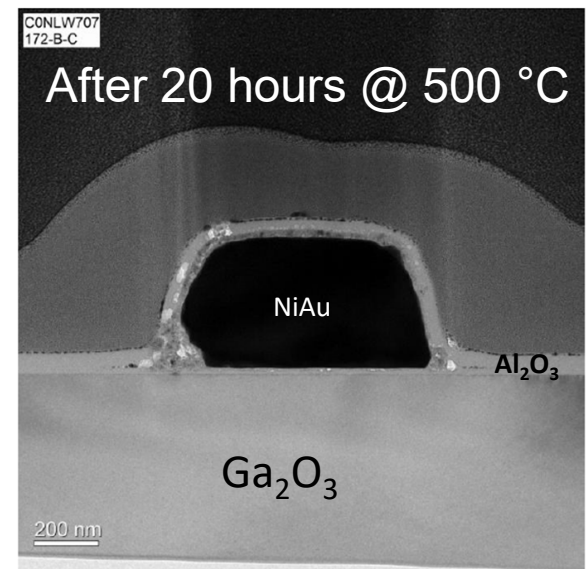
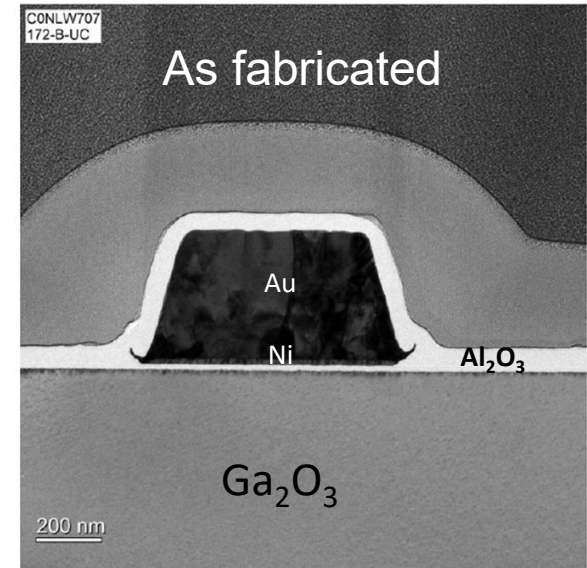
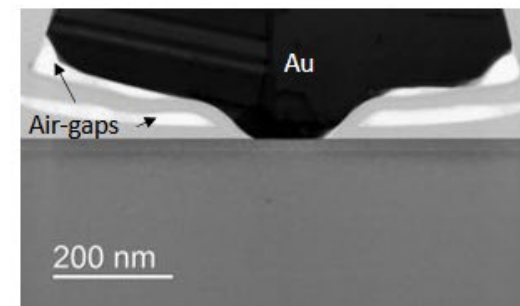
As Fabricated



After 400 °C

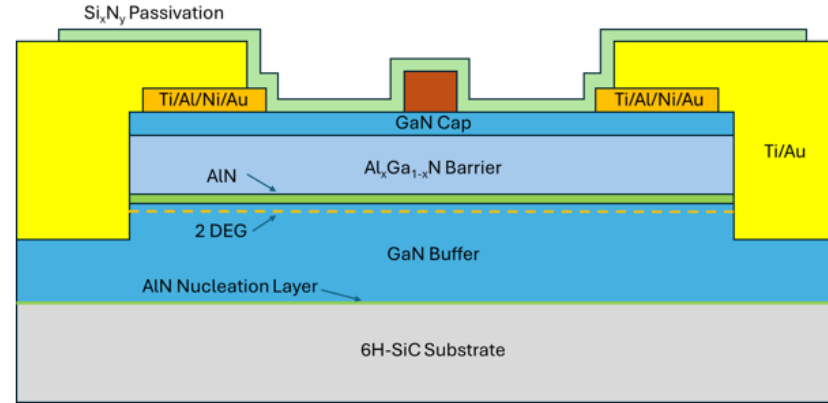


After 500 °C



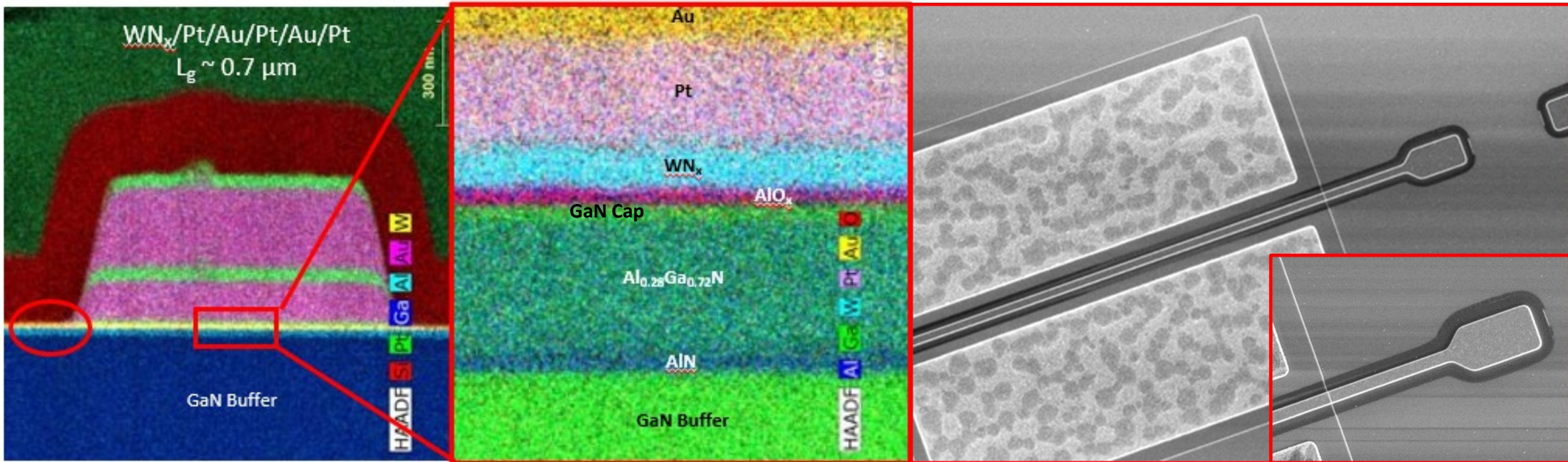
Device Fabrication

1. Define ohmic and evaporate Ti/Al/Ni/Au
2. Anneal at 870 °C for 30 sec
3. Define mesa and ICP etch back to isolate
4. Define gate metal, then sputter WN_x followed by Pt/Au/Pt/Au/Pt evaporation
5. Define test pad metal and evaporate Ti/Au
6. PECVD blanket deposition of Si_xN_y passivation flowed by an RIE etch to open up the probe pads.



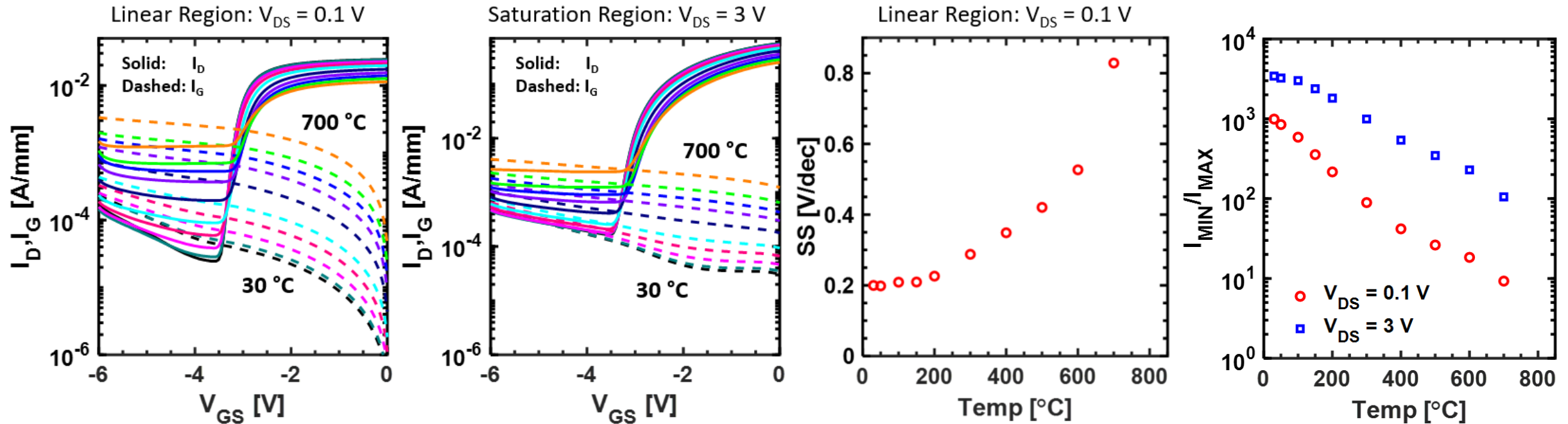
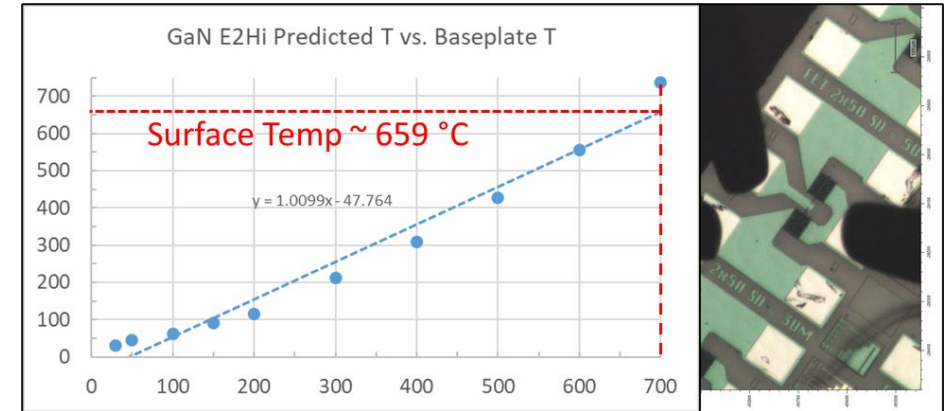
Post Processing Notes

- The sputtered WN_x undercut the photoresist, unexpectedly increasing the gate length, L_g
- A layer of $AlO_x \sim 1$ nm has formed at the surface of the GaN Cap. It is believed that this layer forms during the annealing process. We are investigating processes to remove this layer.



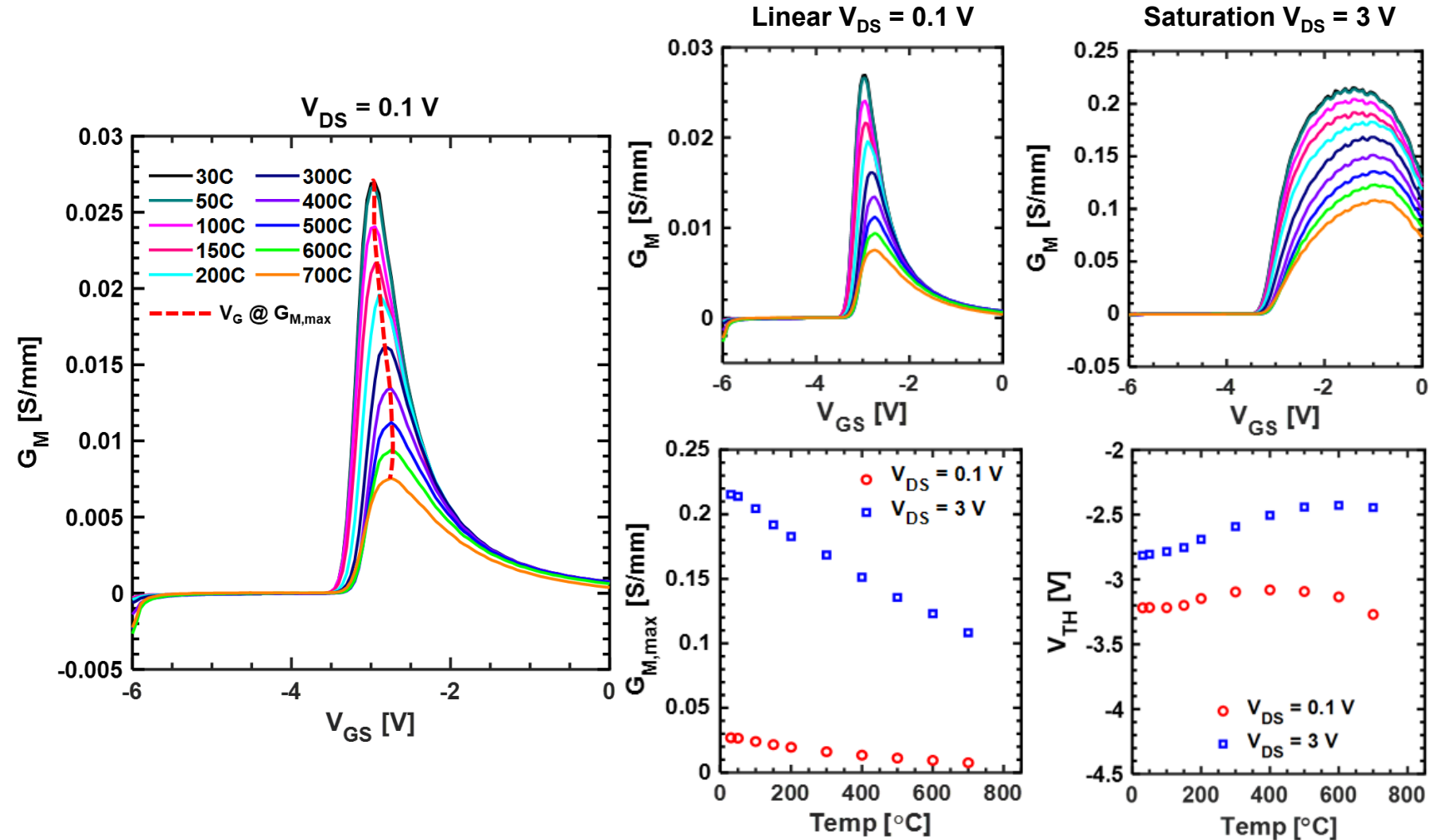
High-Temperature DC Test - Transconductance

- For I_D - V_G , DUT was biased at $V_{DS} = 0.1$ and 3 V with V_G swept from -6 V to 0 V.
- DC bias at temperature increments of 50° from 30 °C to 200 °C and 100° from 200 °C to 700 °C
- Saturation I_{max} : at 30 °C = 565 mA/mm, at 700 °C = 252 mA/mm, 44.6 % reduction in I_{max}



High-Temperature DC Test - G_M and V_{TH}

- The decrease in $G_{M,max}$ as a function of temperature appears to have a linear trend
- The positive shift in threshold voltage was counterintuitive
- The parametric analysis code estimates V_{TH} by indexing the $V_G @ G_{M,max} \pm 3$ points and applying a linear regression to $I_D @$ the indexed V_G

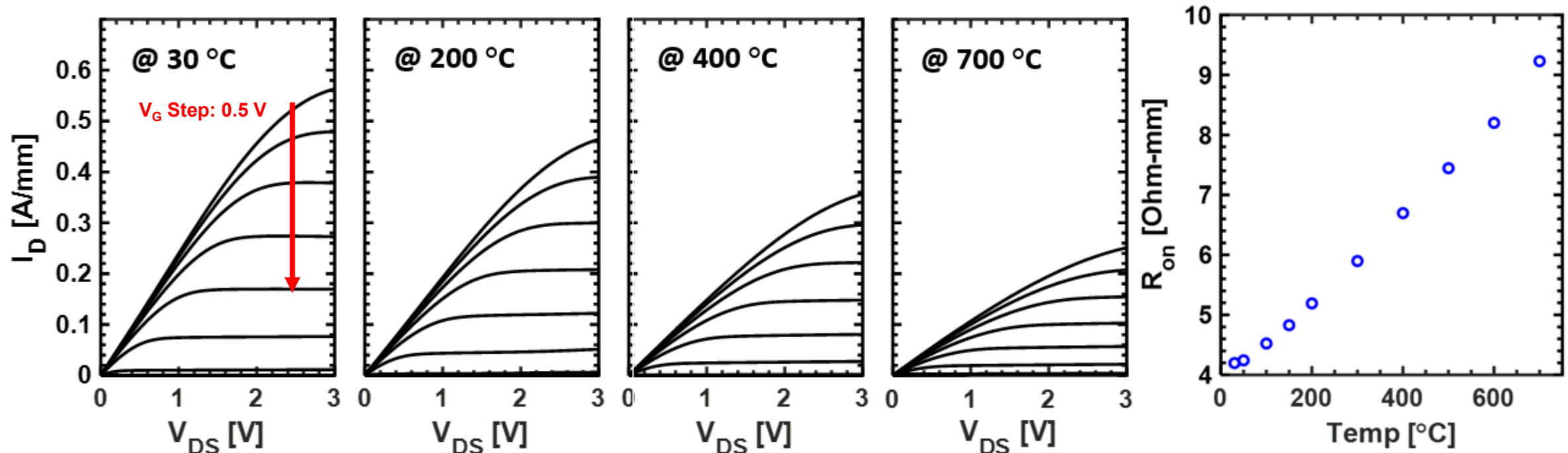


High-Temperature DC Test – I_D - V_D Family and R_{on}

- For I_D - V_D , the drain voltage, V_{DS} was biased from 0 V to 3 V with gate voltage, V_G steps of 0.5 V from 0 V to -6V
- R_{on} is estimated with the inverse of the slope obtain by linear regression of the first 20 point in the I_D @ $V_G = 0$ V sweep normalized to gate width, W_G

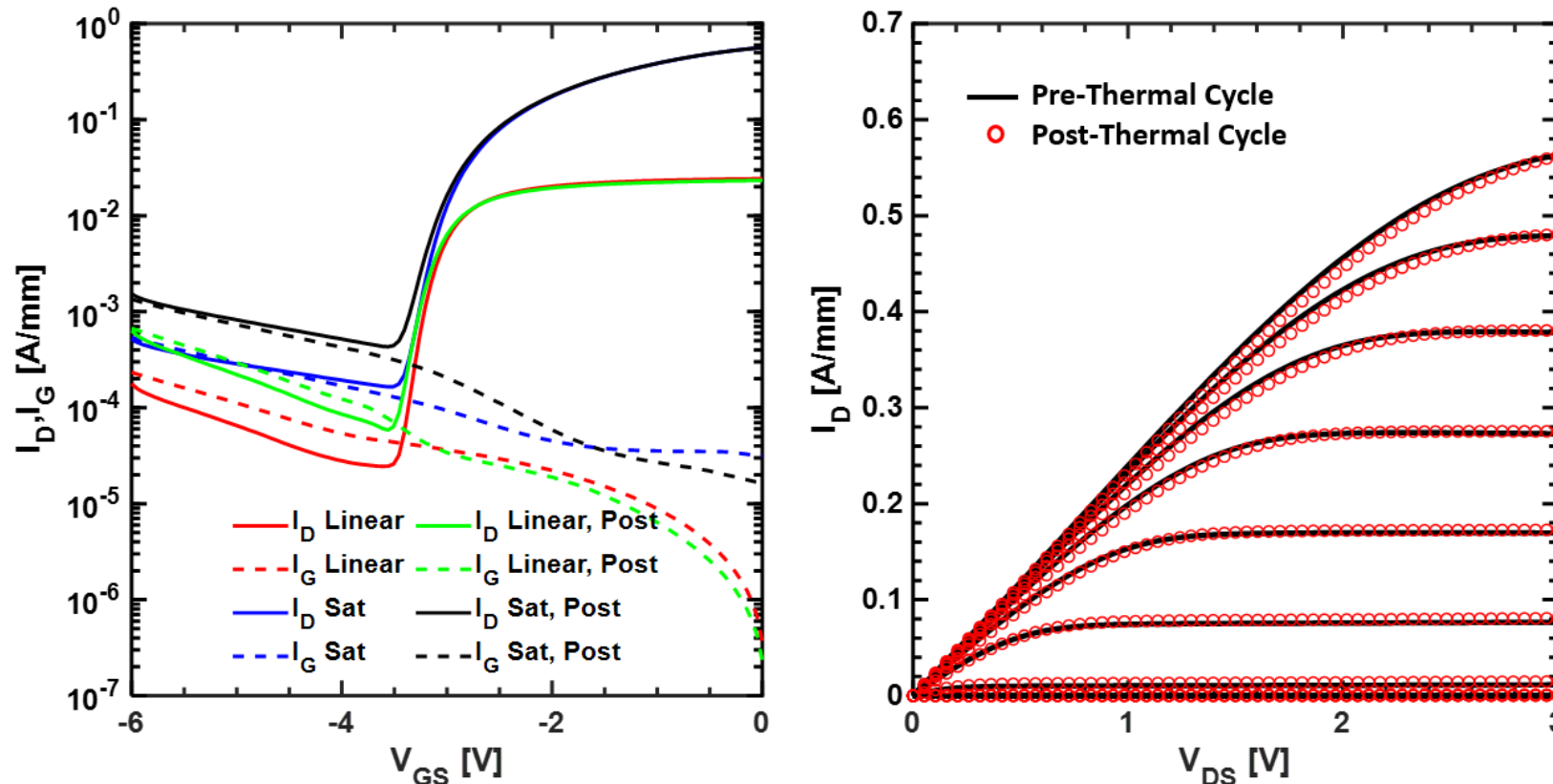
$$I_D = \beta_0 + \beta_1 V_D + \varepsilon$$

$$R_{on} = \left(1/\beta_1\right) W_G$$



High-Temperature DC Test – Pre/Post DC Comparison

- Pre/post I_D - V_G shows increased leakage in the off-state but decrease leakage in the on-state
- Pre/post I_D - V_D shows a recovered saturation current with increased on resistance





Summary

- WNx/Pt/Au gate metal stack on AlGaIn/GaN HEMT show promise for high-temperature operation.
- For RF capabilities, the gate metal stack must be compatible with E-beam lithography for scaled gate lengths, 140 nm and less.
- Investigations into other gate metal combinations in progress.
- A new passivation recipe may be necessary for longer term operation at high temperatures.



Thank you for your attention Question?

WN_x Film

- Sputtered films with different Ar/N₂ ratio at either 2 mTorr or 4 mTorr and 250 W power

WN_x Sheet Resistance

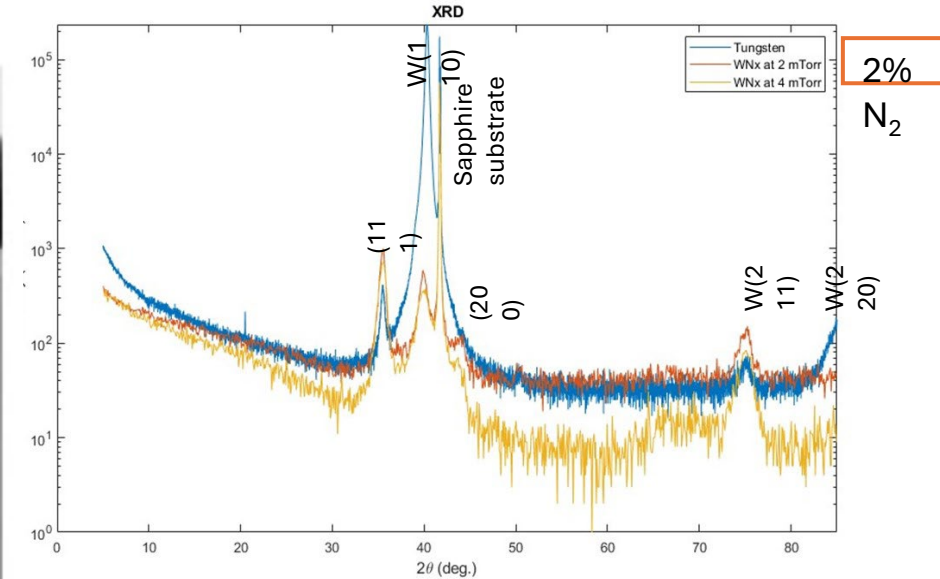
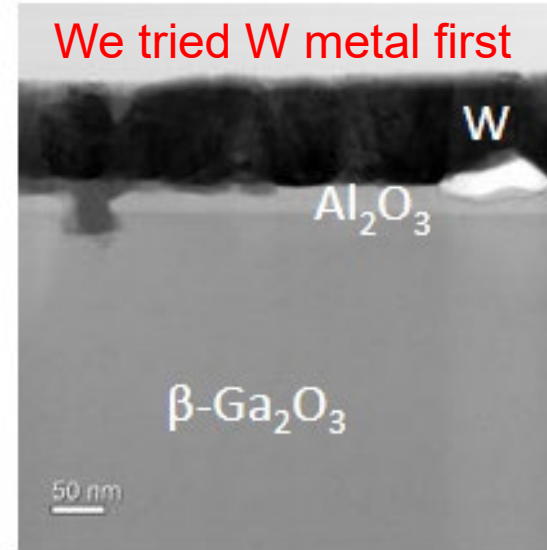
	2 mTorr	4 mTorr
0% N ₂	-	11.21 Ω/□
1% N ₂	23.35 Ω/□	39.07 Ω/□
2% N ₂	23.07 Ω/□	32.99 Ω/□

4000 Å film

1000 Å film

1500 Å film

We tried W metal first



p-Si MOSCAP

