High Operational Temperature Sensors (HOTS)

KK Law, MTO
Todd Bauer, MTO



High performance analog sensor microelectronics technology that operates at extreme high temperature

IMAPS APPE/CICMT/HiTEC Conference
April 15, 2025

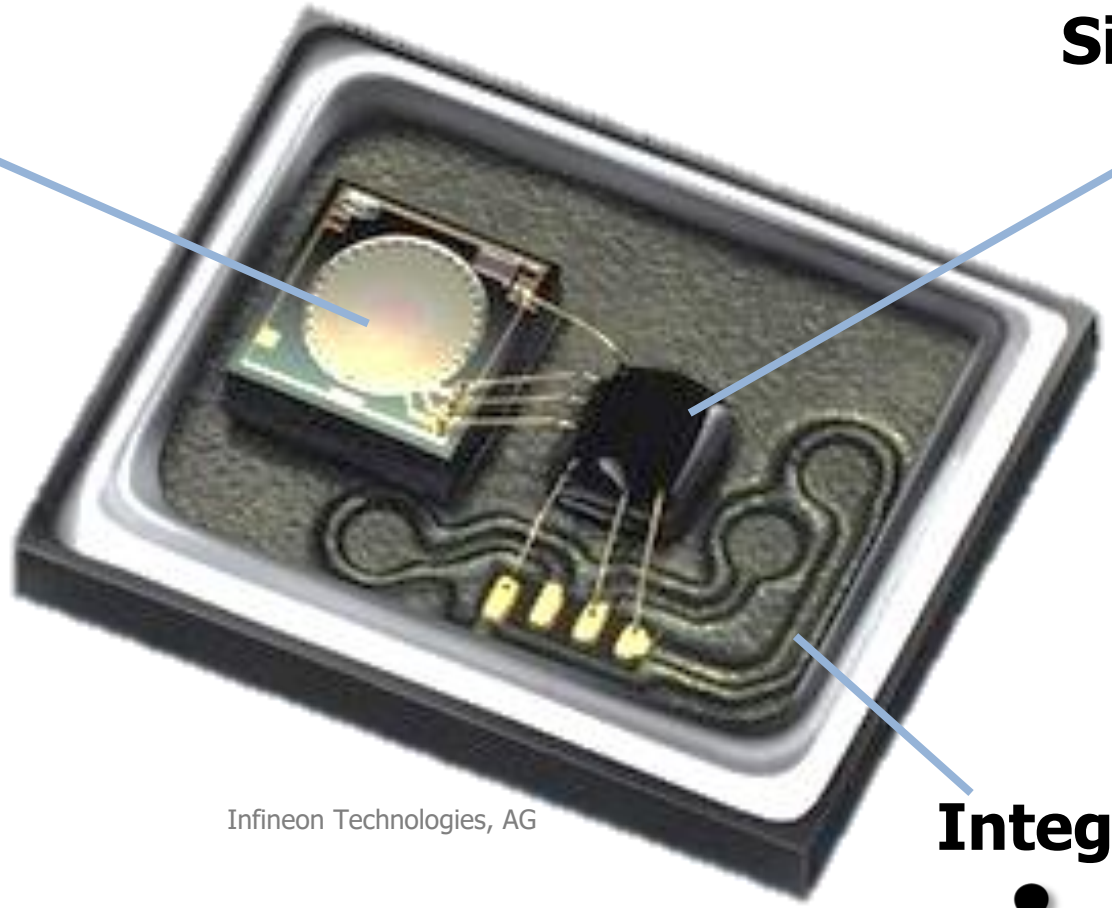
DARPA

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What is a sensor?

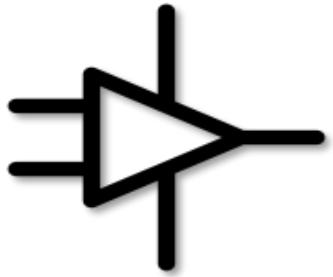
Transducer



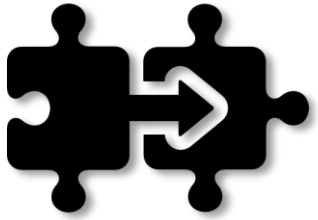


Infineon Technologies, AG

Signal-conditioning microelectronics



Integration



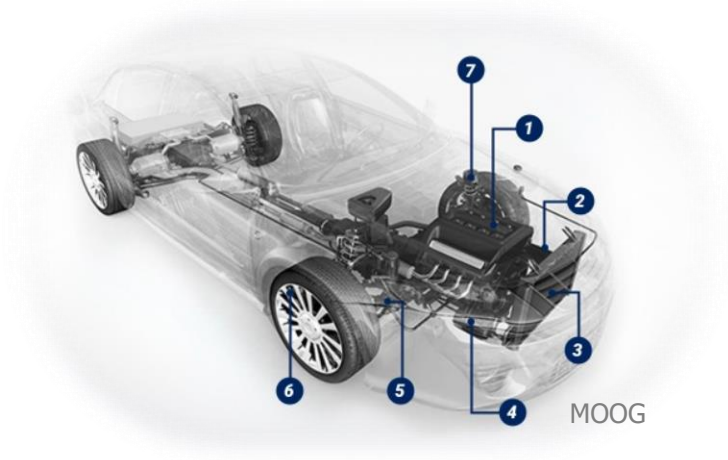
High operating temperature sensor applications

Oil-and-gas



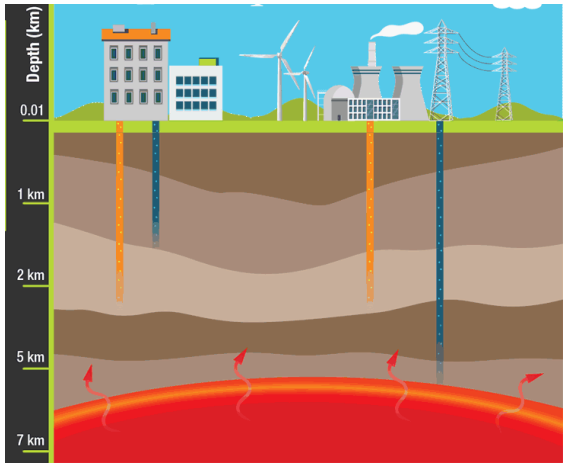
Hexagon

Automotive



MOOG

Geothermal

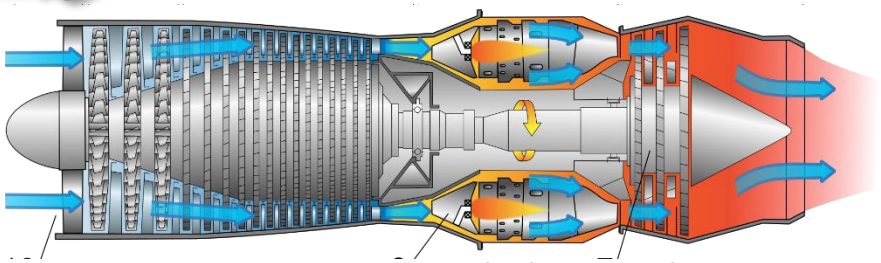


Brookhaven National Laboratories

Turbine engines

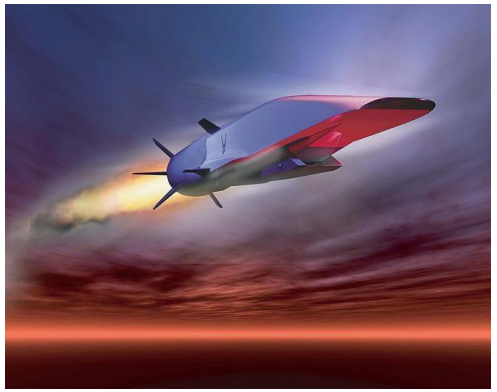


F-35



Federal Aviation Administration

Hypersonic systems



X-51



HTV-2

ELECTRONICS RESURGENCE INITIATIVE 2.0

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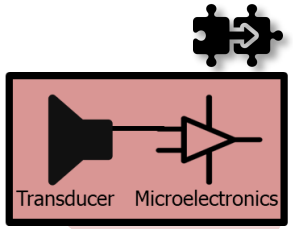
Program goal

High performance analog sensor microelectronics technology that operates at high temperature

High Performance
Low Temperature
Integrated

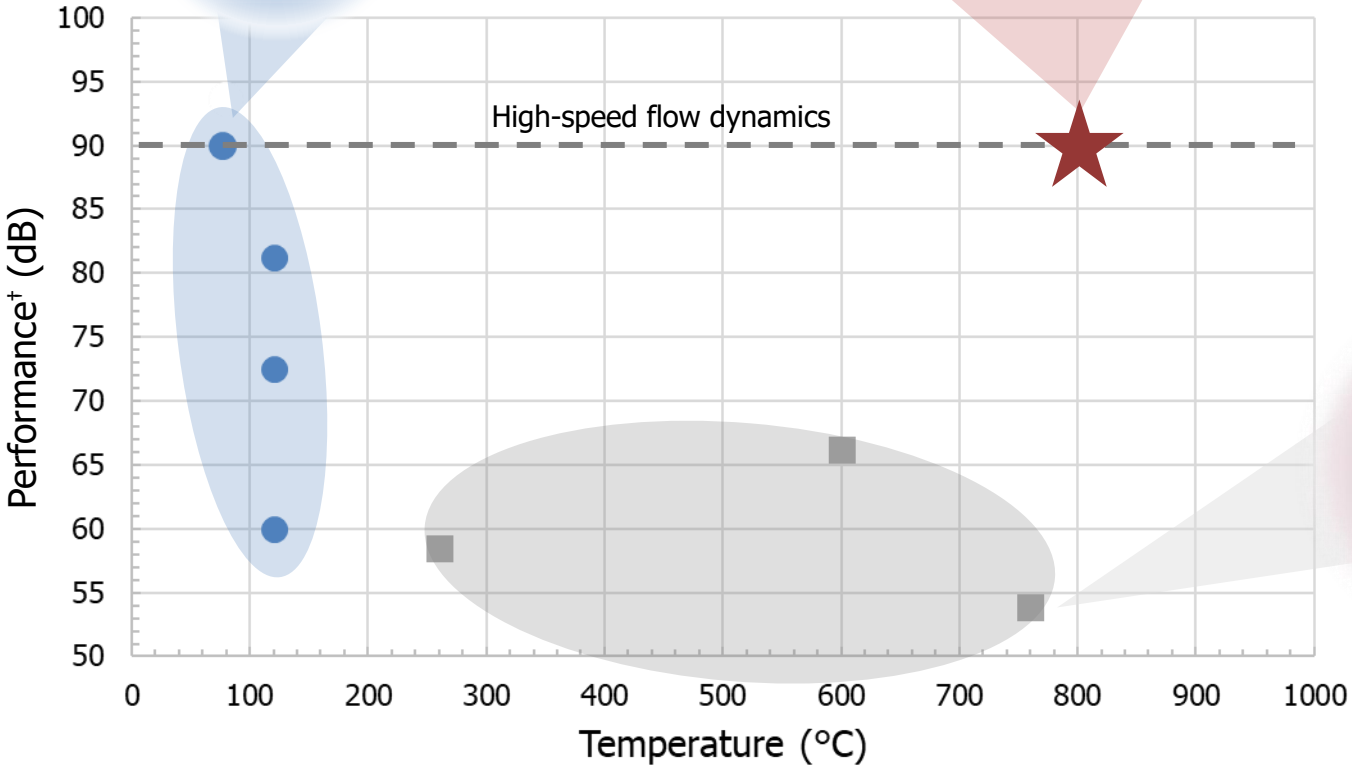
PCB Micro 132B





HOTS

High Performance
High Temperature
Integrated



Program Metrics		
Operating Temperature*	°C	800
Lifetime at Temperature	Hr	> 1
Dynamic Range**	dB	> 90
Bandwidth	MHz	> 1

*without active cooling
**1 Pa/√Hz pressure resolution



PCB Micro 176A



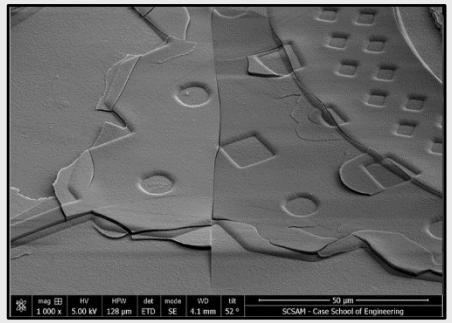
PCB Micro 422M

Low Performance
High Temperature
Disaggregated

†Performance = Dynamic Range · Bandwidth (dB re 1 MHz)

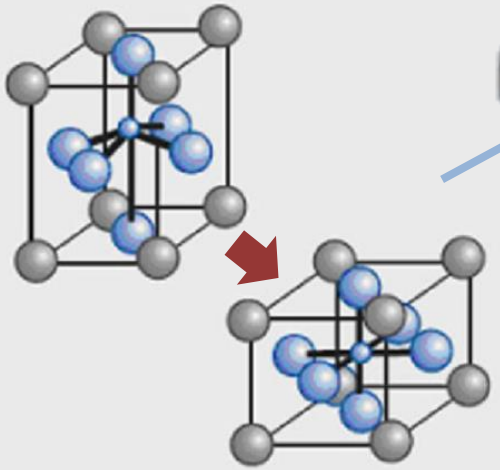
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Failure mechanisms of microelectronics at elevated temperatures

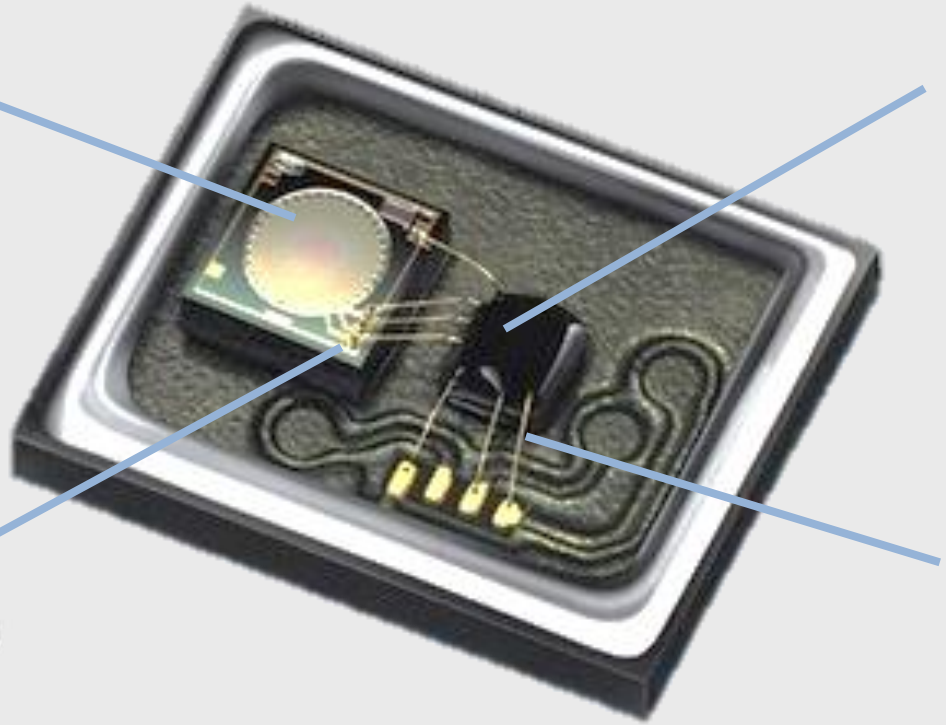


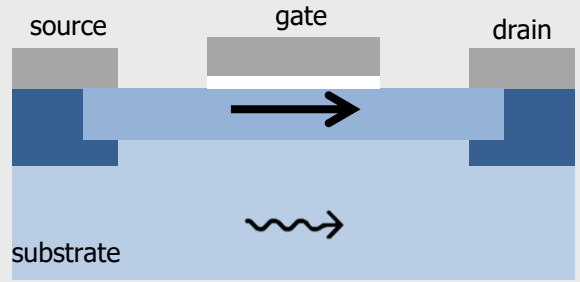
P. G. Neudeck, et al. (2019)

Mechanical cracking

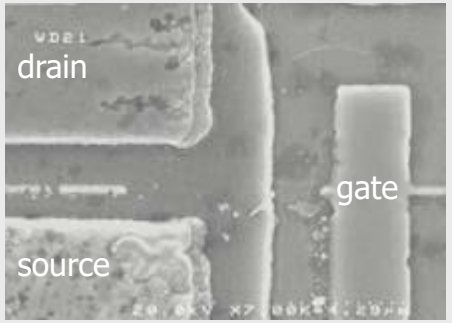


Material degradation





Leakage



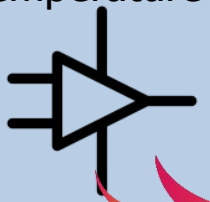
Northrop Grumman (2022)

Electrical breakdown

Technical challenges for high operating temperature sensors

Technical Challenge 1

Achieving both long lifetime and large bandwidth **transistors** at high temperature



Technical Challenge 2

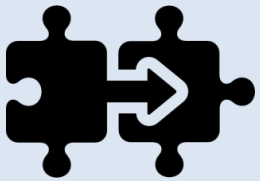
Achieving a high sensitivity **transducer** at high temperature





Technical Challenge 3

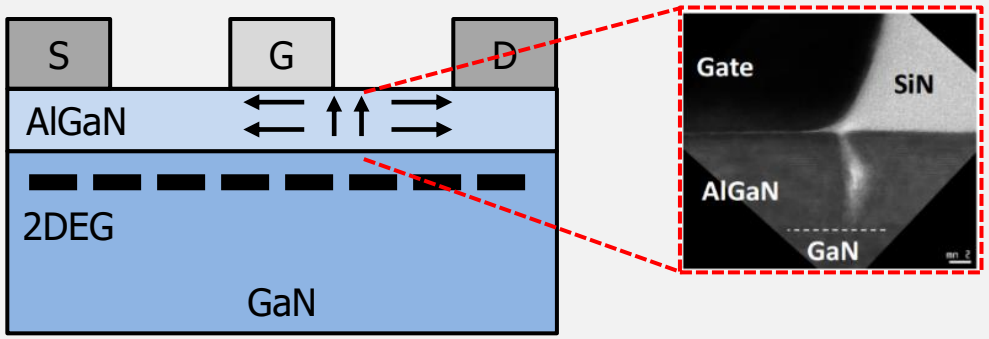
Integrating a high operating temperature sensor without degrading performance



Technical Challenge #1

Achieving both long lifetime and large bandwidth transistors at high temperature

AlGaN/GaN Transistors



C. Zeng, et al. (2015)

Lifetime

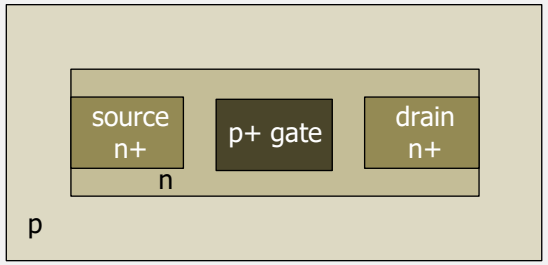
- Lifetime at 800 °C projected to be << 1 second
- Example limitation: stress-induced microcracks

Bandwidth

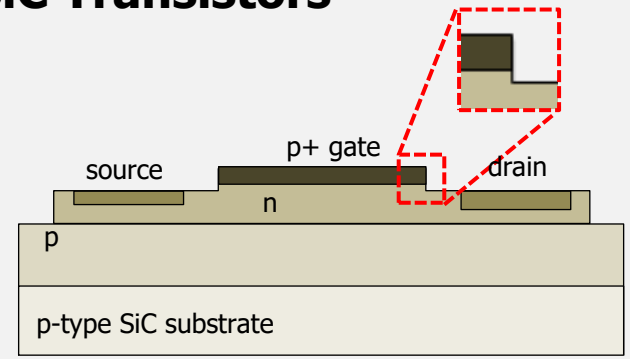
- Large operating frequency

High-Electron-Mobility Transistor (HEMT)

Top-Gated SiC Transistors



Top view



Cross-section

P. G. Neudeck, et al. (2017)

Lifetime

- Demonstrated > 1 hour at 800 °C

Bandwidth

- Limited operating frequency
- Topology limits frequency scaling

Junction Field Effect Transistor (JFET)

HOTS is open to diverse transistor approaches aligned with the program metrics and timeline

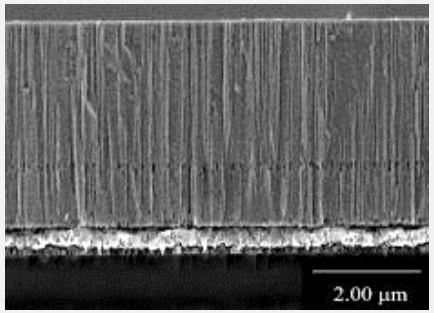
AlGaN = Aluminum Gallium Nitride
2DEG = 2D Electronic Gas
SiN = Silicon Nitride
SiC = Silicon Carbide

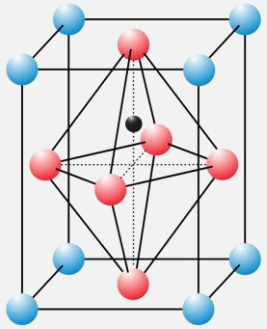
Technical Challenge #2

Achieving a high sensitivity transducer at high temperature

High Sensitivity Transducer

PZT





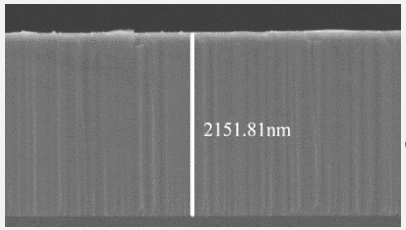
T. P. Comyn, et al. (2021)

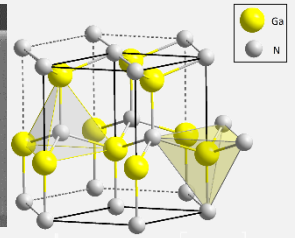
Temperature Limit
- PZT: depolarizes above 250 °C

Sensitivity
- PZT: ~50% energy coupling

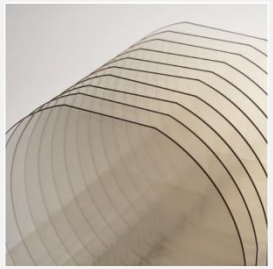
High Temperature Wide-Bandgap Transducer

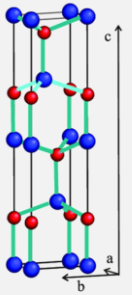
GaN





SiC





M. Rais-Zadeh, et al. (2014)

Temperature Limit
- GaN: > 800 °C
- SiC: > 1200 °C

Sensitivity
- GaN: ~1.5% energy coupling
- SiC: ~0.5% energy coupling

HOTS is open to diverse transducer approaches aligned with the program metrics and timeline

PZT = Lead Zirconate Titanate ($Pb[Zr_xTi_{1-x}]O_3$)

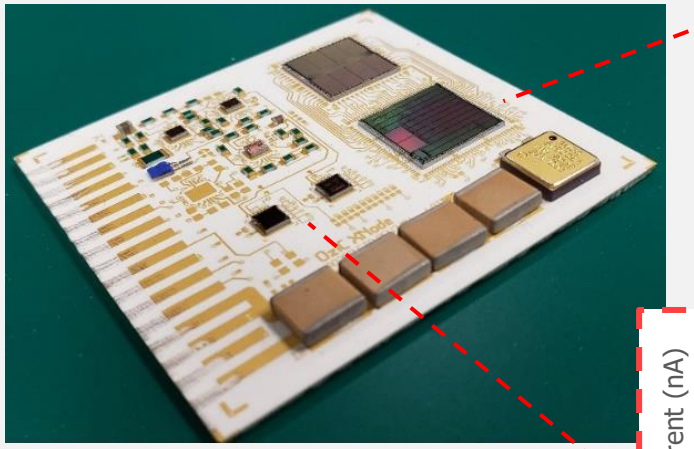
SiC = Silicon Carbide
GaN = Gallium Nitride

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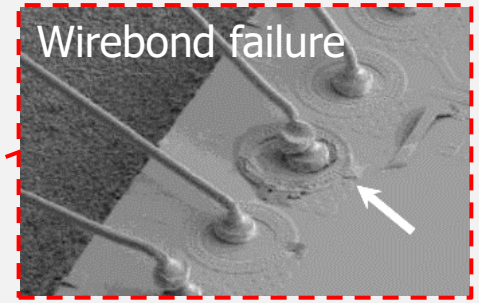
Technical Challenge #3

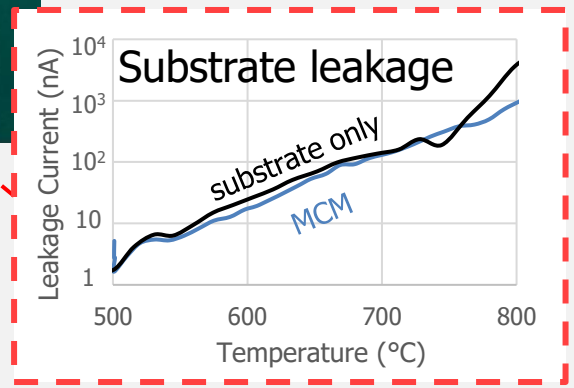
Integrating a high operating temperature sensor without degrading performance

Multi-Chip Module Integration



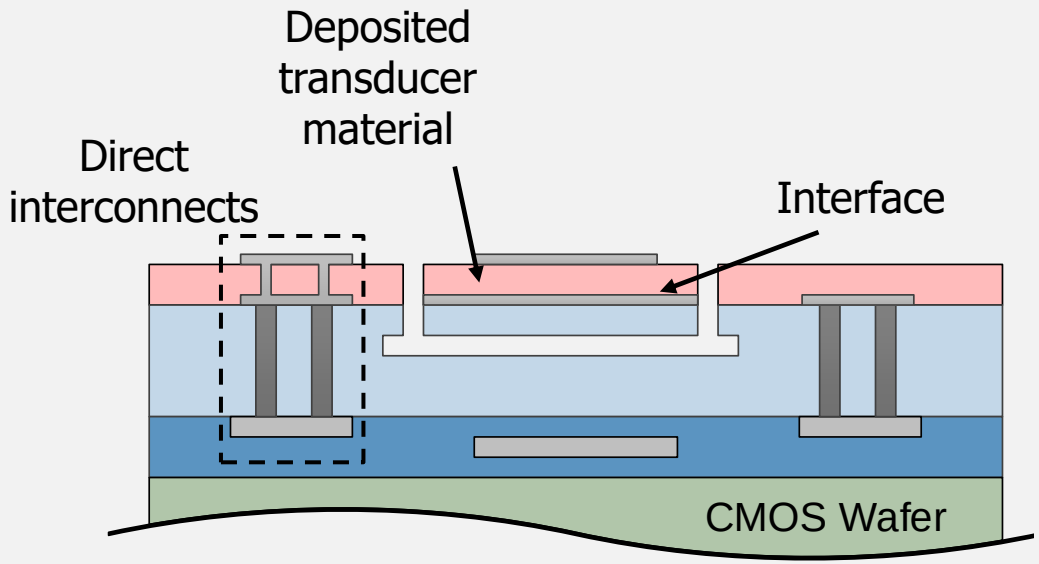
Ozark IC (2020)
P. G. Neudeck, et al. (2017)





Temperature Performance
- Wirebond failure between discrete components

Conventional Heterogeneous Integration



G. Esteves, et al. (2019)

Temperature Performance
- Material interfaces limit operating temperature

HOTS is open to diverse intimate integration approaches aligned with the program metrics and timeline

CMOS = Complementary Metal-Oxide Semiconductor
MCM = Multi-Chip Module

Program Structure

Program structure

FY24	FY25	FY26	FY27	FY28

Phase 1 (18 months) | Go / No-Go | **Phase 2 (18 months)** | **Phase 3 potential expansion**

◆ Design review ◆ Fabrication complete



Discrete transducers and transistors (TC1, TC2)



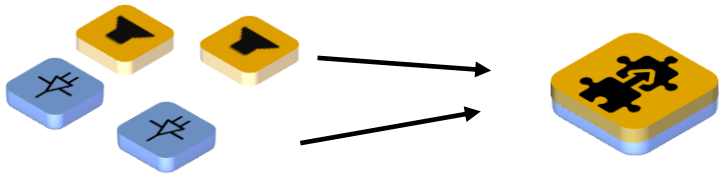
Integrated sensor platform (TC3)



Sensor demonstrators

Program kickoff – March 25, 2024

Program metrics



	Metric	Phase 1 (18 months) Discrete components	Phase 2 (18 months) Integrated sensor module
	Environment(1)	> 1 hr at 800 °C in air	> 1 hr at 800 °C in air
Sensor	Dynamic range(2)	> 90 dB (simulated*)	> 90 dB (integrated)
	Bandwidth(3)	> 1 MHz (simulated*)	> 1 MHz (integrated)
Transistors (TC1)	Unity-gain bandwidth (f_T)	> 100 MHz	
	I_{ON}/I_{OFF}(4)	> 1000	
	Threshold voltage variability	< ±10%	
Transducers (TC2)	$MDS^{transducer}$(5)	< 1 Pa/√Hz	
	Linear pressure(6)	> 33 kPa	
	Bandwidth(3)	> 1 MHz	
Integration(7) (TC3)	Interconnect parasitic load(8)	Performer defined	
	Interconnect survivability(9)	at 800 °C	

*simulations are based on measured discrete device results

I_{ON}/I_{OFF} = transistor current ratio
$MDS^{transducer}$ = transducer limited minimum detectable signal

Metrics notes

(1) All metrics are to be reported at 1 hr operation at 800°C in air

(2) 1 Pa/√Hz pressure resolution measured at 1 kHz

(3) Bandwidth defined as the upper frequency range at which sensitivity is constant to within ≤ 3 dB

(4) I_{ON}/I_{OFF} = transistor current ratio

(5) $MDS^{transducer}$ = transducer limited minimum detectable signal

(6) < 1 dB deviation from linear device sensitivity

(7) Integrated total sensor surface area (i.e., sensing element plus other support structure flush with the sensing element) < 30 mm^2

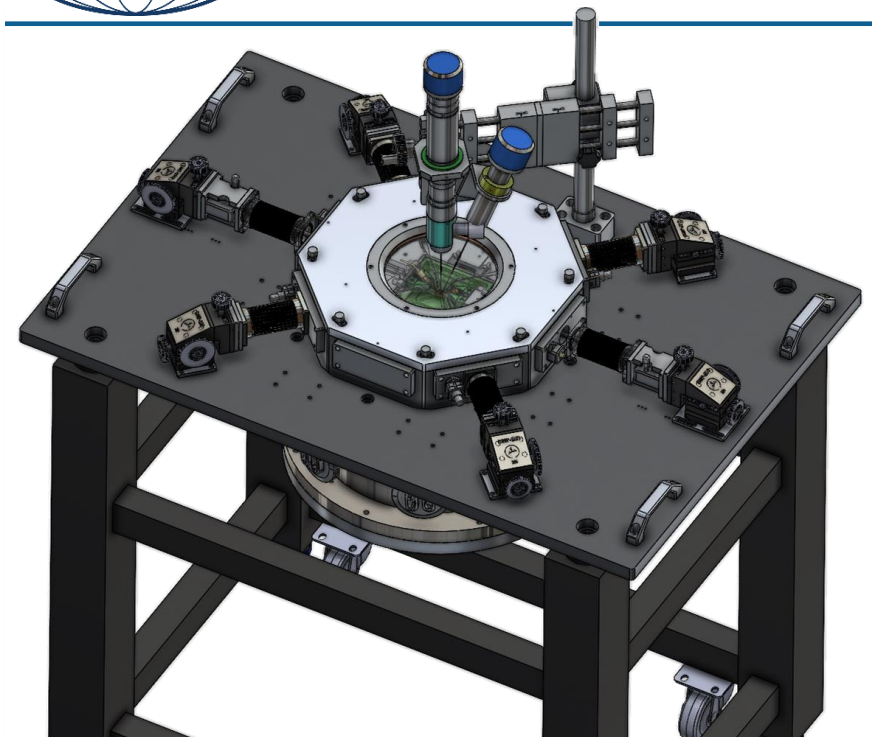
(8) Expected performer defined parasitic loads include resistance and capacitive loads, with quantitative metrics derived and supported by baseline model and simulation as well as test structures

(9) Survivability based on meeting or exceeding the interconnect parasitic load metrics for 1 hour

Test and evaluation

- Testing at 800°C presents unique challenges!
- All submitted proposals should outline technical tasks regarding developing test plan and capability to demonstrate meeting or exceeding the metrics
- Innovations in test to support demonstration of program metrics are encouraged
- Direct experimental demonstrations of program metrics are strongly encouraged
- Performers will be required to deliver test articles with sufficient documentation to support testing to the Government IV&V team, one quarter before the conclusion of each phase

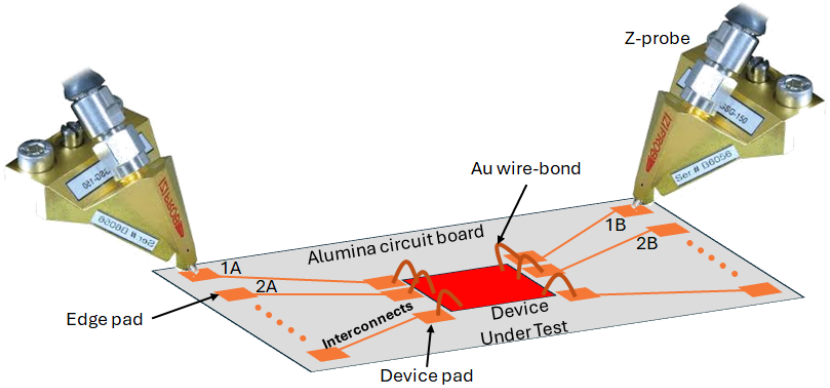
Transistor test & evaluation set-up



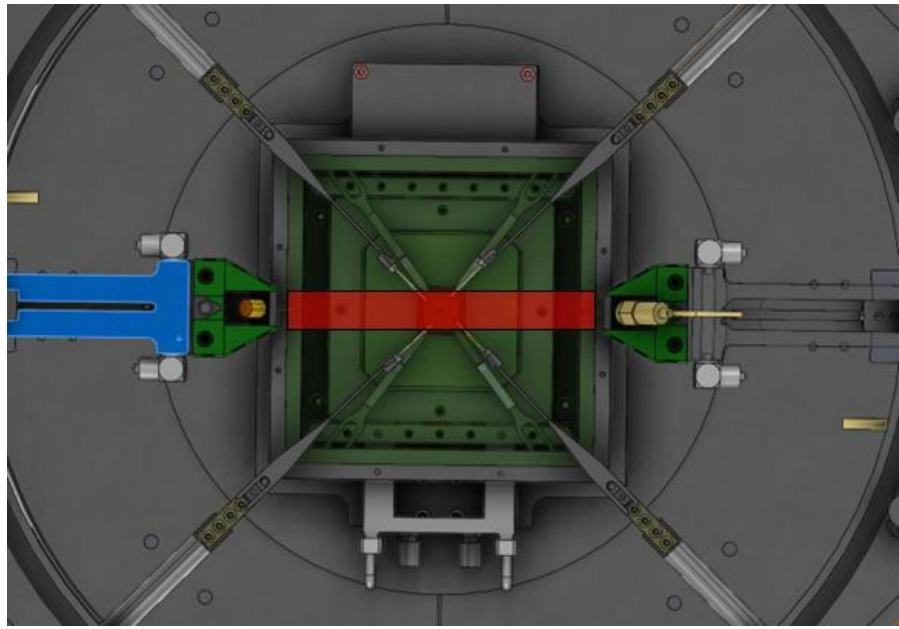
> 1000°C testing capability

INSTEC HP1000V-MP DC/RF System

- semi-automated system with 2” table
- DC (1000°C), RF (≥ 800°C, 9 kHz - 40GHz)
- Vacuum, Ar/N_2/Air, variable pressure (up to atm)
- Surface temperature measurement through window
  - kSA BandIT
  - Energy band edge thermometry



Transistor assembly on alumina board



Transistor positioning on INSTEC system

Transducer test & evaluation – direct pressure measurement



High-temperature plane wave tube

Transducer test & evaluation – reciprocal measurement



Laser Doppler vibrometer





Seven performer teams with diverse technical approaches











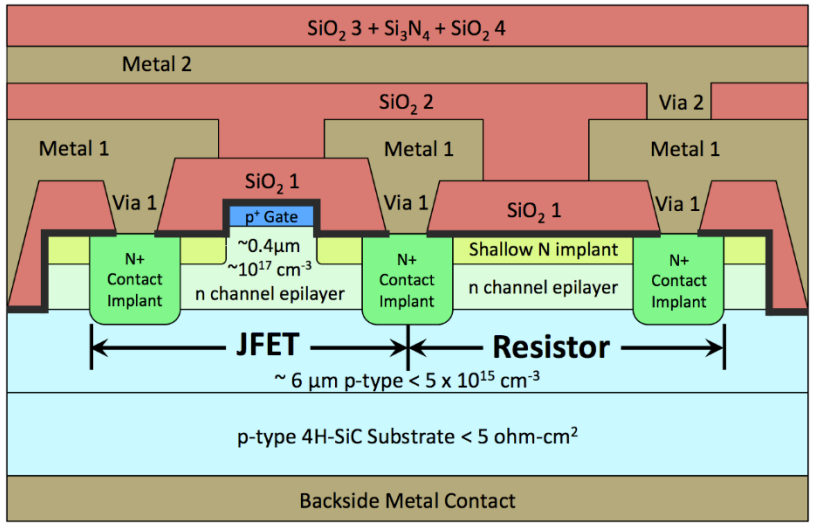




University of Florida – transistor and transducer approaches

NASA-Glenn's SiC n-JFET-R Transistor

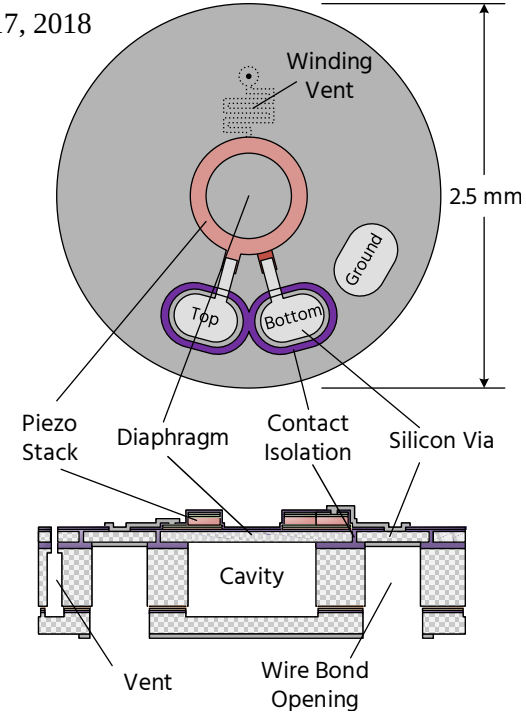
- Demonstrated durability at ≥800°C (>1 hour) and sub-MHz frequencies (LG = 6 µm)
- Proven high-temperature durable film stack
- Intrinsic LG = 1–2 µm enables f_T >100 MHz on 4H-SiC substrate



Neudeck et al., 2017, 2018

Piezoelectric Dynamic Pressure Sensor

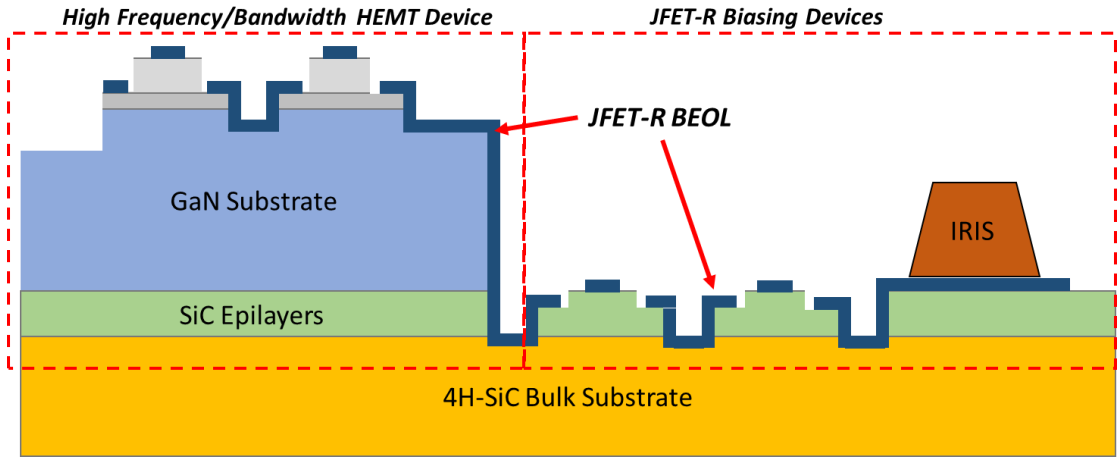
- AlN piezoelectric annular ring on a silicon diaphragm suspended over a cavity
- Backside wire bonds create a smooth surface for flow
- Frontside vent ensures static pressure equilibration



Ozark IC – transistor and transducer approaches

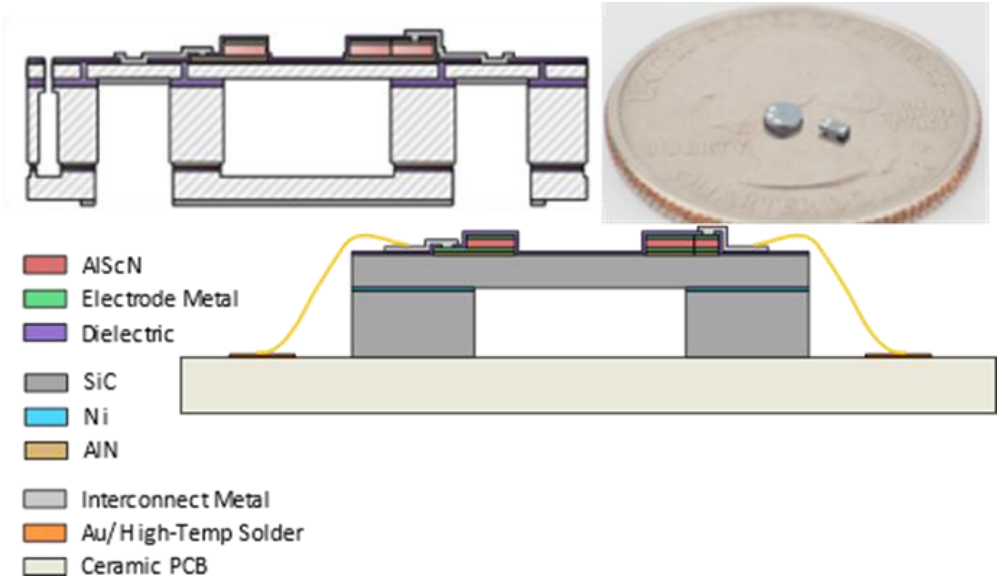
WBG GaN HEMTs

- Increased sheet charge enhances gain and bandwidth vs AlGaN HEMT at 800°C; Ultra-wide bandgap reduces three-terminal leakage
- Improved HEMT electrodes with high barrier height lowers gate leakage; no harmful intermetallic compounds below 1500°C
- Strain-engineered deposition at ~ 800°C minimizes stress under operating conditions



4H-SiC Pressure Transducer

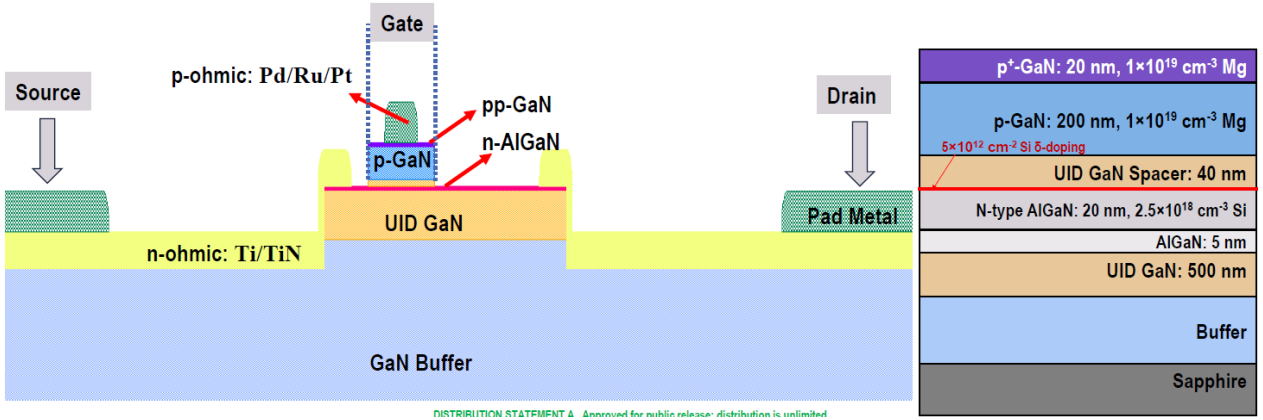
- Diaphragm design with a larger sensor diameter and relaxed amplifier input impedance requirements
- ~2x higher minimum detectable signal compared to Si-based MHz pressure sensors
- High Curie temperature piezoelectric AlScN improves SNR by up to 2x, compensating for SiC diaphragm limitations



Penn State University – transistor and transducer approaches

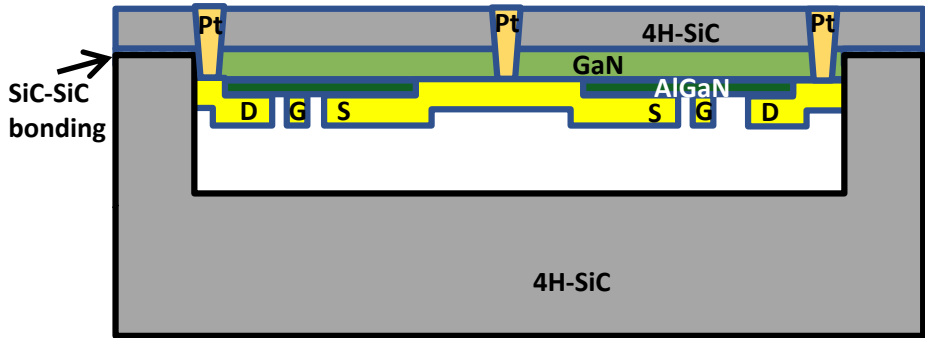
Super-heterojunction Field Effect Transistor

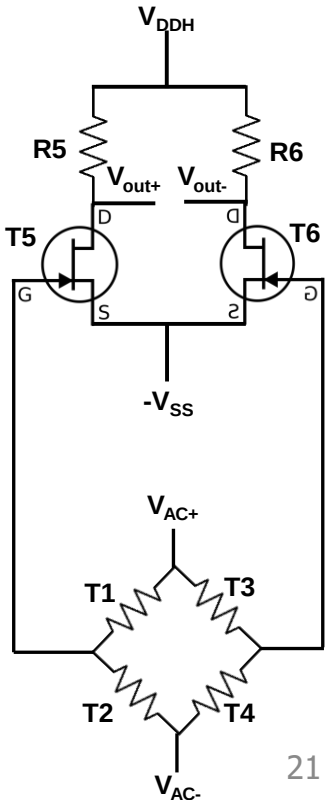
- Super-heterojunction gate with p-ohmic control gate leakage at 800°C
- Thermally stable transistor ohmic contacts (Ti/TiN for source/drain and Pd for gate) all with Ru/Pt cap layers
- p-GaN gate with in-situ TBCl etching to minimize gate leakage and to achieve tunable threshold HEMT operation



SiC Cavity Transducer

- SiC-SiC bonded cavity filled with N_2
- SiC diaphragm with GaN:AlGaN HEMT strain induced transduction in Wheatstone bridge
- Monolithic differential amplifier

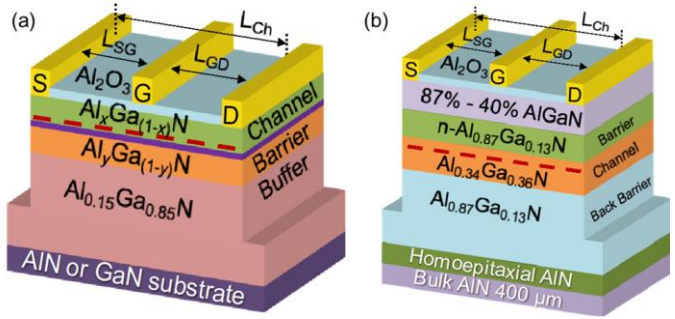




University of Texas Austin – transistor and transducer approaches

AlGaN high electron mobility transistors (HEMT)

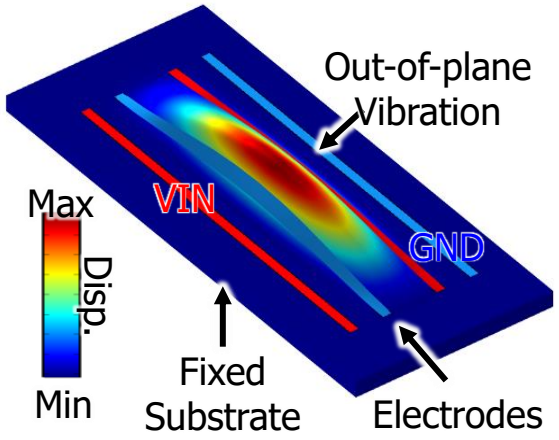
- Nitrogen polar HEMT on AlN buffer on sapphire substrate
- Metal-polar HEMT on AlN substrate as risk mitigation

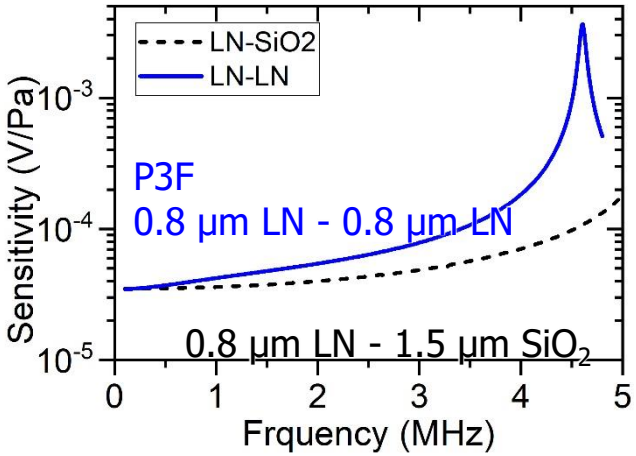


Material	Curie T (°C)	E Field	Sensor FoMs		
			e (C/m^2)	e/ε (GV/m)	$e/(\varepsilon \tan\delta)^{1/2}$ (10^6(J/m^3)$^{1/2}$)
PZT 53/47	350	TFE	18.7	1.30	1.1
PMN-PT	220	TFE	26.0	1.90	0.84
AlN (@25°C)	1150	TFE	0.68	6.99	2.2
$Al_{0.7}Sc_{0.3}N$ (@25°C)	1100	TFE	2.25	12.7	3.1
AlN (@800°C)	1150	TFE	0.85	6.40	0.052
$LiNbO_3$ (@25°C)	**1200**	**LFE**	**4.61**	**13.24**	**6.85**
$LiNbO_3$ (@800°C)	**1200**	**LFE**	**4.74**	**6.59**	**0.72**

Periodically Polarized Piezoelectric Film (P3F) lithium niobate ($LiNbO_3$) transducer

- $LiNbO_3$ – higher Curie temperature, lower dielectric loss, and higher piezoelectricity at 800°C
- Simulation suggests the integrity and stability of the $LiNbO_3$ structures
- (P3F) $LiNbO_3$: Piezoelectric bimorph structure enhances sensitivity by doubling the signal energy captured



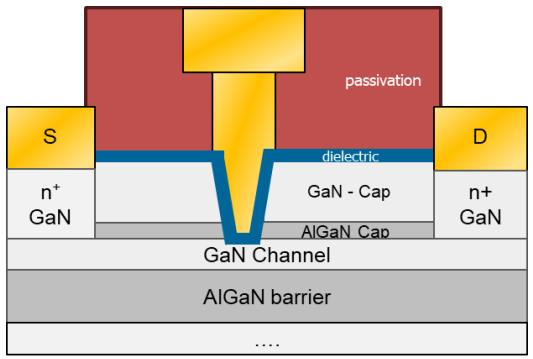


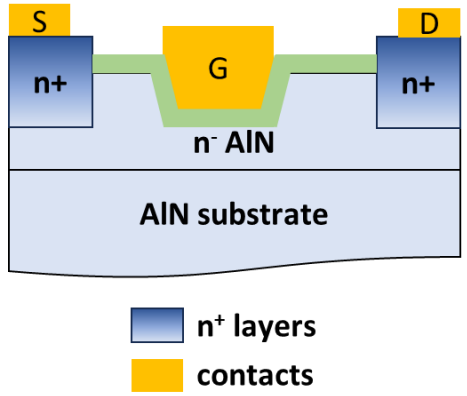
Distribution A: Approved For Public Release

Georgia Tech – transistor and transducer approaches

N-polar AlN and GaN FETs

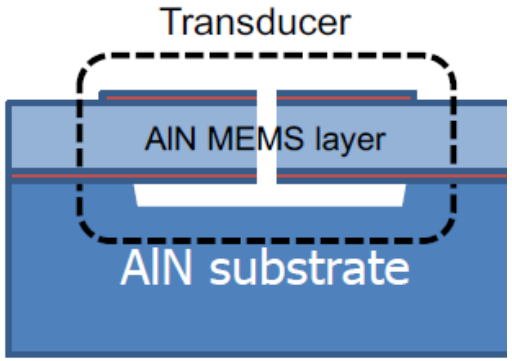
- Two different transistor technologies to mitigate risks
- ZnO and refractory metals for high temperature operation
- AlN substrate facilitates integration with pressure sensor

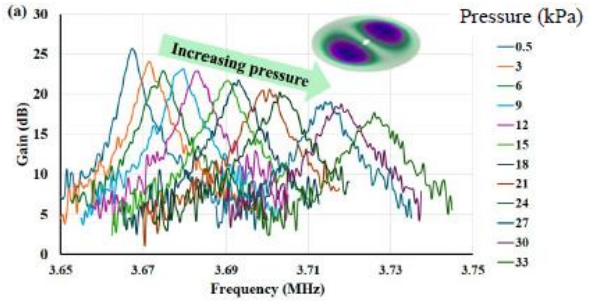


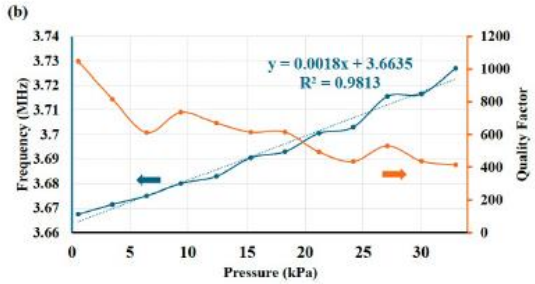


AlN pressure sensors

- CTE-matched AlN thin film transferred to AlN substrate with pre-etched cavities
- Restoring force applied to the thin oscillating membrane by the trapped gas in the cavity modulates the membrane stiffness and therefore its resonant frequency
- Resonant frequency shift sensing used to measure dynamic pressure



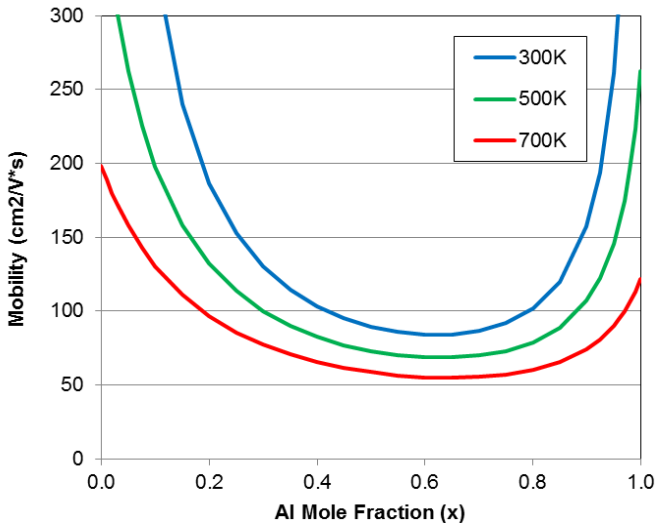


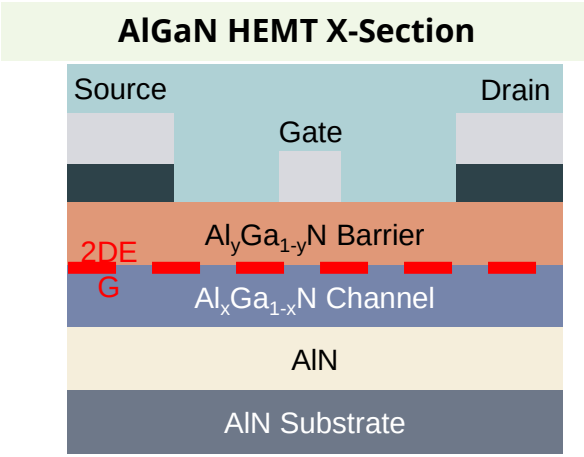


Sandia National Laboratories – transistor and transducer approaches

AlGaN Channel HEMT

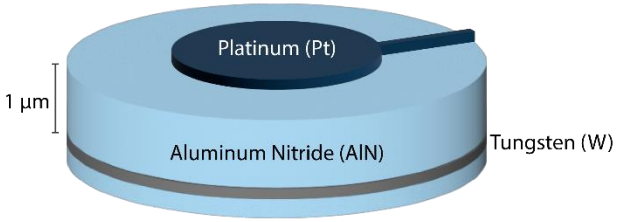
- Wide band gap HEMT suppress intrinsic carrier density effects and thermionic emission-induced leakage
- Mobility engineering for high temperature operation

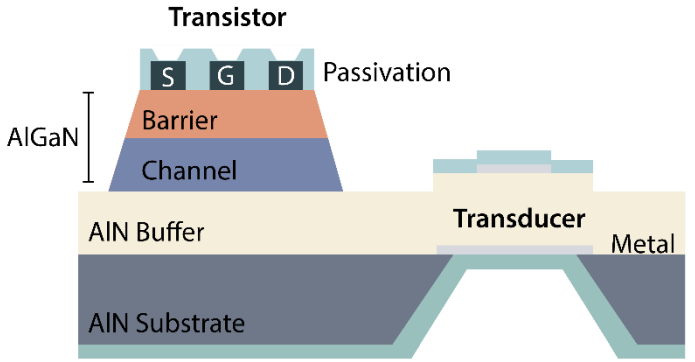




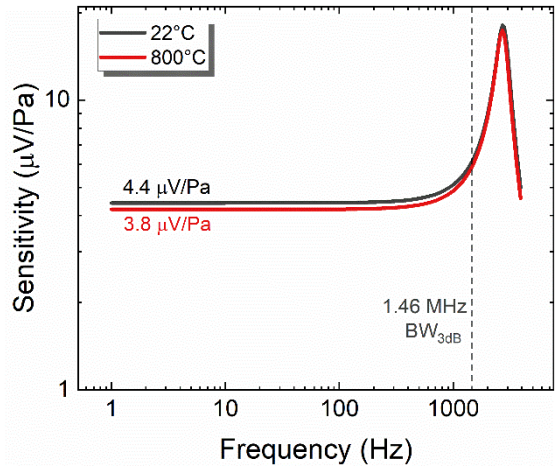
AlN Piezoelectric Transducer

- AlN substrate allows for high quality AlN films with low leakage and high piezoelectric performance at high temperature
- AlN as both the transistor channel and the piezoresistive element in the transducer enables monolithic integration





Simulated Sensitivity (S) with 100 Pa Pressure Wave



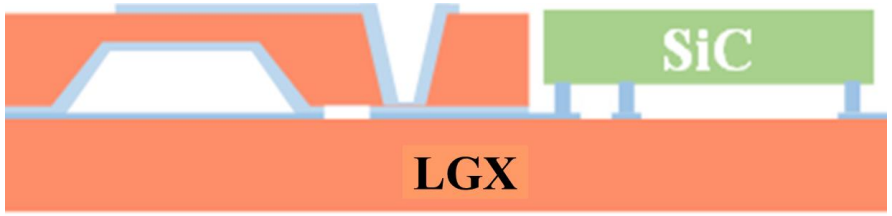
BAE – transistor and transducer approaches

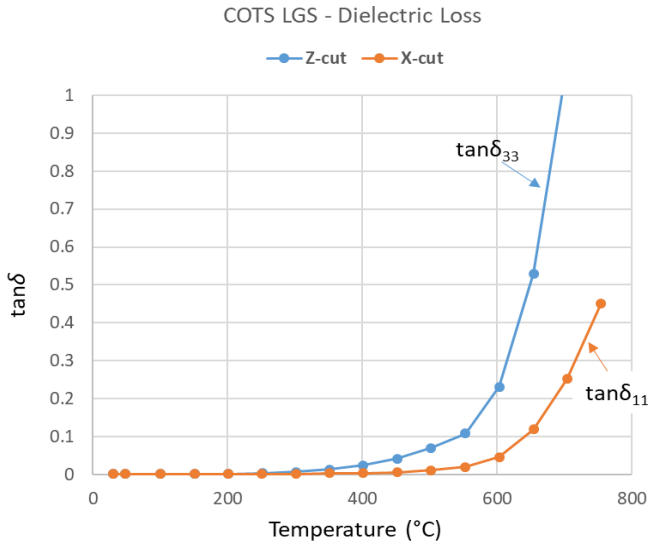
SiC JFET

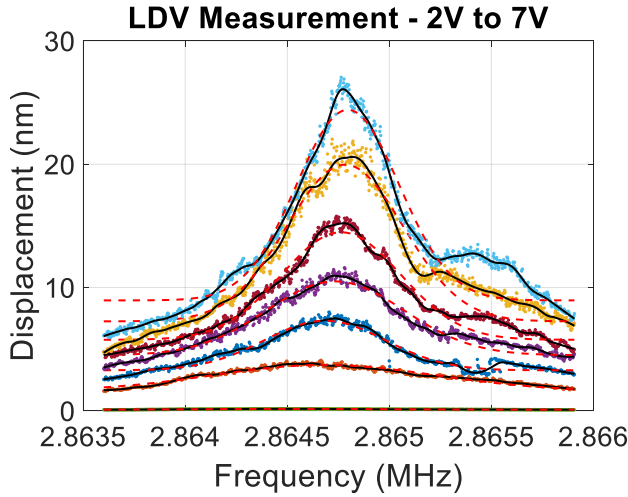
- Lateral multichannel SiC JFET with $NiSi_2$ contact metal
- TiW/Ti/Pt top metal
- SiO_x and SiN_x passivation

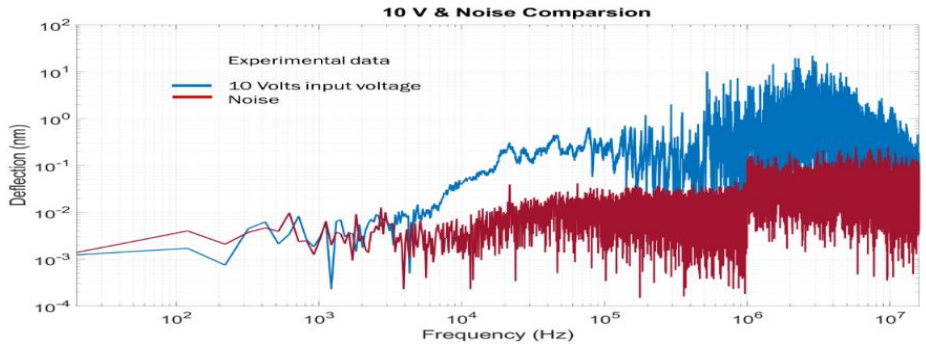
Langasite Piezoelectric Transducer

- Hermetic langasite diaphragm-over-cavity with Pt electrodes
- Monolithic integration of SiC JEFT IC to transducer by Pt-pillar compression bonding

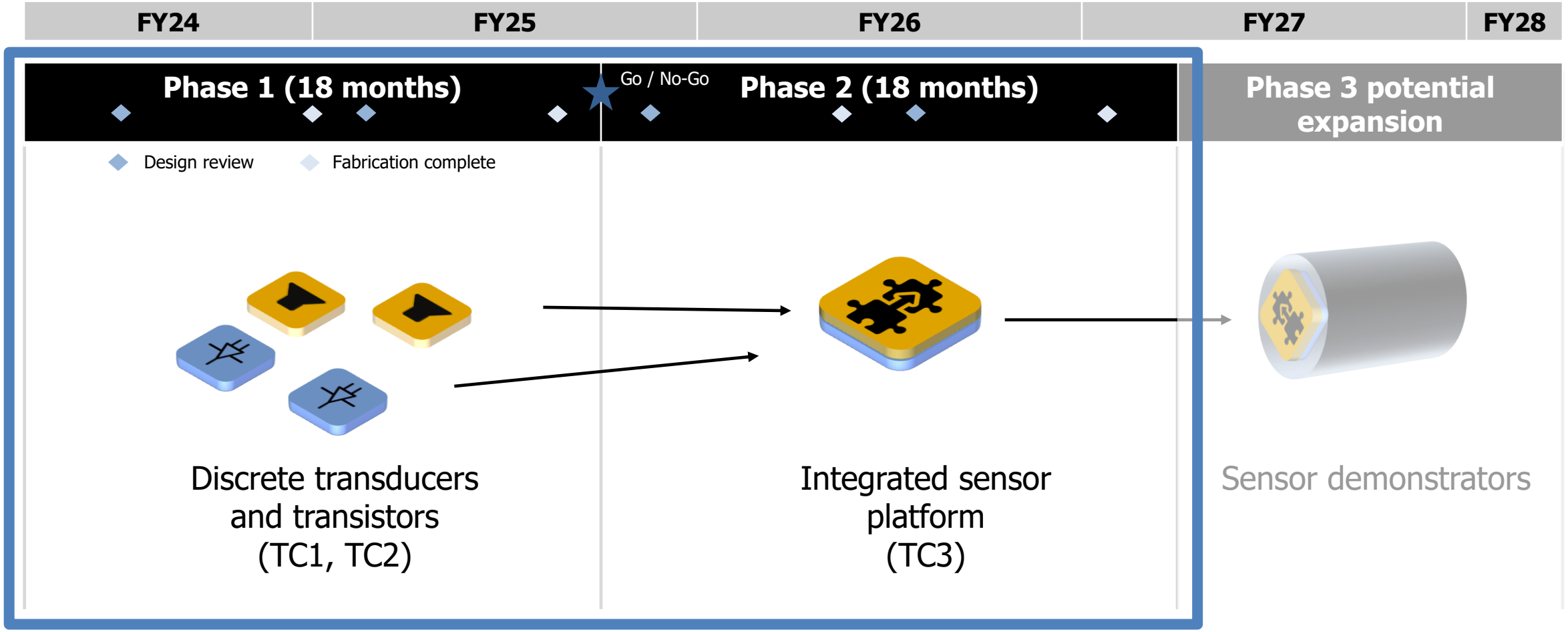








Program structure



End of Phase 1 – Summer 2025
Hardware due soon
IV&V to commence



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