Device Variability Compensation in High Temperature Electronics for Hall Sensing Applications

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Abstract

We demonstrate high temperature electronics for next-generation aircraft, focusing on the realization of a monolithically integrated active Hall effect sensor in SiC. This circuit is required to operate at temperatures up to 450 °C. A novel approach to operational amplifier design is introduced, employing discrete 4H-SiC JFETs and investigates the resulting variability in circuit performance for JFET prameter mismatches, subsequently leveraging these insights to optimize performance at temperatures up to 200 °C. Traditionally, a pair of transistors with highly matched turn-on voltage, is required for the realisation of a differential pair, a fundamental building block in op-amp topologoes. A novel method to compensate for the mismatch in turn-on voltage has been developed in a differential pair, allowing for significant improvements in gain despite a 1.3 V difference in threshold voltage between input JFETs. The op-amp circuit utilizes careful resistor selection in the source follower stages to ensure DC offset symmetry and reduce the influence of variation in JFET conductivity in the subsequent amplifier stages. The op-amp experimentally demonstrates an open loop DC gain of 71.5 dB and is shown to be effective in feedback networks and circuits integrated with a SiC Hall bar. An op-amp differential amplifier with a 359 DC voltage gain and 84 Ω output impedance was developed, and this circuit design offers adjustable signal amplification and significantly improved performance characteristics compared to conventional amplifier topologies.

Keywords

Aerospace, Analogue circuitry, SiC, JFET, Variability, Sensor, Reliability

I. Introduction

There is an increasing demand for more sustainable aircraft with minimal environmental impact, where the aviation industry is setting long-term goals to reduce carbon emissions significantly. In 2008 NASA set the goal by 2030 for reducing NOx emissions by over -75% and fuel consumption better than -70% for subsonic airliners [1]. Longer-term objectives have been set by UK aviation, aiming to achieve net zero carbon emissions by 2050 [2]. With this in mind, there has been a shift towards electrifying aerospace systems to help meet these requirements while cutting operating costs to meet market demands.

The More Electric Aircraft (MEA) is a hybrid solution towards the electrification of aircraft systems - replacing mechanical, hydraulic, and pneumatic actuating systems with one globally optimised electrical alternative [3]. With MEA, electrical machines are being developed for aircraft control systems, and there is a growing need to monitor position and current in extreme environments.

A sensor will be optimised for closed-loop current sensing in a four-phase inverter for electrical aircraft where there is a need to monitor current flow to incorporate feedback control to regulate the output, performance monitoring and power management. One appeal of Hall effect sensors over other technologies is the ability for the device to be constructed on a single semiconductor substrate. This makes the device more compact, potentially saving space and overall system cost [4]. Other advantages include a simple linear magnetic field response, the ability to operate in a large magnetic field range, high magnetic sensitivity, and low electronic noise [5]. The sensor will also be optimised for position-sensing applications, specifically tailored for integration within fuel solenoids and fuel injectors in jet engine systems. Hence, a Hall effect sensor is preferred for its ability to measure both position and current.

When using a hall element for position sensing, a circuit such as the block diagram in figure 1 can be used [6]. A constant current source is needed to drive the Hall device, allowing the Hall voltage to vary just from changes in magnetic flux density. The current source requires a reference voltage, which is supplied

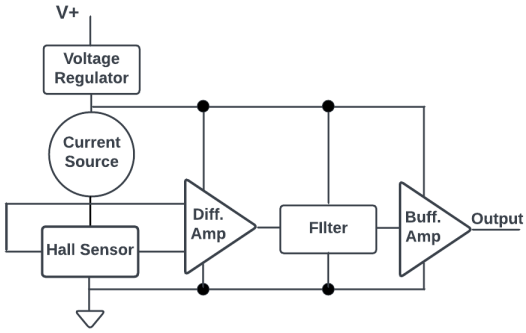


Figure 1: Functional block diagram for a Hall device analogue circuit

using a voltage regulator. The voltage regulator consists of an operational amplifier (op-amp), and may contain a bandgap reference, which also makes use of an op-amp. A bandgap reference provides a stable reference voltage independent of temperature or supply. Since V_H is usually in the micro-amp range, this must be amplified for practical applications. A differential amplifier amplifies the voltage difference across the hall device. The outputted signal is then filtered, rejecting frequencies generated by electrical or electromagnetic noise. Typically this is achieved using a low pass filter, only passing signals below its corner frequency. Finally, a buffer amplifier provides a low impedance output to prevent unwanted currents from the load, which may interfere with the signal source.

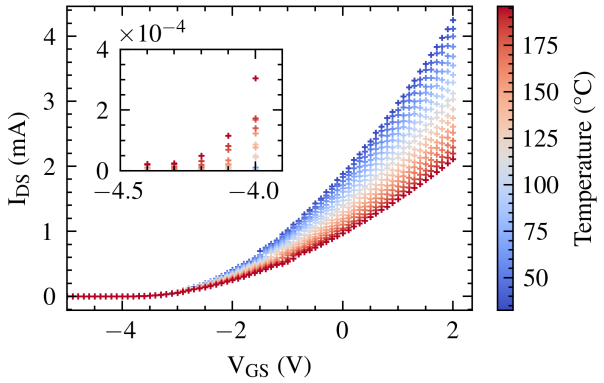
Silicon carbide (SiC) is the preferred semiconductor material for harsh-environment sensing applications because of its excellent material properties, derived from the high strength of the Si–C bond [7]. SiC has a wide bandgap energy (3.2 eV for 4H-SiC), excellent chemical and thermal stability, and high breakdown electric field strength (~2.2 MV/cm) [8]. SiC MOSFETs struggle with reliability in the oxide layer when operated at high temperatures or under high electric fields [9]. Consequently, transistors consisting of only p-n junctions, such as JFETs or BJTs, can withstand much higher temperatures when compared to transistors such as MOSFETs. However, BJTs are shown to have much lower efficiency through switching losses at higher temperatures, while SiC JFETs have demonstrated thousands of hours of continuous 500 °C operation [10, 11].

JFETs are shown to operate with low noise and high input impedance, which helps ensure precise signal amplification and effective oscillation in sensitive and demanding electronic applications [12–14]. Indeed, SiC JFET amplifier circuits have been demonstrated at temperatures up to 600 °C, and with characteristics comparable with similar high performance analogue circuitry [15, 16]. However, defects in SiC wafers and non-uniformity of epitaxial thickness and doping has imposed challenges in commercialising this technology. Large changes to key JFET electrical parameters are observed as a function of temperature and device radial position [17–19].

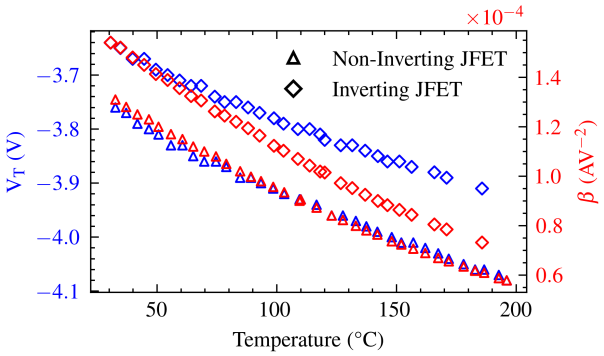
Integrated analogue circuit designs accounting for SiC device variability have been demonstrated to improve consistency in circuit performance for varying radial positions on a 4H-SiC wafer and temperature variation [19]. This work assumes perfect uniformity across devices in an IC. Here we optimise analogue circuit design, investigating the importance of device variability between 4H-SiC JFETs within a circuit.

II. Electrical characterisation of SiC JFETs

Parametric testing of the JFETs was performed using a Keithley 4200A-SCS parameter analsyer. The experimental data in figure 2a illustrate the drain-source current as function of gate voltage ($I_{DS} - V_{GS}$) for an example depletion mode 4H-SiC JFET in saturation, with a constant channel voltage V_{DS} = 15 V, as a function of temperature (for temperatures ranging from 32.6 °C to 196 °C). The observed saturation drain current decreases with increasing temperature for V_{GS} >threshold voltage,V_T, due to the reduction in device carrier mobility [20]. Moreover, the inset plot, for -4.5 V <V_{GS} <-4 V demonstrates a decrease in V_T with increasing temperature.



(a)



(b)

Figure 2: Channel current I_{DS} and voltage V_{GS} relation for a discrete JFET as a function of temperature (a). Extracted V_T and β at different operating temperatures (b).

As discussed in section III, the input stage of an experimentally demonstrated single-stage operational amplifier consists of an inverting and non-inverting JFET as a differential pair. The performance parameters V_T and transconductance parameter, β,extracted from data similar to that shown in figure 2a is plotted as a function of temperature in figure 2b for both devices. The data demonstrate a linear variation in β and V_T, where the non-inverting JFET linear regression model for both parameters have $R^2 = 0.99$. A more dominant linear decline in V_T is observed (as expected following work in [20]), while a second degree polynomial may better describe β (as realised in [20]) if characterisation was extended to higher temperatures. Nonetheless, the data clearly demonstrate non-equal forward conduction characteristics for both devices, and vary inconsistently with increasing temperature. The inverting JFET shows a greater reduction in β, $7.31 \times 10^{-5}\,\mathrm{AV}^{-2}$, compared to $9.06 \times 10^{-5}\,\mathrm{AV}^{-2}$ for the non-inverting JFET, while the shift in V_T shows a different variation with temperature (0.32 V compared to 0.28 V), for characteristics between 30 °C and 200 °C.

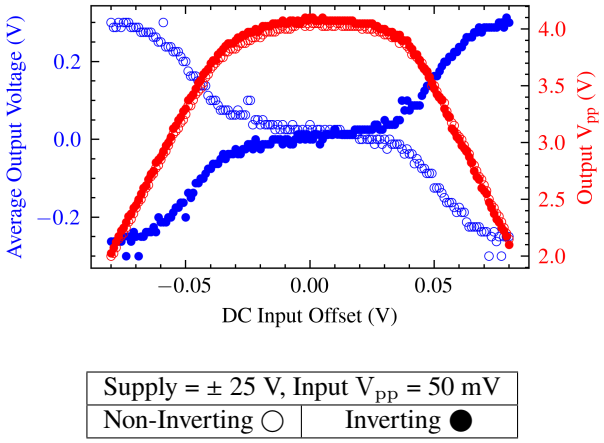


Figure 3: Average AC output voltage and peak-to-peak output voltage as a function of difference in DC offset voltage between inputs of the operational amplifier input stage.

III. Amplifier circuit designs

A. *Two-Stage Operational Amplifier*

A two stage operational amplifier circuit design was constructed and subsequently optimised at room temperature, consisting of four main sections as shown in figure 5. A long tail pair makes up the input stage, where a source resistor value is selected in the current source to determine both the desired current and overdrive gate voltage for the input JFETs. An overdrive gate voltage of 0.5 V was chosen as a compromise between increased gain and reduced leakage current [15]. This introduces the first challenge of designing with discrete 4H-SiC JFETs. Traditionally, a pair of well-matched transistors, particularly in turn-on voltage, is required for use in a differential pair, allowing an equal current and overdrive voltage across the JFETs. It was found by adding a source resistor on the branch with lowest drain-source resistance, r_{ds}, can effectively balance resistances where there is severe device mismatch. Applying this method has enabled a voltage gain of 62.4 to be extracted from a differential pair with transistors differing in turn-on voltage by 1.3 V, where using traditional methods limited the gain to 38.4. However, following equations 1 and 2, an additional resistor on a branch reduces V_{DS} across the JFET, limiting the drain resistance and therefore the gain further, but still offers significant improvements in performance especially when preventing large differences in overdrive gate voltage, see figure 3. Drain resistors were selected to maximise gain while allowing the input JFETs to reliably operate in the saturation region.

$$|A_{dm}| = g_m\,(r_o \parallel R_D) \tag{1}$$

$$V_{DS} = V_{DSx} - I_{DS} \cdot R_D \tag{2}$$

where g_m is the transconductance of the input differential pair, r_o is the small-signal transistor output resistance. In equation 2, V_{DSx} represents the externally applied voltages.

The second section, shown in blue, are the source source follower level shifters, acting as a buffer between the first and second amplification stages while shifting the DC offset to effectively bias the second differential pair. The current sources in this stage both determine the amount of DC level shifting and the output impedance from the input stage, as described in equations 3 and 4. Smaller source resistances, R_S, are used in this current source, compared to amplification stages, to allow for a higher current and relatively low source resistor in the source follower to achieve a desired level shift to better limit overdrive gate voltage and output impedance:

$$V_{\text{out}} = V_{\text{in}} - I_{DS}R_S - V_T - \sqrt{\frac{I}{\beta}} \tag{3}$$

$$Z_o = R_S \parallel \frac{1}{g_m} \tag{4}$$

where V_{out} and V_{in} are the respective output and input voltages from the source follower stage. In equation 4, Z_o represents the output impedance and g_m is the transconductance of the JFET.

One of the biggest obstacles in circuit design with discrete devices in the two-stage op-amp, is accounting for device variability between the source followers that connect the two amplification stages. Equation 3 highlights how unequal key electrical characteristics, mainly V_T, accounts for DC level shift, represented by V_{out}. One must therefore compensate by changing R_S to ensure balanced transistor conductivity in the second amplification stage. A large negative DC offset of around -4 V is desired at this stage to bias the second long tail pair with a high transconductance, maximising gain, as seen in equation 1. Subsequent sections include a single ended output differential pair producing further signal amplification and a final source follower stage to

reduce output impedance and trim the DC offset voltage to zero.

B. Differential Amplifier

A differential amplifier circuit was realised using the two-stage op-amp design as a differential amplifier structure shown in figure 4. We demonstrate the op-amp circuit working successfully in feedback, offering adjustable signal amplification and significantly improved performance characteristics compared to conventional amplifier topologies [15, 21]. The circuit design has equal input resistors R1 and R2, and the feedback resistor R3 is the same as R4. Careful resistor matching is crucial to minimise sensitivity to common mode signals. For instance, a mismatch of 0.1% between resistor pairs will result in a CMR of only 66 dB no matter the CMRR of the op amp [22]. Therefore, high precision resistors are carefully selected when optimisng the feedback network of the op-amp circuit.

Choosing the resistor values depends on the circuit's intended application as both gain and output impedance are inversely proportional to the feedback factor,

$$\beta_{fb} = \frac{R_2}{R_2 + R_3} \tag{5}$$

where in figure 4, R_3 is the feedback resistor and R_2 is R_{in}, assuming $R_1 = R_2$ and $R_3 = R_4$. In this work, $R_1, R_2 = 3.9\,\mathrm{K\Omega}$ and $R_3, R_4 = 1.5\,\mathrm{M\Omega}$ resistor values were selected to offer a theoretical voltage gain of 385 and predicted output impedance 50 Ω, based on simulation.

C. Single-Stage Operational Amplifier

A single-stage operational amplifier was engineered and subsequently optimised to function up to $200\,^{\circ}\mathrm{C}$. In order to design a circuit to reliably operate at extreme temperatures, one must first understand how each stage behaves in these conditions. Overdrive gate voltage in the amplification stage, as discussed earlier, is dependent on JFET transconductance, threshold voltage and I_{DS}. All three are subject to temperature change as observed in figure 2. A change in overdrive voltage can result in loss in gain and device pinch-off, while an inconsistent change between input transistors can limit gain even further with loss of signal integrity and potential total loss of output, as shown by the data in figure 3. Moreover, one must be careful to not select too large drain resistors at the input stage, as loss in transconductance may cause JFETs to fall out of saturation, as demonstrated in equation 2.

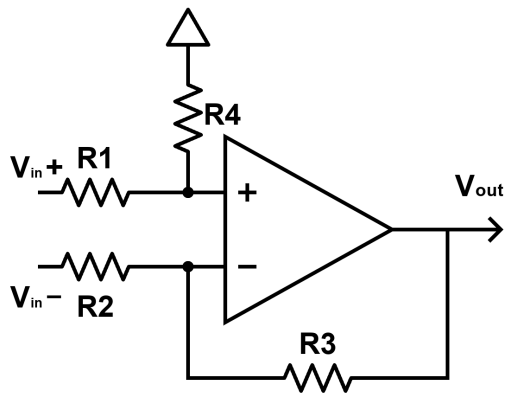


Figure 4: Schematic of a differential amplifier circuit

Changes in I_{DS} from the current source with increasing temperature can be accounted for by tuning the source resistor to achieve the desired current at a temperature corresponding to midway in total current variation, avoiding any significant changes to circuit performance. A positive relationship between temperature and output current is observed, and is due to the inherent temperature dependence of the JFET characteristics, as shown in figure 2, increasing JFET conductivity for a given V_{GS}. Similarly, in source follower stages, source resistors can be adjusted to minimise the total shift in DC output with temperature, as well as reducing the offset between the two. DC level shift, as determined in equation 3, decreases with temperature where the V_{GS} setting a lower quiescent point as device conductivity increases.

When considering device uniformity, in the source follower stage, temperature variation can lead to signification distortion of a two-stage amplifier output voltage. As shown in figure 3, a DC input offset of 50 mV at the differential pair input results in almost complete loss of symmetry in sine wave output, where a $1.34\times$ difference in positive and negative amplitudes is observed, while reducing the DC voltage gain by 30. Selecting JFETs with larger transcondctance parameters and threshold voltages will help reduce loss in performance due to device variability, where change in conductivity is minimised for a given change in temperature, as seen in figure 2. Similarly, by choosing a smaller overdrive gate voltage, JFETs operate with a higher transconductance and have less variation in performance. One must be conscious when designing such amplifier circuits to select devices with similar electrical characteristics, and with similar temperature variation, but also characteristics best suited to cope with device non-uniformity.

IV. Performance of amplifier circuits

A. Two-Stage Operational Amplifier

The open loop DC voltage gain, $A_{OL} = 71.7 \pm 0.1$ dB , for a two stage operational amplifier, using the topology shown in figure 5, was extracted from the differential input-output transfer characteristic from the circuit using a ± 25 V power supply. As can be observed from the data presented in figure 6a, a linear relationship shows a constant gain, exists between input and output peak-to-peak voltage before reaching saturation. The circuit was powered using a ± 25 V power supply. From the data, saturation is taken to be at a residual - 0.082 V output V_{pp} or lower

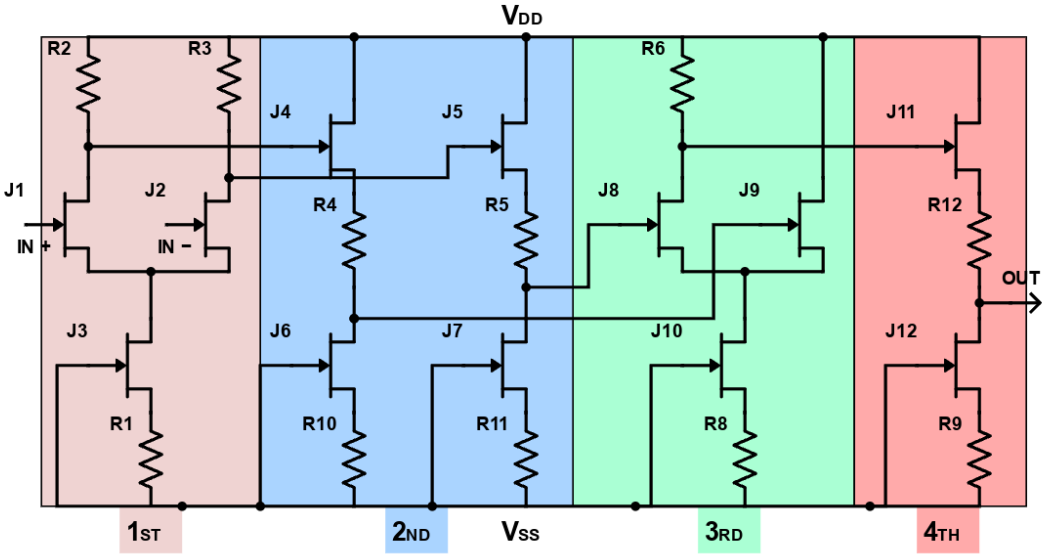


Figure 5: Schematic of a two-stage operational amplifier circuit with sections 1-4

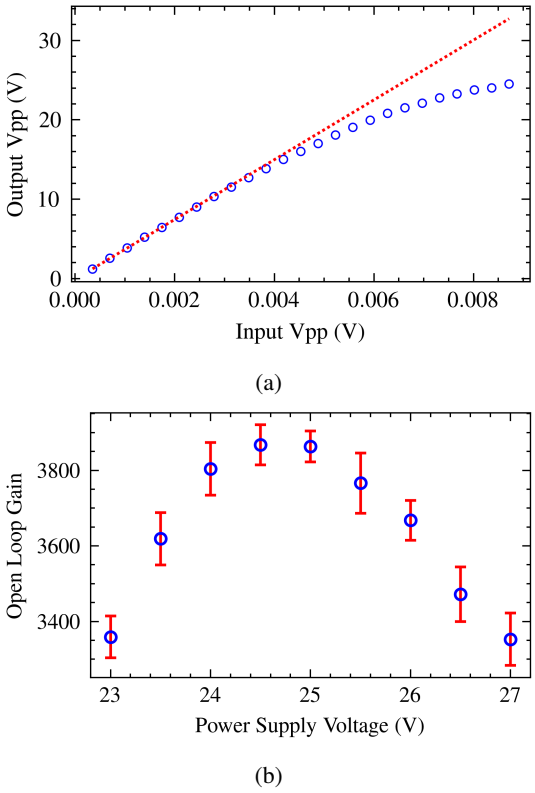


Figure 6: Output and input peak-to-peak voltage relation for the two-stage operational amplifier circuit (a). Extracted open loop gain as a function of ± power supply voltage applied to both V_{DD} and V_{SS} (b).

from the regression line at 10.3 V output V_{pp} and 2.8 mV input V_{pp}. The extracted A_{OL} is greater than or comparable to similar SiC based amplification structures [16, 19]. The high open loop gain helps achieve a larger closed loop gain with reduced non-linearities when operated in feedback as well as improved stability and bandwidth [23].

The DC gain of the amplifier circuit extracted from the data shown in figure 6a is plotted as a function of power supply voltage in figure 6b. The data demonstrates a maximum variation of 514 ± 87 in open loop gain from a ±2 V variation in supply voltage. Considering A_{OL} remains high, performance degradation in feedback circuits due to supply voltage variation will be minimal.

B. Differential Amplifier

The DC voltage gain from a differential amplifier circuit, as shown in figure 4, without load, $A = 359 \pm 1$, and with a 10 kΩ load, $A_L = 356 \pm 1$ were extracted from the data shown in figure 7. This circuit was demonstrated with a ± 25 V power supply. Limited by the open loop gain of the op-amp, the experimentally verified A is close to the theoretical gain, 385. Comparing the circuit's performance with different load resistors, an output impedance of 84 Ω was calculated using

$$R_{\text{out}} = R_L \left(\frac{V_{O1}}{V_{O2}} - 1 \right) \tag{6}$$

where R_{out} represents the output resistance of the circuit, R_L is the load resistance, V_{O1} is the output voltage with the load, while V_{O2} is the output voltage without a load.

Increasing the feedback factor described in equation 5, offers a

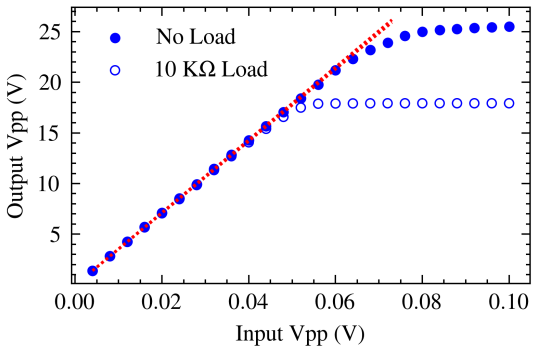


Figure 7: Output and input peak-to-peak voltage relation for the differential amplifier circuit without a load and with a 10 KΩ load.

reduced output impedance and improved agreement between circuit performance with ideal op-amp characteristics. This circuit demonstrates the realised two-stage op-amp operating in negative feedback with improved gain and output impedance compared to similar amplification topologies [15, 21].

C. *Single-Stage Operational Amplifier*

The performance metrics differential gain, A_{OL} and common mode rejection ratio, CMRR, were realised at temperatures up to 200 °C for the single-stage op-amp circuit as shown by the data in figure 8. The circuit was demonstrated with a ± 25 V power supply. The decrease in differential gain is considered to be due to loss in JFET transconductance for a given overdrive gate voltage, resulting from the decrease in key performance parameters, as observed in figure 2. Common mode signal gain, A_{cm}, also shows a decline but at a slower rate compared to A_{OL}, due to an increase in device conductivity asymmetry in the input differential pair. Consequently, a sharp reduction in CMRR is observed, but appears to level off beyond around 150 °C. This suggests matching gradients between A_{OL} and A_{cm} as they decrease with temperature above 150 °C. It is thought, this relationship is because device conductivity mismatch results in one JFET being pinched-off at $V_{GS} < V_T$, preventing further non-uniformity in branch resistance in the differential pair. This behaviour is also observed in figure 10, showing a dramatic shift in AC output symetry for a sine wave at temperatures beyond 150 °C.

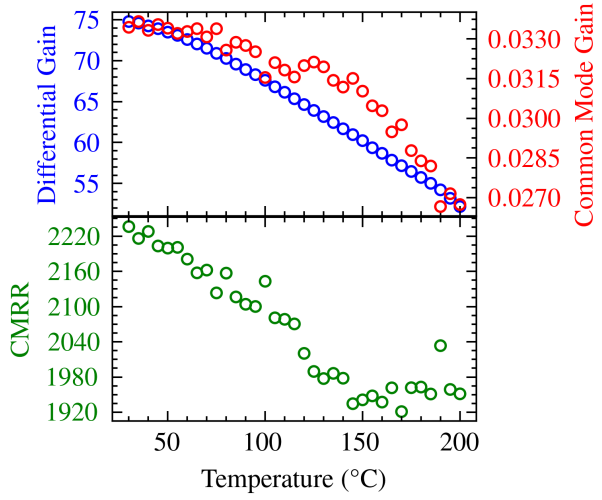


Figure 8: Extracted differential gain (A_{ol}), common mode gain (A_{cm}), and common mode rejection ratio at temperatures up to 200 °C

V. Temperature dependent SiC JFET device variability

Figures 9 and 10 demonstrate an increase in JFET variability at temperatures up to 200 °C. The DC output voltage is measured from the two source followers in section 2 of figure 5, shown in blue, from the single-stage op-amp and the DC offset is determined as shown in figure 9. The data clearly demonstrates an increase in DC output and reduction in level shift from the two source followers, in addition to an increase in voltage offset. This circuit was optimised at room temperature, and without accounting for key performance parameter variability, namely V_T (equation 3), the circuit would not function correctly as a two-stage op-amp at 200 °C. This is because the JFETs in the second amplification stage would operate with different transconductance, resulting in loss of gain, unbalanced conduction in the differential pair, and complete loss of symmetry in the signal output, as observed in figure 3. Temperature dependent device variability compensation techniques in op-amp circuit design are described in section IV C.

As shown in figure 10, a deviation in average AC output voltage between inverting and non-inverting outputs from a single-stage operational amplifier is observed with increasing temperature. This data demonstrates a reduction in symmetry between JFET

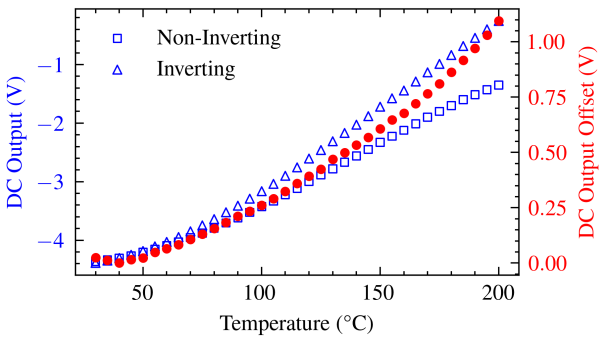


Figure 9: DC output voltage from the inverting and non-inverting inputs from the first source follower stage of the op-amp circuit, and the offset between the voltages, at temperatures up to 200 degrees.

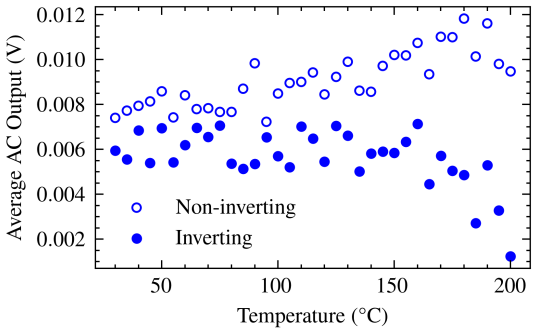


Figure 10: Average AC output voltage as a function of temperature for both single-stage op-amp outputs.

conductivity in the input stage differential pair up to 200 °C. An initial non-zero AC output voltage is present due to device mismatch at room temperature limiting CMRR. The sharp deviation in average AC output voltage at temperatures above 150 °C is considered to be caused by device pinch-off in one JFET in the differential pair input stage, as non-uniformity in branch resistance increases. The same relationship is demonstrated in figure 3, where an imbalance in voltage input bias causes an initial gradual change in AC output symmetry, which increases significantly as one JFET enters the pinch-off region.

VI. Conclusions

A novel approach to operational amplifier circuit design is introduced, employing discrete 4H-SiC JFETs. The significance of device variability between devices is investigated and we leverage these insights to optimise the performance of op-amp circuits. A realised op-amp circuit experimentally demonstrates an open loop DC voltage gain of 71.7 ± 0.1 dB. This circuit is shown to be effective in feedback networks and has been engineered as a differential amplifier offering adjustable signal amplification and significantly improved performance characteristics compared to conventional amplifier topologies. Careful resistor selection, and device bias control is demonstrated to reduce non-uniformity in JFET conductivity in amplification stages as well as DC level shifting in source follower stages, as temperatures approach 200 °C. Moreover, a novel method to turn-on voltage compensation has been developed in a differential pair, allowing for significant improvements in gain despite a 1.3 V difference in threshold voltage between input JFETs. In addition to selecting JFETs with similar electrical characteristics, it is shown devices with certain performance metrics can offer greater performance in spite of device non-uniformity with temperature.

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