Additively Manufactured High Temperature Passive RF Components

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Abstract

There is growing interest in extreme temperature electronics to support instrumentation for sensors at temperatures beyond the normal range of electronics. Reliable packaging in the temperature range of more than 300°C has been demonstrated using ceramic multi-chip modules using conventional hybrid circuit technology. This approach typically requires high NRE costs and lead time. Additive manufacturing processes of ceramics, conductors, and dielectrics provides a digital transformation of hybrid circuit manufacturing technology that reduces time and cost for packaging with the added benefits of novel 3D structures and embedded features. This report extends these materials and direct die interconnect methods to demonstrate RF components that operate in the 300 to 750°C range. Design, fabrication, and testing of resistors, capacitors, and inductors that were printed in 2D and 3D freeform formats are presented.

Key words

Additive electronics, high temperature packaging, reliability, SiC

I. Introduction

There is growing interest in extreme temperature electronics to support instrumentation for sensors at temperatures beyond the normal range of electronics. Reliable high temperature packaging for 300°C has been demonstrated using ceramic multi-chip modules using conventional screen-printed hybrid circuit technology [1,2]. This approach typically requires high NRE costs and lead time. Additive manufacturing processes of ceramics, conductors, and dielectrics provides a digital transformation of hybrid circuit manufacturing technology that reduces time, waste, and cost packaging for prototypes with the added benefits of novel 3D structures and embedded features.

GE Research and Binghamton University have demonstrated additive materials and processes for packaging and direct die interconnects for extreme temperatures under funding from NextFlex [3,4,5,6,7]. This paper will present additional results of additive fabrication of planar and freeform RF components leveraging the learnings from these programs. The components fabricated in this program are resistors, capacitors, and inductors. The components were characterization over the temperature range of 300°, 500°, and 750°C.

The processes to additively fabricate ceramic sawtooth resistors, cylindrical spiral inductor, and conical spiral inductor were developed. Examples of components are shown in Figure 1. Planar resistors were printed using an nScrypt 3Dn Tabletop and Optomec AJ-300 Aerosol Jet Printer (AJP). Planar capacitors and spiral inductor were printed by AJP for the electrodes and a Nordson EFD PRO4L for the MIM capacitor dielectric. The freeform printed inductors were printed using an Optomec AJ 5X Aerosol Jet 5 axis printer. No suitable freeform capacitor was fabricated due to limitations with how thin a dielectric could be formed in 3D with these materials.

II. Additive Ceramic Printing

Additively printed alumina is selected because its capability for high reliability electronics packaging and compatibility with the materials targeted for this program. The ceramic printing used a Lithoz CeraFab 7500 DLP printer to print the slurry and form the initial shape. The forms are created in CAD and exported as STL files to use by the printer. The shape is dried and sintered to solidify the shape. During this process there is shrinkage, so the initial printed part is made to compensate for the shrinkage. The high sintering temperature, 1600°C, can also induce thermal stresses and temperature uniformity is required.

The saw tooth resistors printed well on the first attempt. The spiral inductor was printed with two

attempts. The first attempt printed the base vertically with the cylinder horizontal to the build plate. Rod supports were added under the tube, which were removed after printing. Small pieces of the cylinder were pulled out during support removing, leaving behind negative features on the tube wall. A second print attempt was done with the spiral inductor flipped 90 degrees so that the base is parallel to the build plate and the cylinder prints vertically. The conical inductor modeled in HFSS to define the geometrical parameters to create a solid model needed for ceramic printing. A hole is made in the top and bottom of the inductor to allow for drainage of the ceramic slurry with a wall thickness greater than 0.5 mm. Two inductors are printed on the same build plate and removed. Care is needed when removing to prevent fracture.

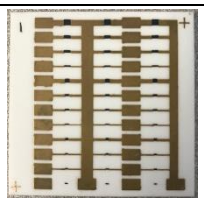
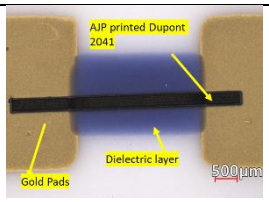
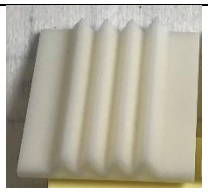
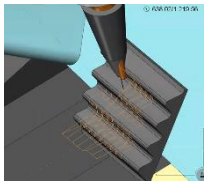
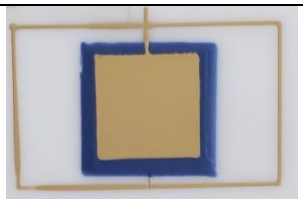
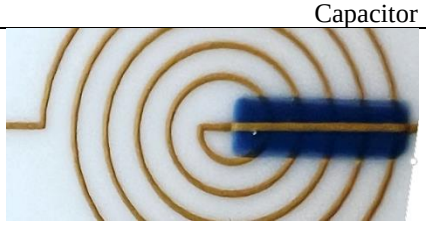
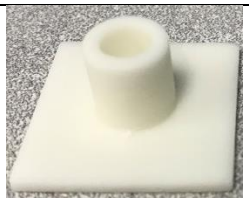
Component	Planar	Freeform
Resistors	 Resistor Test  AJP Resistor	  Saw Tooth Resistor
Capacitors	 MIM Capacitor  Interdigitated Capacitor	Was not able to fabricate significant and useful values given the materials and capability of the additive processes.
Inductors	 Planar Spiral Inductor	 Cylindrical Inductor  Conical Inductor

Figure 1 Examples of Fabricated RF Components

III. Component Fabrication and Testing

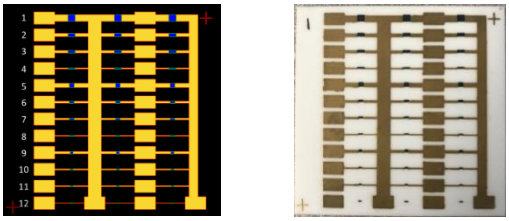
The conductors and dielectrics used to print the components are listed in Table 1. The materials were characterized in [7] with the addition of the resistor material used in this paper. The materials are provided with rheology suitable for nScrypt microdispense printing. Au1 has a small particle size (<1 µm) that allows it to be diluted and atomized for AeroJet printing. Details regarding the performance and testing of this material and other Aerojet printed materials can be found in [5].

Table 1 Thick Film Properties

Type	Conductor	Dielectric	Resistor
Material ID	Au1	D1	R50, R1k, R10k, R1M
Description	Au conductor	Dielectric	RuOx
Particle Size (um)	<1 um	<5 um	<5 um
Viscosity (Pa-S, Kcps)	300-400	80-120	140-220
Resistivity (Ω-cm or Ω/□)	5.00E-06	NA	50, 1k, 10k,1M Ω/□
Dielectric Constant (@ 1MHz)	NA	8-10	NA
Dissipation Factor (@ 1MHz)	NA	<0.002	NA

Resistor Printing and Testing

Each sheet resistance material was printed and tested for stability at 300°, 500°, and 750°C for a minimum of 100 hours in air. The resistors were printed dispense printed using a nScrypt 3Dn Tabletop and Nordson Pro4L and diluted for Aerojet printing with Optomec AJ-300 and 5X Aerojet printers. A test pattern was dispense printed to evaluate each sheet resistance with a range of resistor values that may be useful in an analog or RF circuit. The test pattern is shown in Figure 2. The test pattern was made by printing an interconnect pattern with varied gaps using Au1, firing, and printing the resistor material between the gaps so it overlaps the gold pattern then fired.



a. Artwork. Resistors shown in blue

b. Printed test sample after 150 hours at 300°C

Figure 2 Resistor High Temperature Stability Test Substrate.

The resistor material shrinks after drying due to solvent loss and during firing due to sintering. Figure 3 plots the percent shrinkage in the R50 and R1M resistors. The width shrinks much more for the R1M but not much for R50 while the height shrinks much more for the R50 than the R1M.

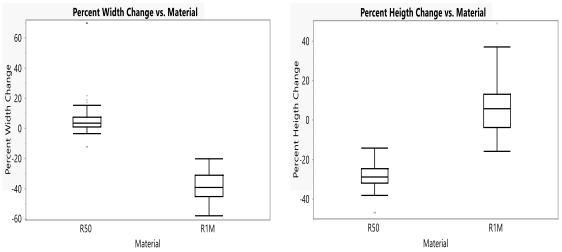


Figure 3 Resistor Shrinkage after 850°C firing

Samples of each resistor material were measured for resistance at room temperature at intervals after aging at 300°, 500°, and 750°C. Figure 4 contains plots of the resistance of the printed samples over time. The mean resistance stability of the four resistor materials is consistence over time at 300°C and 500°C. The R10K material increase in resistance within the first 25 hour at 300°C then remained stable. The resistances were not stable at 750°C and inconsistent. The R50 resistor increased over time while the others decreased.

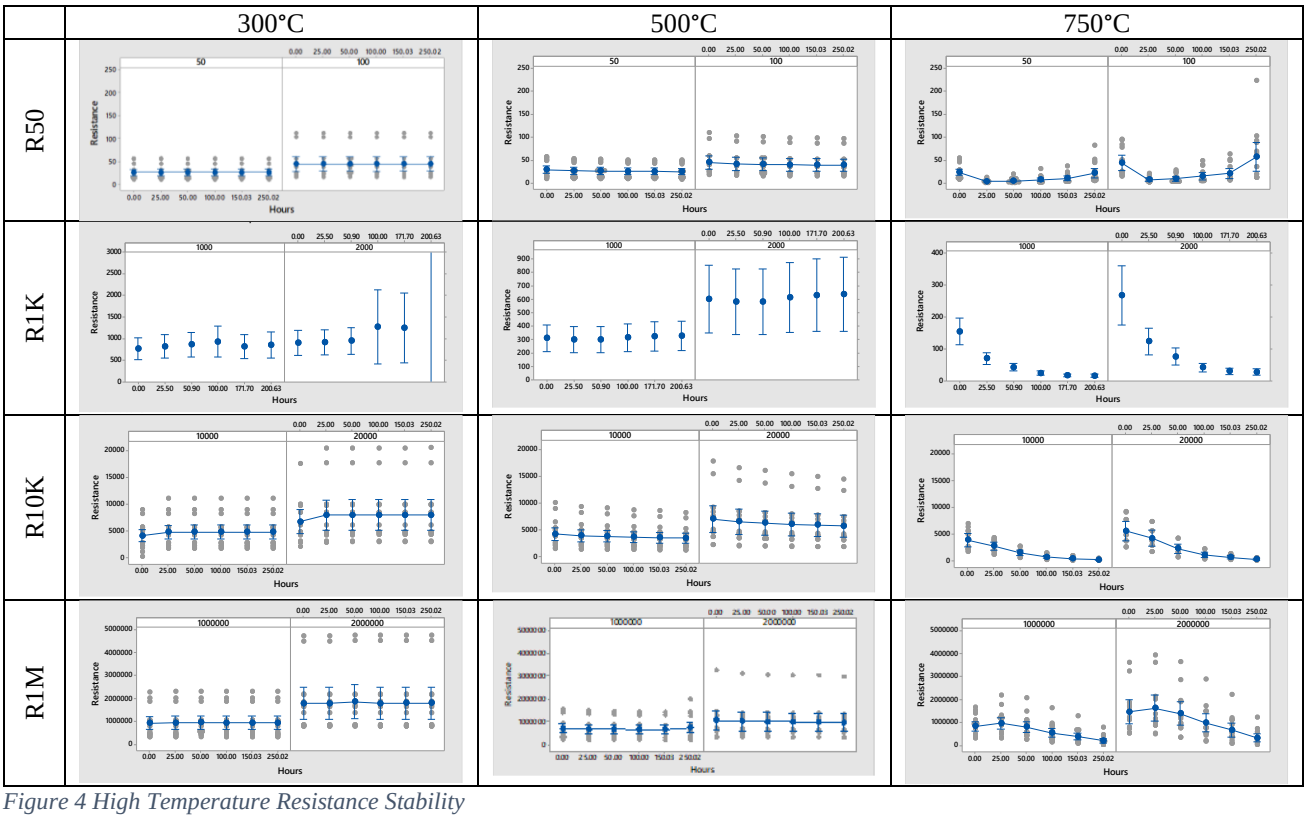


Figure 4 High Temperature Resistance Stability

An experiment with higher firing temperatures of 950°C and 1100°C did not change the trend at 750°C which indicates that the cause is not incomplete sintering. SEM inspection of microstructure analysis of sample cross sections taken from each test group is shown in Figure 5. The cross sections were taken after aging at 1000 hours at 750°C. A comparison of the microstructure of R50, R1K, R10K, and R1M after aging shows a difference in the microstructure that aligns with the resistance trend. The dense microstructure of R1K, R10K, and R1M contrasts with the porosity of R50. The dense microstructure correlates to the decrease in resistance observed in the samples of R1K, R10K, and R1M as they were aged for 1000 hours at 750°C. The increased porosity of R50 correlates to the observed increase in resistance when aged at 750°C.

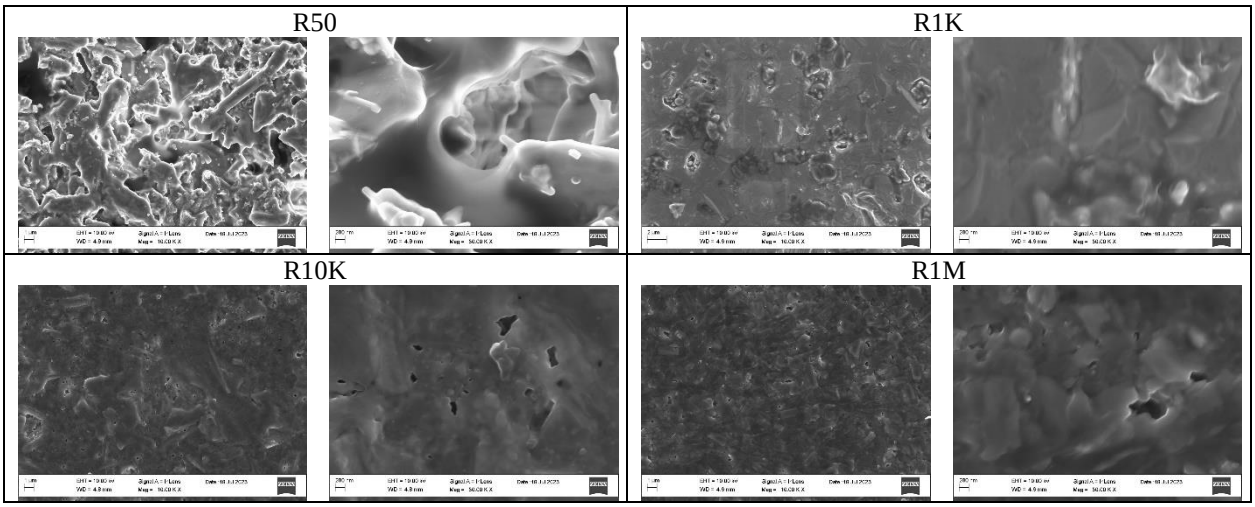


Figure 5 Comparison of the microstructure of R50, R1K, R10K, and R1M after 1000 hours aging at 750°C

Capacitor Printing and Testing

Direct write capacitors were fabricated with two designs, Metal-Insulator-Metal (MIM) and interdigitated capacitors (IDC) were fabricated. The designs were first modeled in HFSS to evaluate the needed geometry for a targeted capacitance. The capacitors were then printed and tested for high temperature stability.

Metal-Insulation-Metal (MIM) capacitors are made using layers of Au1-D1-Au1 materials printed with the Nordson EFD ProL dispense printer. The fabrication process is shown in Figure 6.

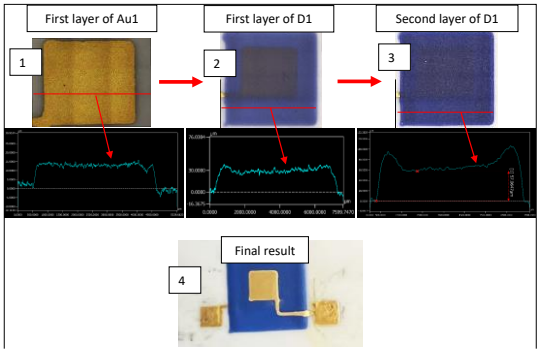


Figure 6 Fabrication process for MIM capacitor

Two layers of D1 dielectric are used to minimize the probability of pin holes. The capacitor shown is 2.47 mm x 2.51 mm with a capacitance of 9.22 pF. The sample was used to characterize capacitance and dielectric constant over frequency and temperature (Figure 7). The dielectric constant increases to 300°C, remains steady until 500°C when it increases at a more rapid rate.

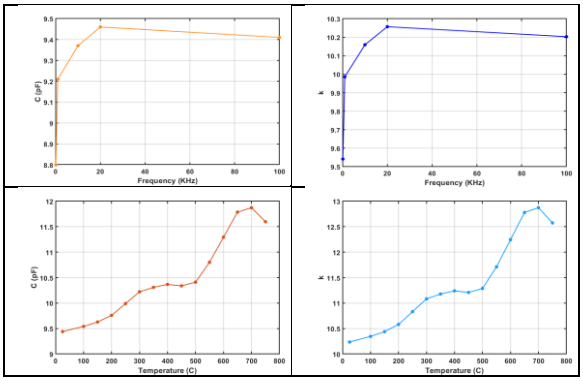


Figure 7 MIM capacitor and D1 dielectric constant over frequency and temperature

Leakage current was measured at 300°, 500°, and 750°C and shown in Figure 8. At room temperature, the leakage current was in the nanoamp (nA) range, it

increased to around 1.6 µA at 300°C and returned to the initial current after cooling down to room temperature. The current spiked to 18 µA and 40 µA, then it decreased at the stable temperature to around 1.4 µA and 5.3 µA at 500°C and 750°C, respectively. After cooling down to the room temperature, the current returned to its initial value after each condition. Leakage current increases with temperature due to the number of electrons with enough energy to migrate between metal plates of the capacitor at high temperatures. The spikes that happened once the temperature reached its peak is because as the temperature increases, the charge carriers begin to gather then sweep away to the electrical ground followed by the leakage current decrease.

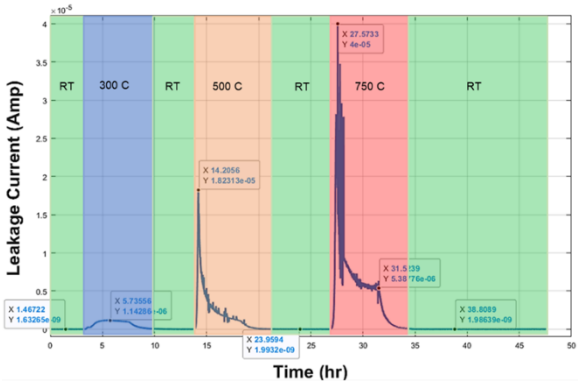


Figure 8 Leakage current across MIM capacitor

Another MIM capacitor was fabricated to target 100 pF at 100 MHz based on a HFSS simulation design. Simulation was made assuming the conductivity of the gold is the conductivity for bulk which is 4.1 x 10^7 S/m, the substrate is ceramic, and the dielectric insulation is D1 with dielectric constant of 10. The capacitor has a plate electrode of a size 7.1 mm x 7.1 mm and dielectric thickness of 50 µm. The simulation gave a capacitance of 99.26 pF at 100 MHz as shown in Figure 9.

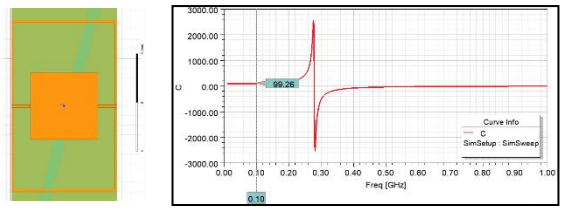


Figure 9 HFSS Simulation of MIM Capacitor

Two capacitors were fabricated, the capacitance of each one was measured with VNA machine at 100 MHz and found to be 82 pF and 101 pF for sample A and sample B, respectively. Figure 10 shows images of the capacitors with dimensions.

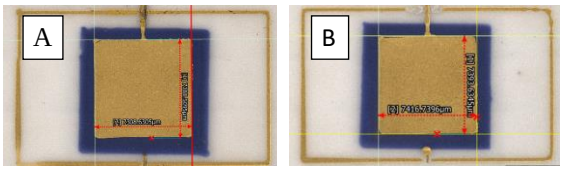


Figure 10: Two capacitors were fabricated and measured with VNA at 100 MHz. Capacitance was found to be A: 82 pF, and B: 101 pF.

Figure 11 shows the measurement of the capacitors with a Keithley 4200 SCS over frequency to 200 kHz and temperature up to 750°C. The capacitance is around 63 pF and 72 pF for samples A and B. The capacitance increases with temperature due to the increase in dielectric constant with temperature. The increase in capacitance is minimal up to 400-500°C and starts increasing above that at a faster rate.

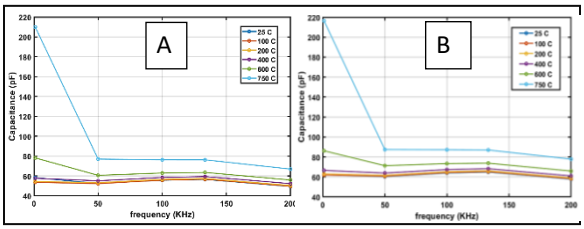


Figure 11: Capacitance over temperature and frequency for two MIM capacitors.

The MIM capacitors were aged at high temperatures; 300°C, 500°C, and 750°C, for 100 hours with the capacitance measured during the test at selected frequencies. The results are shown in Figure 12. Sample A was aged at 300°C for 100 hours, then cooled to the room temperature and was used for aging at 500°C for 100 hours. Sample B was used for aging at 750°C for 100 hours. The capacitance increased with temperature as predicted at all frequencies. The capacitance, at 200 KHz, increased 4%, 12%, and 34% at 300°C, 500°C, and at 750°C. The capacitance stabilized at the constant temperature for the entire aging periods and returned to the initial values when the temperature decreased to the room temperature.

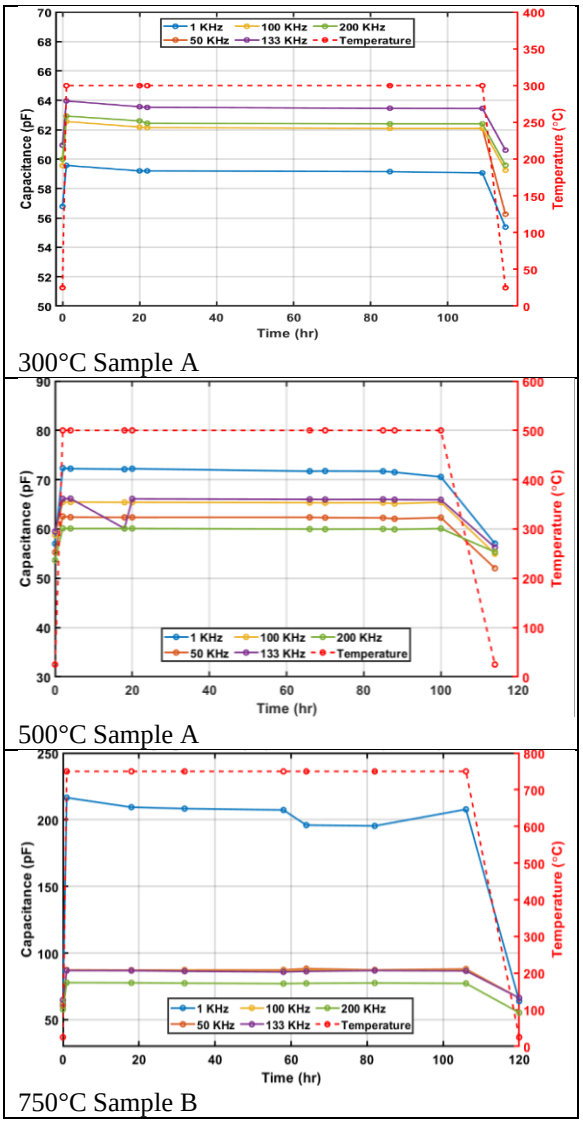


Figure 12 MIM Capacitor High Temperature Aging Results

Additional MIM capacitors were fabricated and thermal cycled at -40 to 300°C, RT to 500°C, and RT to 750°C. The results shown in Figure 13 before and after cycling. The capacitors survived thermal cycling and the capacitor variance was reduced in all cases.

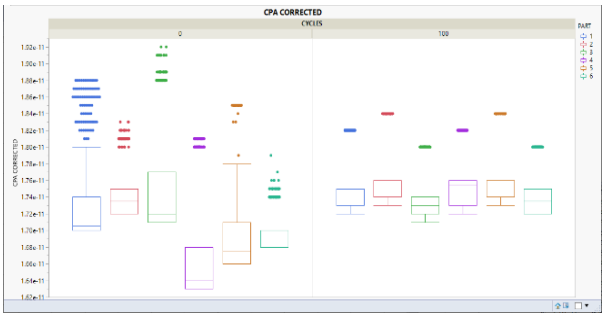


Figure 13 Thermal Cycling Results

Two of the thermal cycling samples were selected and measured before and after a 1000°C, 1 hour exposure. The results are shown in Figure 14. Sample 1 was selected after -40°C to 300°C and Sample 3 after RT to 500°C. Sample 1 reduced in capacitance about 1 pF but Sample 3 had a significant reduction. *Figure 15* provides the reason for the drop in Sample 3 capacitance. The connecting trace became courser and opened. This trace was 1 layer with a thickness of about 2 microns. The Sample 1 traces are thicker with a thickness of 6 microns. The high temperature can lead to Ostwald Ripening of the gold since it is close to its melting temperature. A thicker printed trace of 6 microns is needed to survive this test. This was applied to the printing requirements for other components to be exposed to 1000°C.

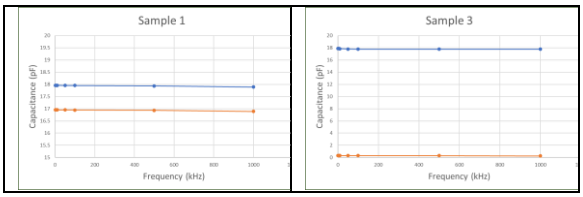


Figure 14 MIM Capacitors before (blue) and after (orange) exposure to 1000°C, 1 hour

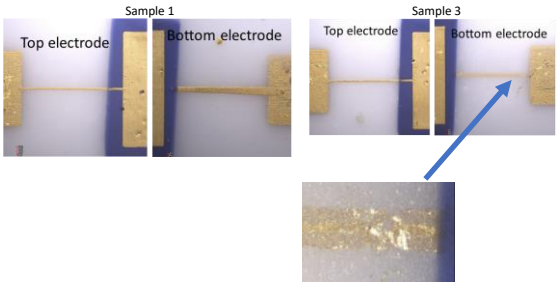


Figure 15 Inspection after 1000°C, 1 hour exposure

Interdigitated capacitors have a comb structure with opposing electrodes in plane with one another. The field lines are between, above and below the electrodes. Interdigital capacitors were simulated using HFSS with capacitances of 62 pF and 97 pF at 100 MHz. The capacitors were designed as gold printed on ceramic substrate and coated with D1 dielectric as shown in *Figure 16*.

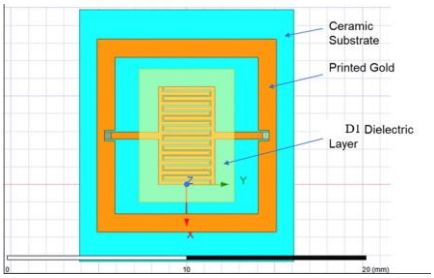


Figure 16: The design of Interdigital capacitor

The parameters of the simulation design for both capacitors are shown in *Table 2*.

Table 2: Simulation parameters for the interdigital capacitors

Parameter	Capacitor 1 (62 pF)	Capacitor 2 (97 pF)
Arm width	200 µm	200 µm
Arm length	3.1 mm	2.7 mm
Arm thickness	5 µm	5 µm
Arm spacing	120 µm	80 µm
Number of arms	20	20
Substrate thickness	1 mm	1 mm
Dielectric thickness	50 µm	50 µm

The interdigital capacitors were printed using AJP of a thickness between 5 µm and 7 µm, arm width of about 190 µm, arm length of about 2.8 mm for 97 pF design and 3.1 mm for 62 pF design, and about 85 µm and 125 µm spacing between arm for 97 pF and 62 pF designs, respectively. Two layers of D1 dielectric were printed using Nordson dispenser to prevent pin holes and to have a higher dielectric than air. *Figure 17* shows the fabricating process of the capacitors.

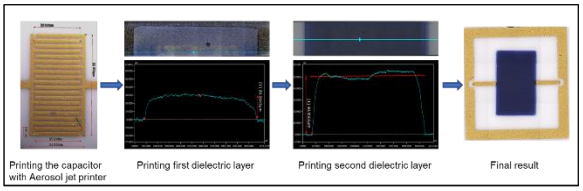


Figure 17: Fabrication process of the interdigital capacitors

After fabrication, the capacitors were measured at room temperature and 100 MHz using VNA machine and the results are shown in *Figure 18*. A large difference between the design and the actual measurements. The reason is that with the narrow gaps AJP overspray of Au1 causes shorting between the lines and reduces the effective capacitor area. Wider gaps would decrease capacitance.

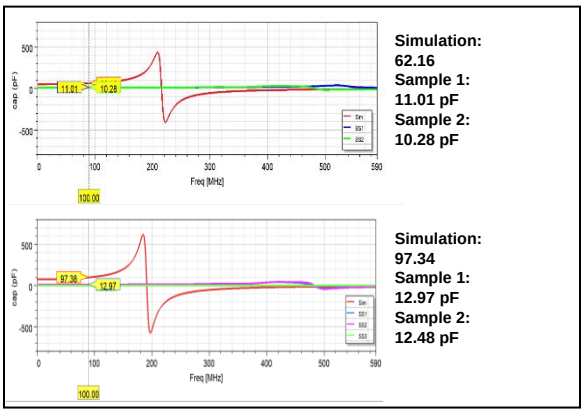


Figure 18 Measurements of the fabricated interdigital capacitors

Inductor Printing and Testing

Planar and freeform conical inductors were fabricated and tested. Figure 19 shows examples of these components. HFSS simulation of the inductors was made to determine the geometry needed for the targeted inductance and is shown in Figure 20.

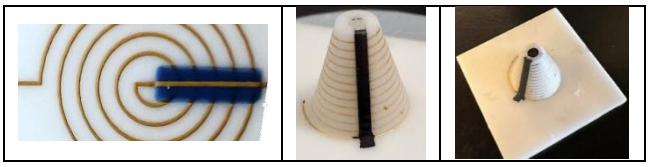


Figure 19 Pictures of Inductor Samples

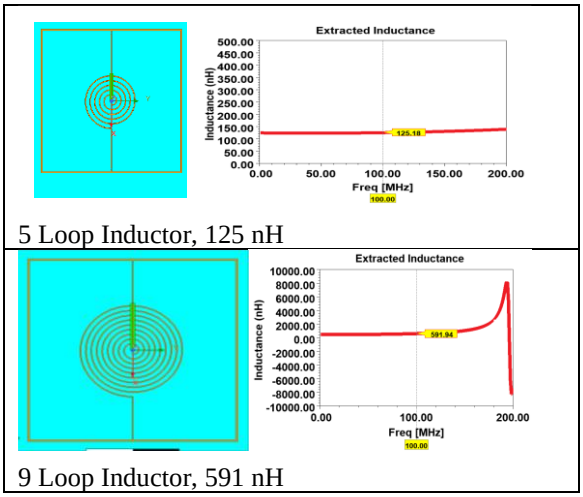


Figure 20 Ansys HFSS Design Simulations

One five-loop (125 nH) inductor and two nine-loop (591 nH) inductors were fabricated and tested. The designed planar inductors were printed on alumina

substrates. The printing process is shown in Figure 21 with the ground loop and the coil AeroJet printed first with gold (Au1) and fired. The second step is dispense printing a D1 dielectric layer to isolate the return line then dry and fire. The last step is to AJ print the return line using Au1 gold to connect the inner end of the loop, over the dielectric layer and connect to the ground loop. Measurements of the fabricated dimensions using the Keyence has the lines to be ~120µm with spacing of ~475 µm.

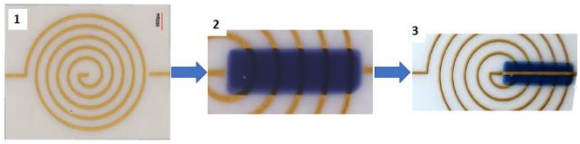


Figure 21 Fabrication of the AJ printed inductors

The fabricated inductors were measured for inductance at ambient conditions between 100kHz and 500MHz. An Inductance value of 135.4nH was measured at 100MHz for the 5 loop-inductors while values of 684.33nH, and 605.05nH were measured at 100MHz for the 2 samples of 9 loop-inductors. The actual fabricated dimensions were simulated with HFSS and the results were close to the results from fabrication as shown in Figure 22. There are slight deviations from the target inductances in the design and these deviations are attributed to the variations in the dimensions (lines and spacing) of the inductors.

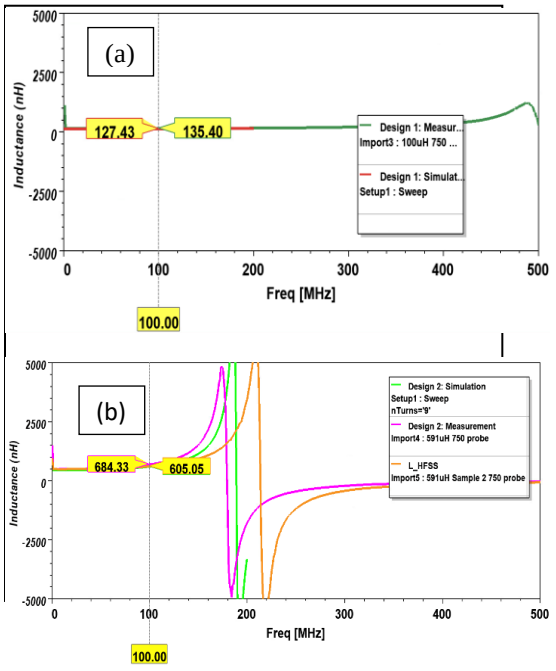


Figure 22 Inductance of measured samples and simulated prediction

A 9 loops planar inductor was aged at 300°C and the inductance was monitored and measured with LCR meter at frequencies up to 200KHz. Two layers of D1 pads were printed on top of the ground trace of the inductor, then Au1 traces with pads at the end were printed from the inductor leads passing on top of the D1 pads as shown in Figure 23. Finally, the gold pads were attached to wires using a high temperature capable silver adhesive.

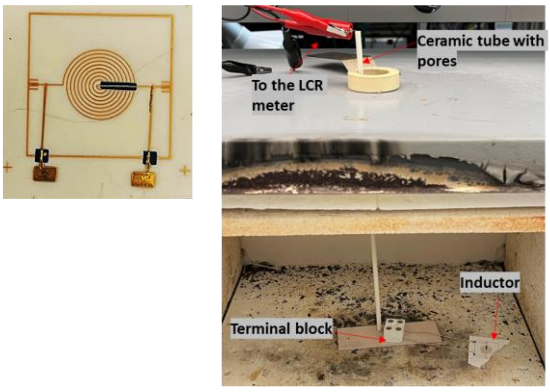


Figure 23 Planar inductor with additional gold pads for LCR measurements

The inductor was connected to the LCR meter and placed inside a box oven. Figure 24 shows the inductance behavior at 300°C and 500°C at 10kHz, 100kHz and 1MHz for 50 hours. Inductance increased with temperature at both frequencies. The inductance was lowest at 10kHz then increased at 100kHz and decreased at 1MHz at both temperatures. The inductance was moderately stable over the test time.

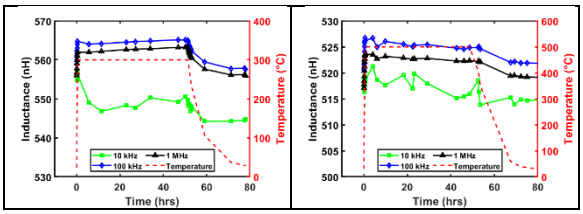


Figure 24: Inductance while aging at 300°C at 10kHz, 100KHz and 1MHz.

The 9-loop planar inductor was measured before and after each aging step using VNA machine (0.1 – 110 MHz). Inductance remained stable up to 60 MHz before and after both aging conditions and increased after aging at 300°C, especially at frequencies higher than 80 MHz. After aging at 500°C, inductance values were lower than the value after the previous ageing at 300°C as shown in Figure 25. At 100 MHz,

inductance values were 605 nH before aging, 1760 nH after aging at 300°C, and 835 nH after aging at 500°C.

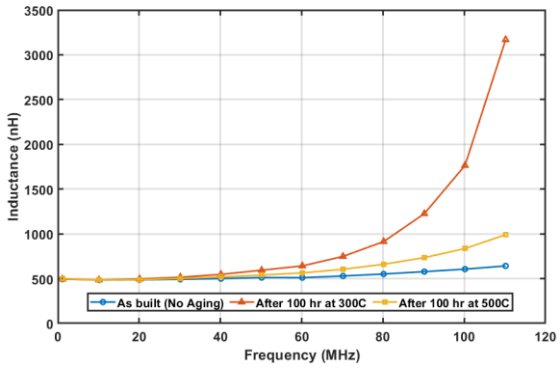


Figure 25: Inductance sweep between 100 kHz and 110MHz of a 9-loop inductor measured at room temperature.

9-loop planar spiral inductors were thermal cycled from -40°C to 300°C, room temperature to 500°C, and room temperature to 750°C for 100 cycles. Figure 27 presents the inductance and Q before and after thermal cycling at the three conditions. There was little difference found in the inductance and Q.

Planar spiral inductors were modeled in this period to evaluate the effect of using a thicker conductor needed for 1000°C exposure. The inductance measurements before and after this exposure is shown in Figure 26. The inductor was printed with 5 micron AJP Au1 to survive the temperature exposure. Little change in the inductance and Q was noted.

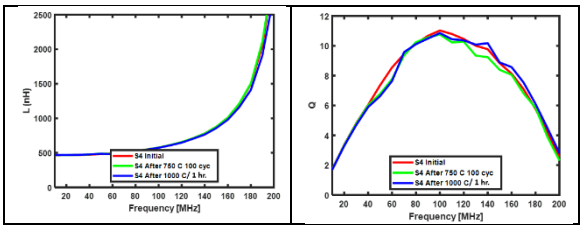


Figure 26 Planar spiral inductor after 1000°C, 1 hour exposure

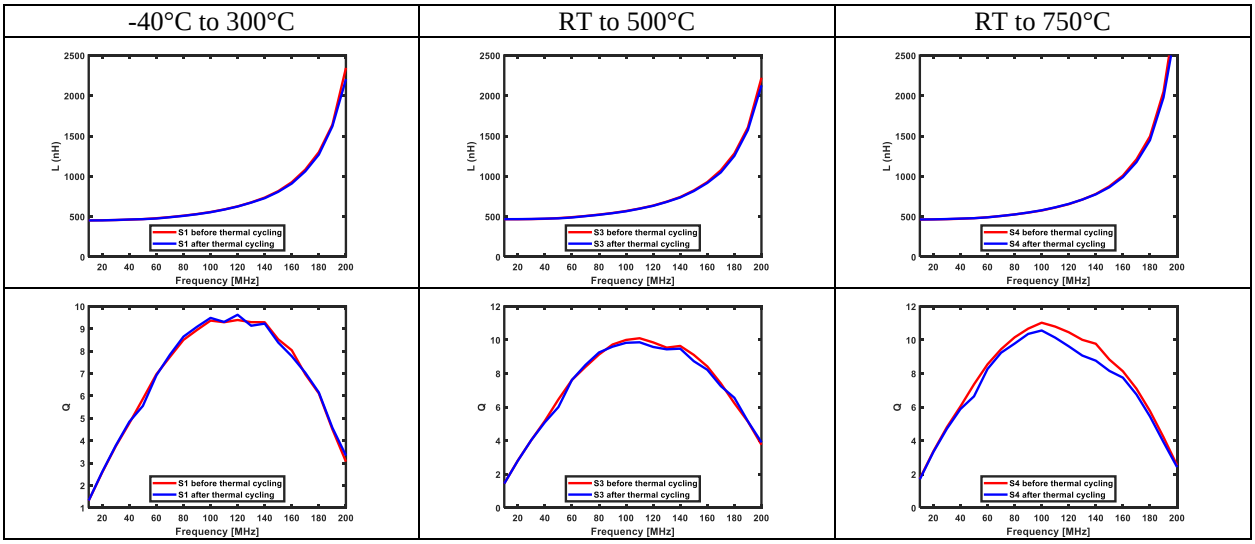


Figure 27 Planar spiral inductor thermal cycling results: inductance and Q

Conical spiral inductors were fabricated using the Lithoz printer with 350D alumina. The windings were AJ printed with diluted Au1 using the Optomec AJ 5X Printer. The inductors were simulated in HFSS with the number of windings and geometry to determine the inductance. The HFSS and MasterCAM simulations were used prior to fabrication to help determine the fabrication strategy. Simulations in Mastercam of the 5 axis printing process was used to first determine the proper inductor design, fixtures, and clearances. Parametric HFSS simulations were used to determine the electrical impact.

A 922 nH conical inductor HFSS design model was made with 5 mm radius base, 2 mm at top, 1 mm thick walls, 15.5 turns of spiral, 50 microns by 200 microns wire and shown in Figure 28. The substrate used is 1 mm thick alumina ceramic with a dielectric constant of 9.8. The model trace is Au1 with a conductivity of 4.1 x10E7 siemens/m. The trace is 10 um thick and 50 um wide. Spacing between traces is kept at 150 um. The overall size of the inductor is 5 mm x 5 mm. The cone has a base diameter of 10mm and top diameter of 4mm. Figure 29 shows the extracted inductance. The inductance value is 922 nH

at 100 MHz and is in the region before self-resonance.

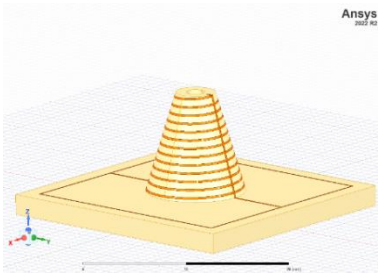


Figure 28 Conical Inductor Model

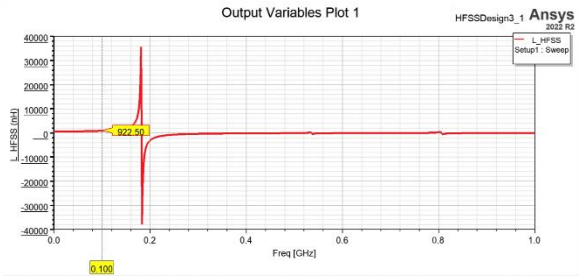


Figure 29 Extracted inductance

A Mastercam simulation of printing a conical inductor is shown in Figure 30. The inductor is mounted on the 5x AJP trunnion attached with a fixture with the central axis aligned to the trunnion rotating axis. Clearance between the shutter of the 5X AJP and the inductor base was not sufficient to avoid collision while rotating. The inductor was modified to raise its height from 10 mm to 12 mm and begin printing coils 2 to 5 mm higher as shown in Figure 31. HFSS simulation was made on 1000 nH, 500 nH and 100 nH cylindrical inductors designs with the added 2 mm clearance to determine any changes needed in the printed design.

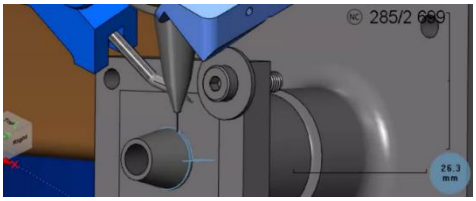


Figure 30 MasterCAM simulation of descrete conical inductor

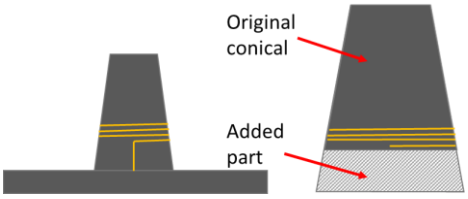


Figure 31 Clearance needed for spiral inductors

The conical inductor was measured for inductance and results are shown in Figure 32 at room temperature.

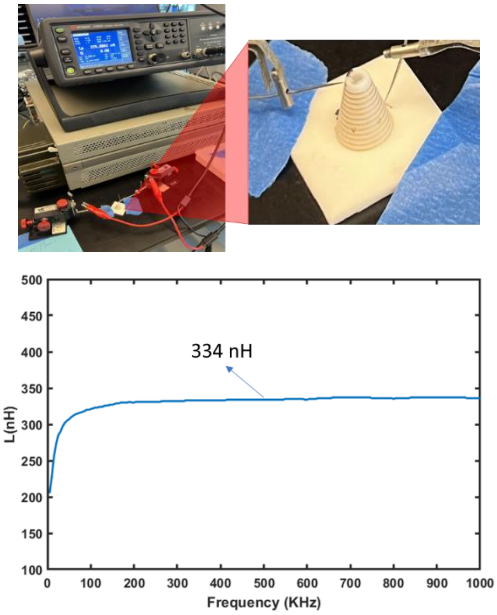


Figure 32 Conical Inductor Inductance

A high temperature ferrite was used to fabricate inductor with higher inductance by filling the cavity in the conical inductor. A lithium ferrite with an initial permeability of 54 and Curie temperature above 500°C was mixed with a high temperature binder and injected into the conical inductor core hole.

An HFSS simulation was made of the conical inductor with the ferrite core to understand its effect on inductance. The results of the simulation show (Figure 33) that adding the ferrite core lowers the inductor resonance frequency to within the targeted operating range (100MHz). Further simulations indicate that changing the core inner diameter and trace width the ferrite changes the resonance frequency very little but decreasing the wall thickness also decreases the resonant frequency.

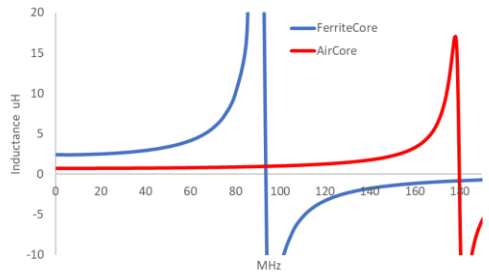


Figure 33 HFSS model results showing shift in resonance frequency

The conical inductor with the ferrite core was tested by measuring the inductance from room temperature to 620°C at GE Research on a probe station with a 620°C hot chuck shown in Figure 34. The inductor was measured from 100 Hz to 110 MHz using an Agilent 4294A Impedance Analyzer connected to the inductor using high temperature test probes. The results are shown in Figure 35 along with the measurement taken before application of the ferrite. Ferrite increases inductance about 3.1x (air core = 334nH, ferrite = 1.05 uH). The inductance decreases with increased temperature and the ferrite lowers the resonance frequency from the air core inductor that was found in the HFSS simulation. The resonance frequency was measured lower (4 to 5 MHz) than the simulation model results (10 MHz).

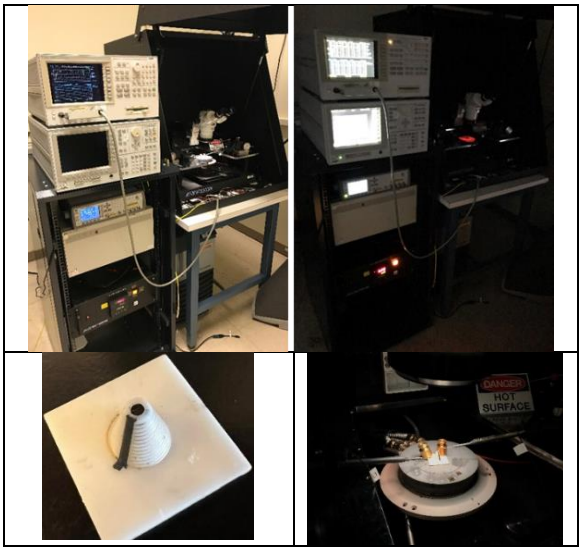


Figure 34 GE Research Probe Station with 620°C Hot Stage

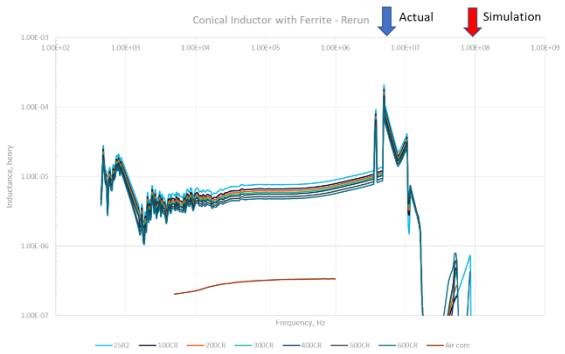


Figure 35 Measurement of Conical Inductor with Ferrite Core from 25°C to 600°C.

Acknowledgment

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