Advanced substrate metallization in the Era of AI and HPC

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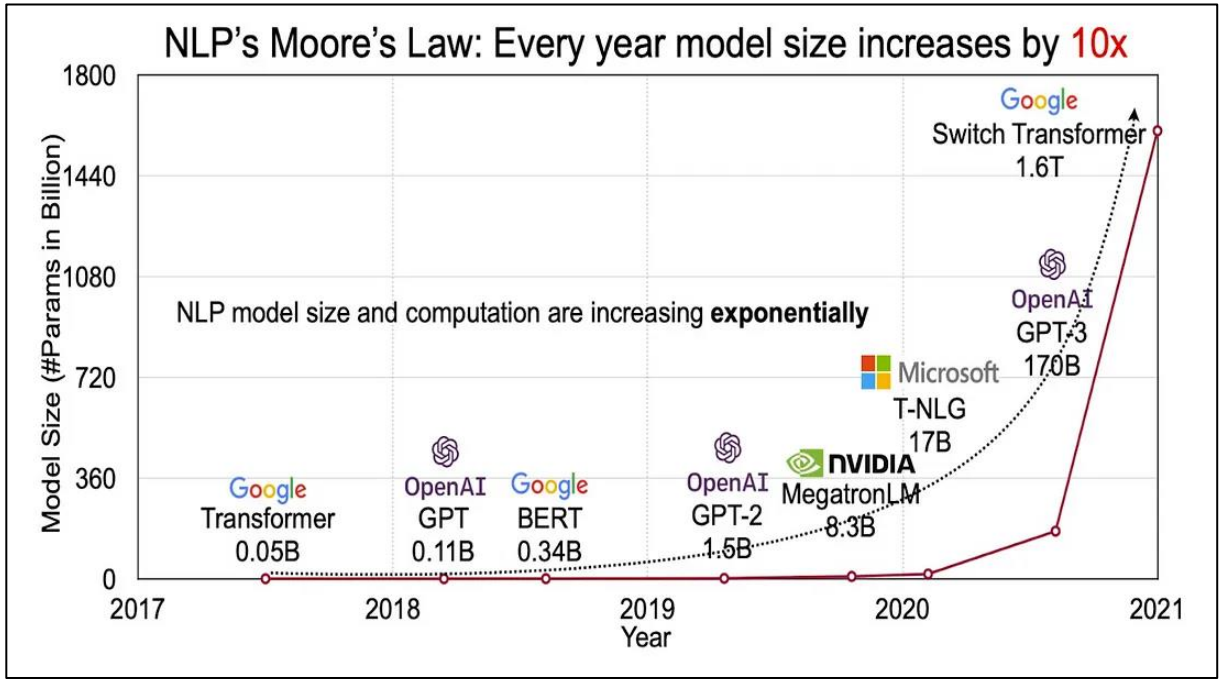
R&D Business Partner – IC substrate

MacDermid Alpha ELECTRONICS SOLUTIONS

Scaling New Heights: The Exponential Growth of AI Models



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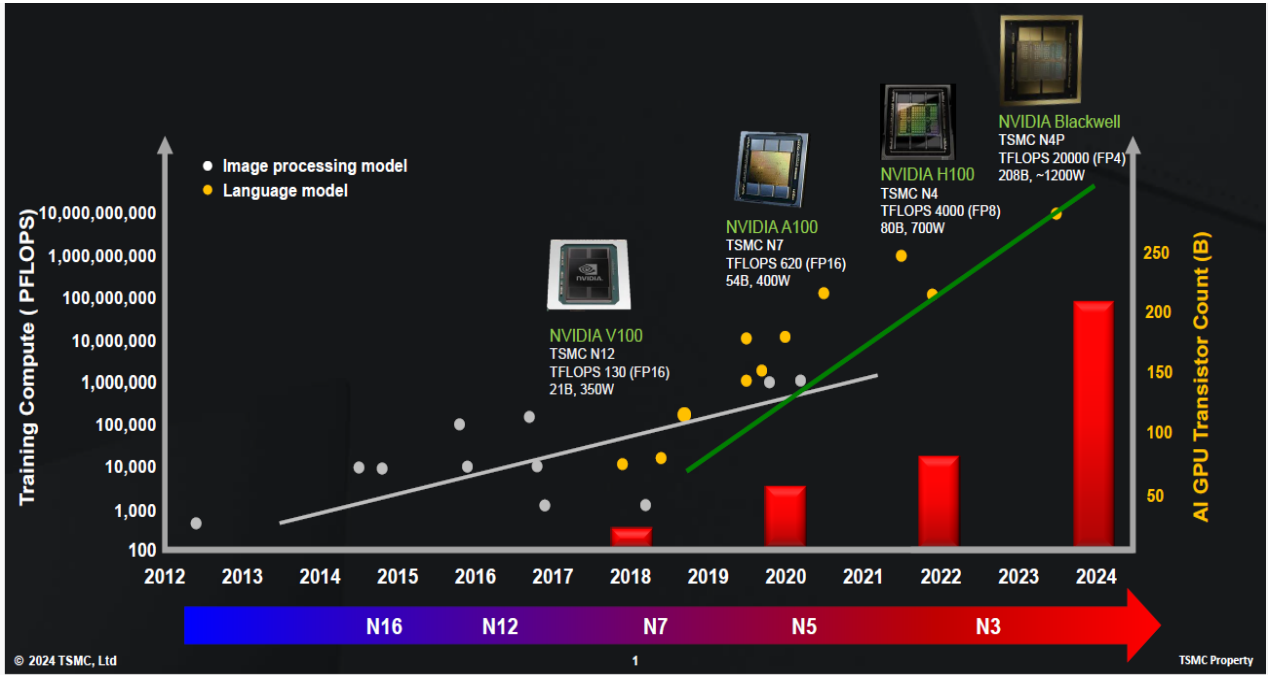


TSMC

- AI model size **growing exponentially**
- Need hardware to support the **computing needs**
  - Low energy consumption, latency, cost, yield

Advanced packaging for AI and HPC

- Trend toward **higher-density** packaging
- **technology migration** to advanced technology
- Shrinking **I/O** pitches
- **Multi-component modules**
- System **integration, 3D stacking**

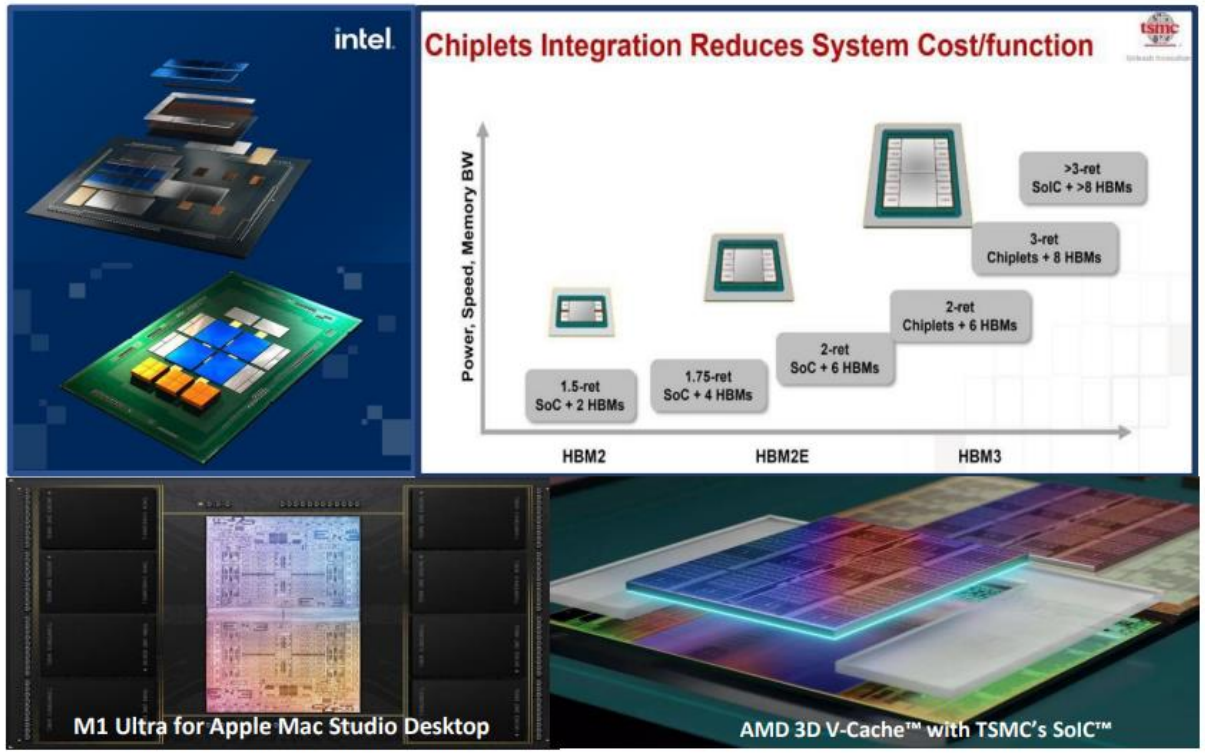
$Bn	2023	2024F	2025F	2028F	2024F/2023	2025F/2024F	2023-2028
Leadframe	$14.4	$12.9	$13.1	$15.1	-10.0%	1.2%	1.0%
WB BGA/CSP	$6.0	$6.3	$6.4	$6.7	4.2%	1.6%	2.3%
Stacked CSP	$6.0	$6.5	$6.7	$8.9	7.0%	3.5%	8.0%
WB SiP	$1.7	$1.7	$1.8	$2.0	4.1%	1.8%	4.1%
Flip Chip SiP	$4.0	$4.1	$4.3	$6.1	3.4%	3.1%	8.9%
FCCSP	$5.9	$6.5	$6.8	$8.4	10.3%	4.2%	7.3%
3D Stacking HBM	$0.4	$1.1	$2.2	$6.1	190.4%	110.6%	75.9%
FCCSP/DRAM	$1.5	$1.9	$2.1	$2.4	29.4%	5.8%	9.6%
FCBGA[1]	$9.0	$7.5	$7.6	$10.4	-16.8%	2.0%	2.8%
WLCSP	$5.2	$5.0	$4.9	$7.1	-4.5%	-1.3%	6.5%
FO-WLP/PLP[2]	$1.1	$1.1	$1.2	$1.4	3.6%	8.6%	5.1%
HD-FO / CoWoS/CoWoS-like[3]	$1.6	$4.1	$6.6	$9.8	152.3%	60.2%	43.7%
COF/COG	$2.6	$2.4	$2.4	$2.8	-6.4%	0.4%	1.8%
Total[4]	**$59.3**	**$61.1**	**$66.0**	**$87.2**	**3.0%**	**8.0%**	**8.0%**

Prismark Partners

- Technology is moving towards advanced IC substrates and high-density interconnects, to support the exponential growth in AI model sizes

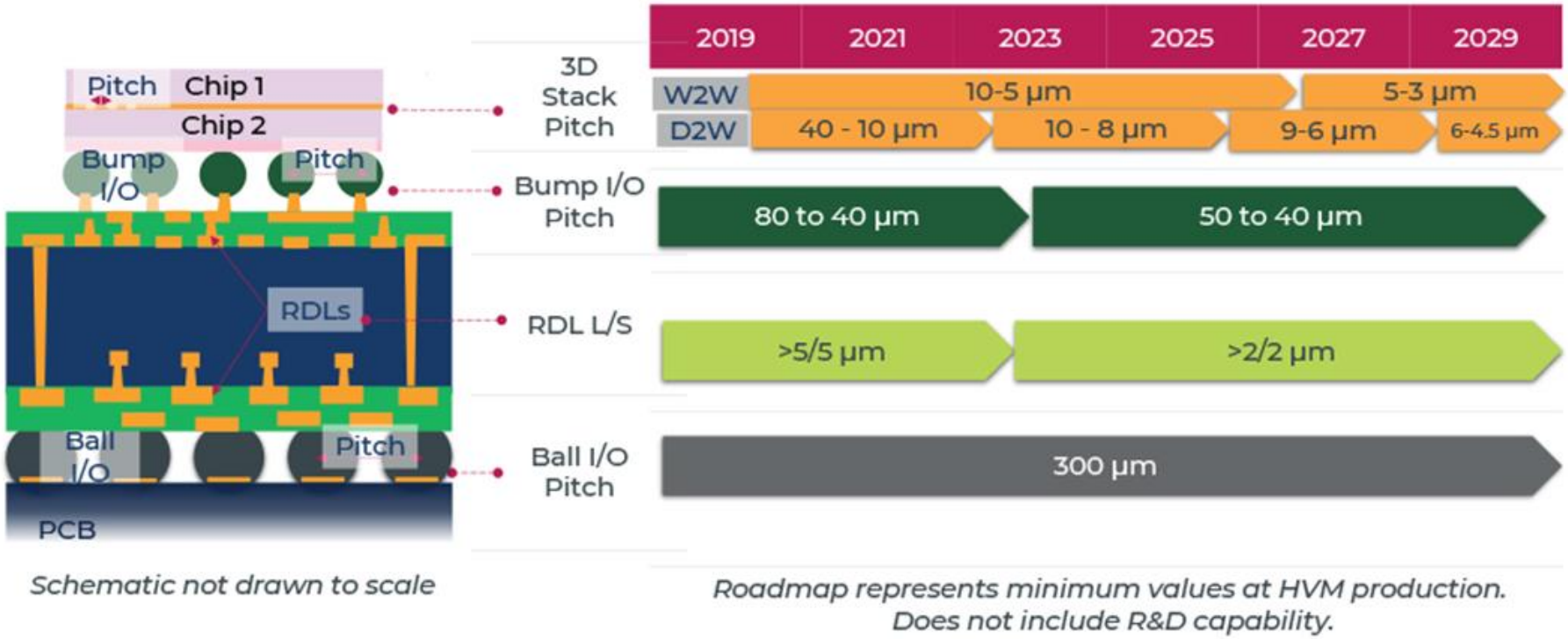
Advanced IC Substrates packaging

- **Advantages**
  - Enhanced **power and signal performance** and miniaturization.
- **Challenges**
  - Manufacturing **complexity, low yield, and cost.**
  - **Thermal** management issues.



: Prismark Partners

Advanced packaging roadmap



Yole Intelligence

- **Bump I/O** pitch is scaling faster than **Ball I/O** which drives a finer RDL L/S at ICS package level
- Innovative NPD is essential to fill the gap and enable RDL metallization

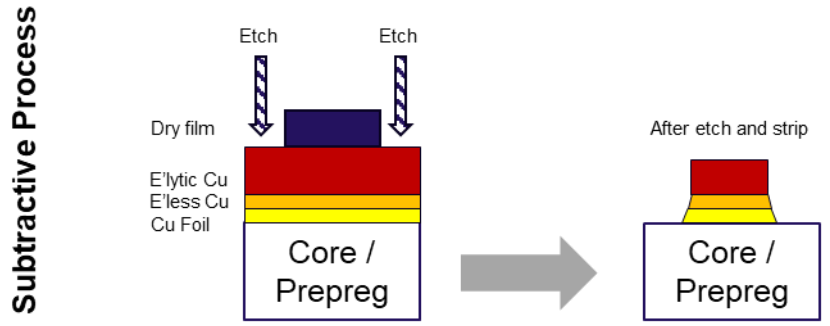
Advanced Patterning Technologies for IC Substrates

- **Subtractive Process:**

  Cost: **Lower cost** due to the simpler process.

  Challenges: Difficult to **etch through thick electrolytic copper layers,** to achieve fine features.

  Usage: **Less complex designs** with larger features.



- **Modified Semi Additive Process (MSAP):**

  Method: Plate only interconnects

  Advantages: **Achieve finer features while using some etching**.

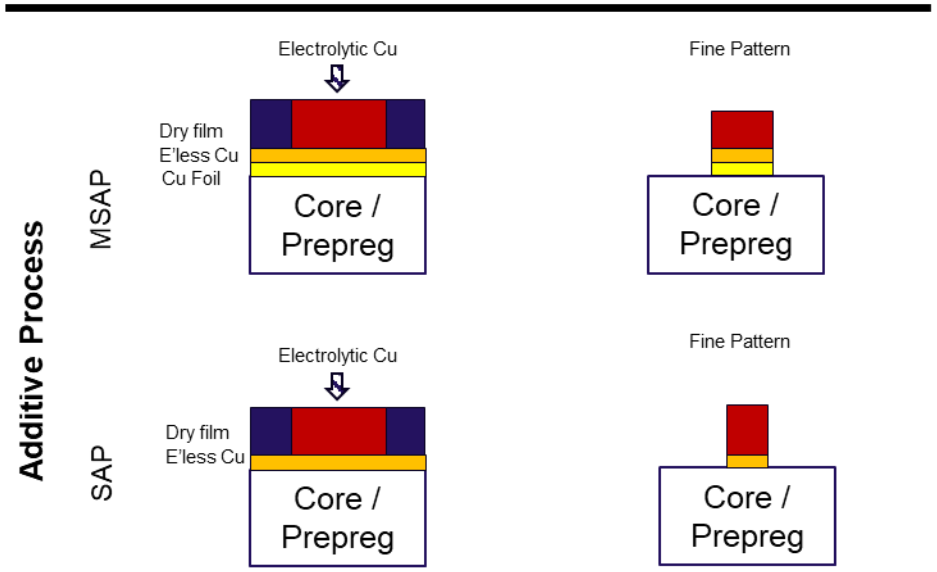
  Applications: **Moderate to fine features.**

- **Semi Additive Process (SAP):**

  Method: flip chip substrates with ABF layers. No copper foil, **allows finer feature resolution.**

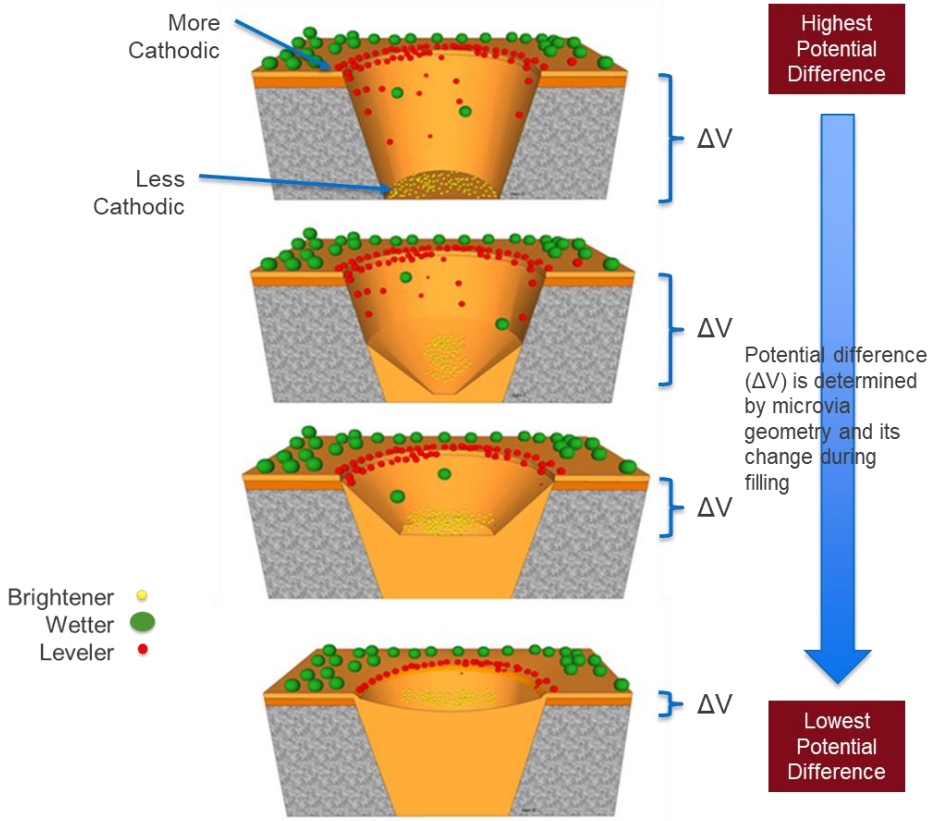
  Advantages: Achieves the **finest features among these processes**

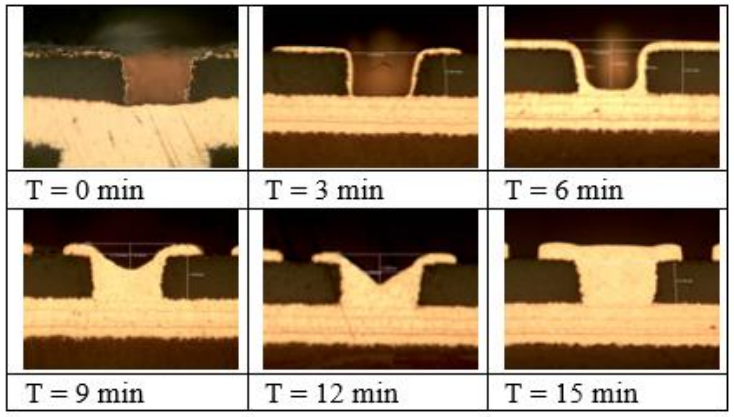
  Applications: High-density designs and **advanced packaging.**



Deposition Mechanism

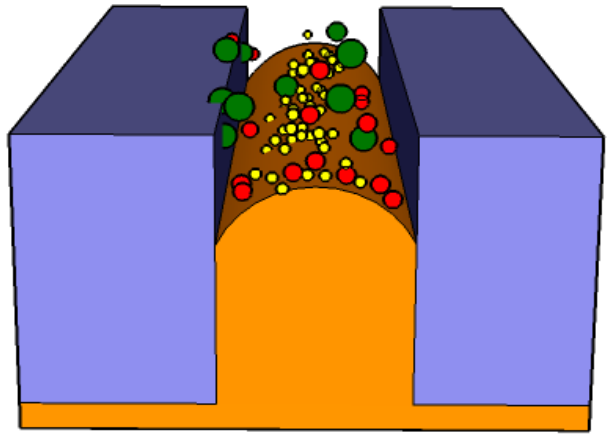
- **Bath composition**
  - **H_2SO_4** - Conductivity
  - **$CuSO_4$** - Cu source
  - **Chloride** - **anchor** sites to Suppressor
- **Organic additives**
  - Suppressor **adsorbed** on the surface
  - Brightener **diffuses** to bottom of the microvia
  - Leveler **selectively** adsorbs on the high current areas
- **Fill progression**
  - Plating at via bottom is fastest at the beginning
  - As plating proceeds, the potential differences and plating rate difference of surface and microvia lessen
  - Once filled, all plating rates are similar



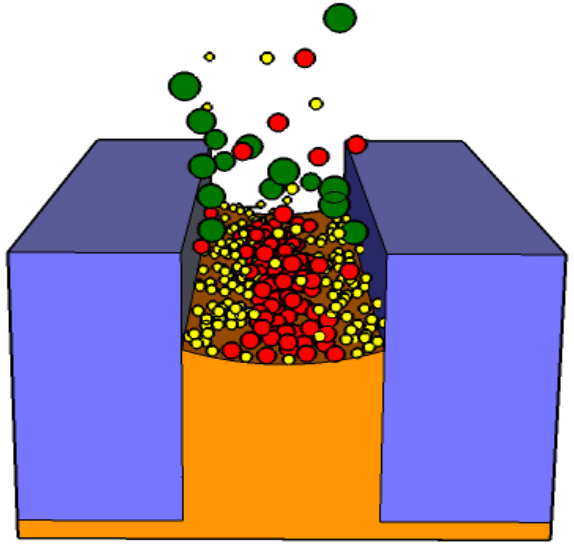


Innovative Additive Design

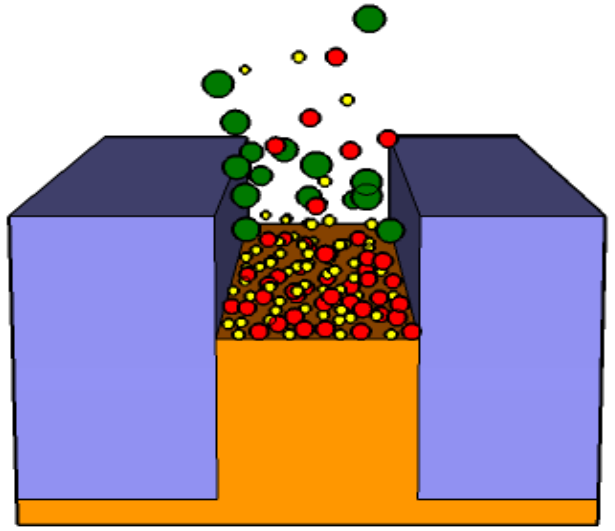
- Molecules with **certain functional groups** can be used to obtain **desired outcome**
- Innovative R&D approaches can **fine tune plating performance** to yield any **shape** depending on the additive and the conditions used



- Interact less with the current
- Lower diffusion speed



- Interact more with the current
- Higher diffusion speed

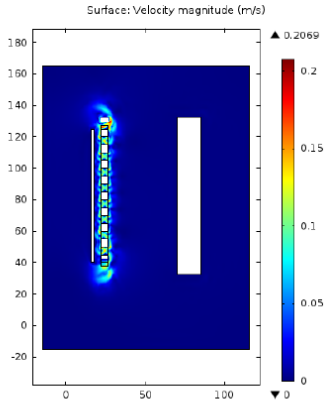


- Distributes uniformly on the surface
- Interact with the Br to create even layer

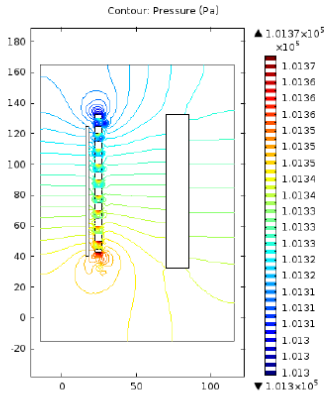
Plating Tools for Advanced Packaging

- Electrodeposition using **advanced L/S** requires **synergy** between **equipment** and **additives** for optimal performance.
- Modern tools **utilize unique mass transfer** methods as opposed to conventional VCP systems

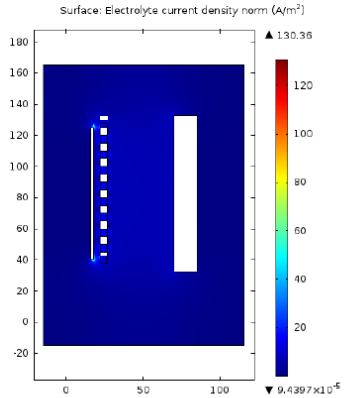
Flow velocity



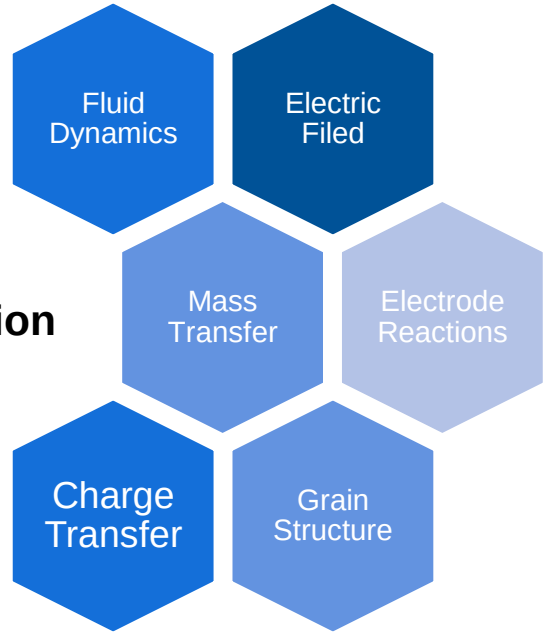
Pressure



Current density



Electrodeposition



- Better **understanding of tools and additives** leads to more **robust formulations**

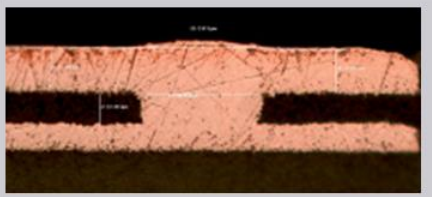
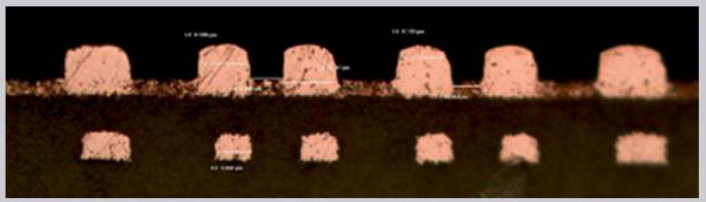
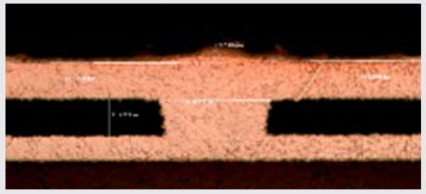
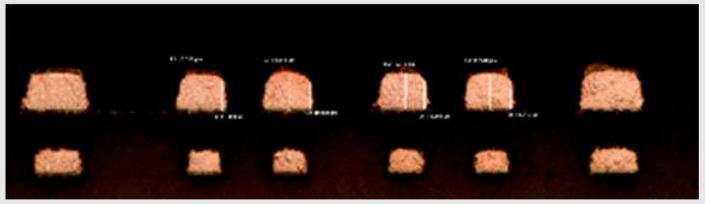
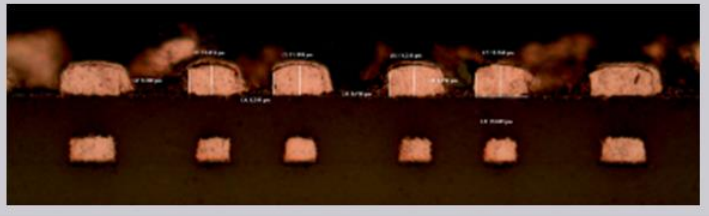
Process Parameters

Parameters	Systek UVF	
	Range	Optimum
Wetter	15 - 30 mL/L	10 mL/L
Brightener	0.5 - 2.5 mL/L	2 mL/L
Leveler	12 - 15 mL/L	5 mL/L
Copper Sulfate ($CuSO_4$.**5** H_2O)	180 - 250 g/L	200 g/L
Sulfuric Acid	40 - 60 g/L	50g/L
Chloride Ion (Cl^-)	40 - 60 ppm	50 ppm

- Plating was carried out in two settings
  - VCP style tool and ASM P500 High speed plating tool

Systek UVF Performance

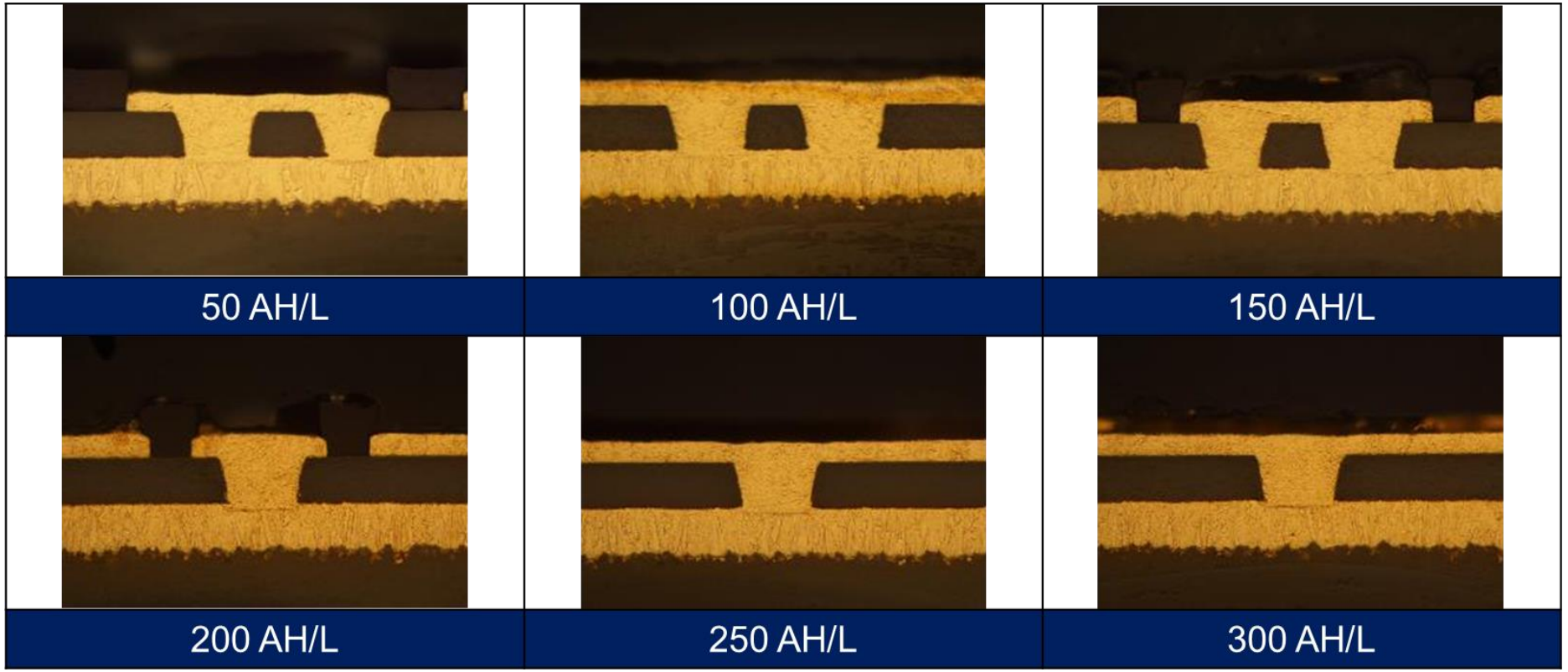
VCP type plating tool - 15 min. plating cycle

VMS	Dimple (µm)	Via image	R value (µm)	Line area image
220/60/50	-2.15		2.4	
200/70/50	-1.2		0.88	
200/100/50	0.23		0.20	

- Higher copper sulfate concentration increases via fill efficiency
- Lower copper sulfate and higher sulfuric acid reduce R-value

Aging Study X-Sections

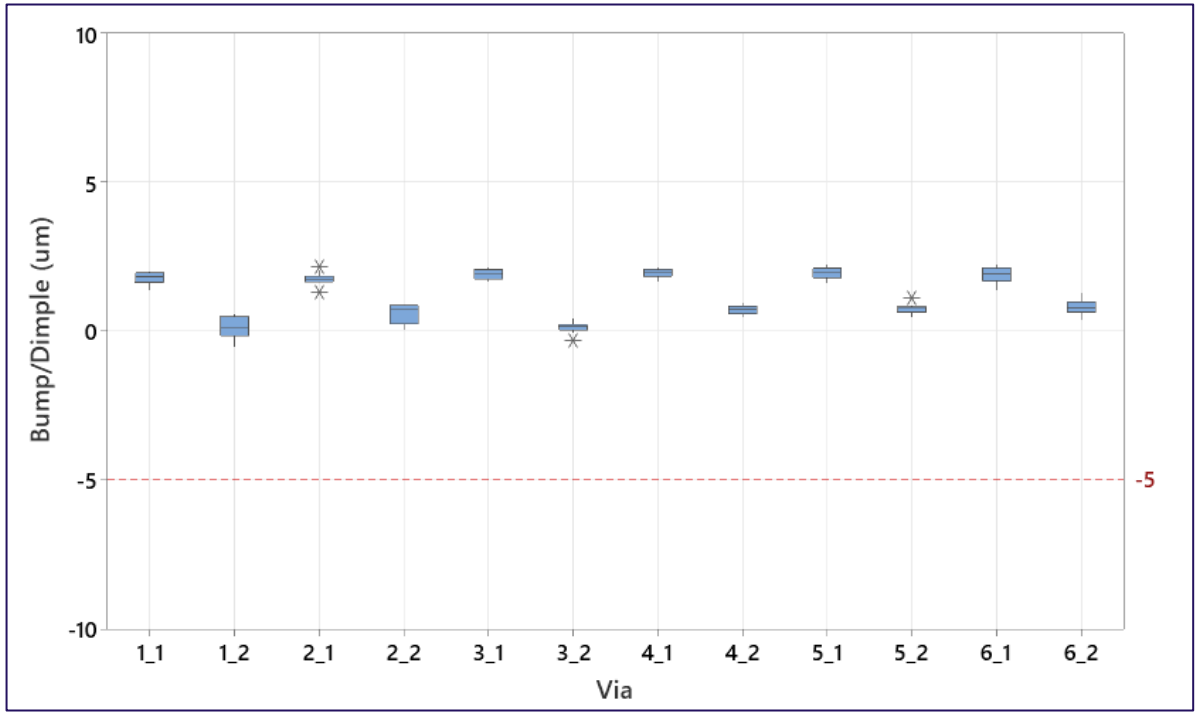
VCP type plating tool - 15 min. plating cycle

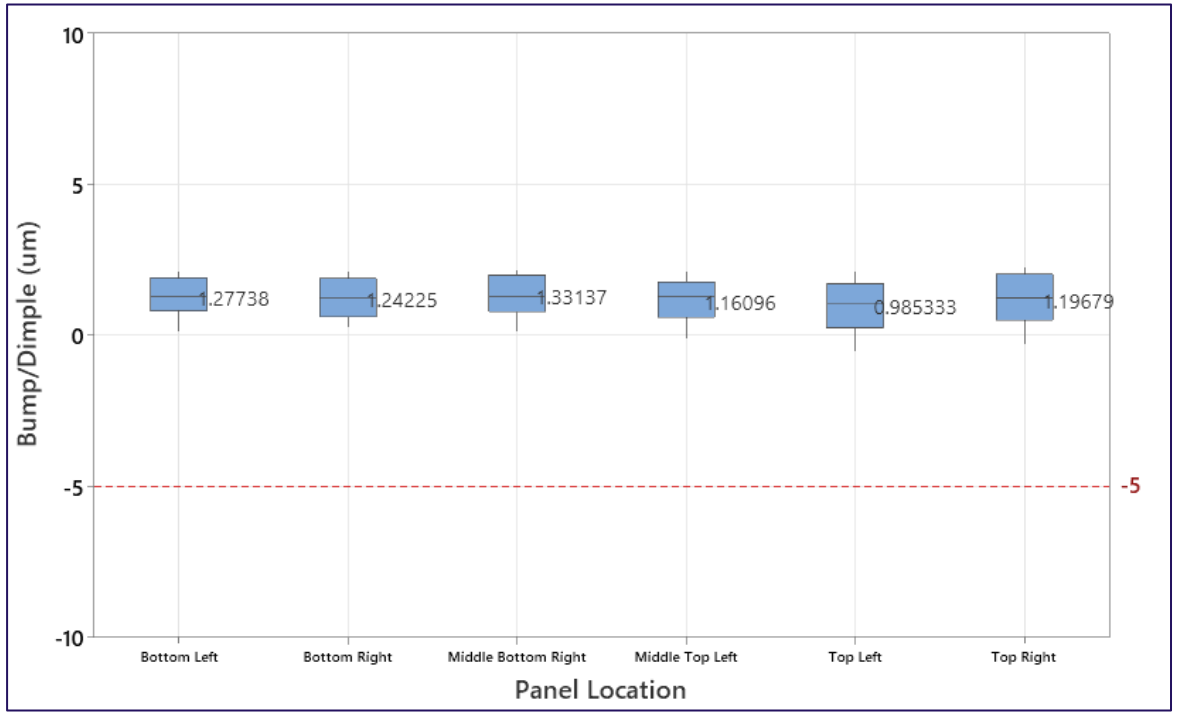


- Consistent via fill up to 300 Ah/L
- Defect free, flat to slight bump

Systek UVF Performance

ASM Nexx HSP tool – full panel plating 510x510mm





- Via size 65X40 µm , Overburden 18 µm, plating time 20-23 min
- All vias filled flat, No cavities,

Physical Properties – Tensile and Elongation

0Ah/L

	Break Force [lbf]	Elongation [%]	Tensile Strength [PSI]	Thickness [Mil]
1	70.63	19.48	42671.46	3.5
2	68.47	18.97	41860.52	3.46
3	61.90	20.30	41211.44	3.18
4	61.40	19.72	41626.67	3.12
5	61.56	23.40	41961.06	3.11
6	60.51	22.80	41517.20	3.09
Mean	63.06	**20.92**	**42582.07**	**3.14**

150Ah/L

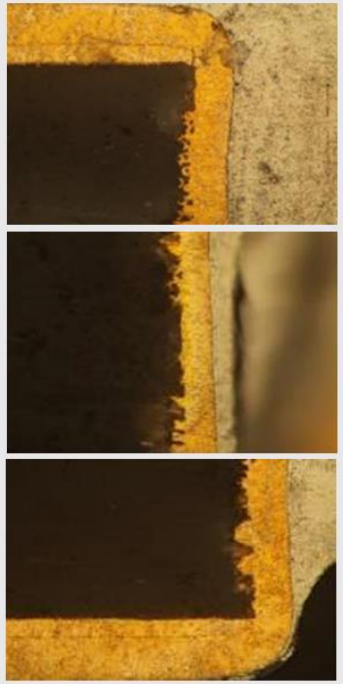
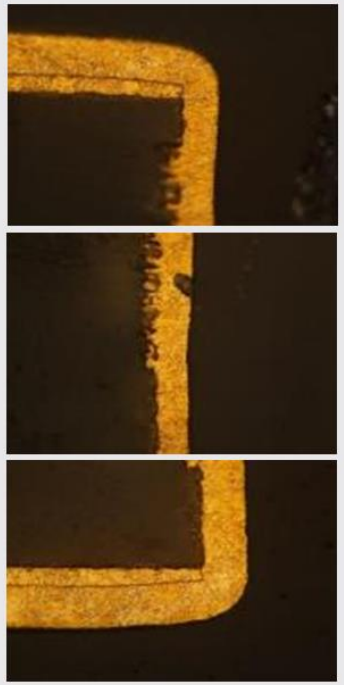
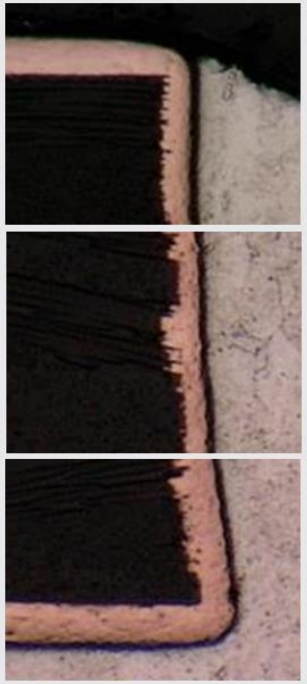
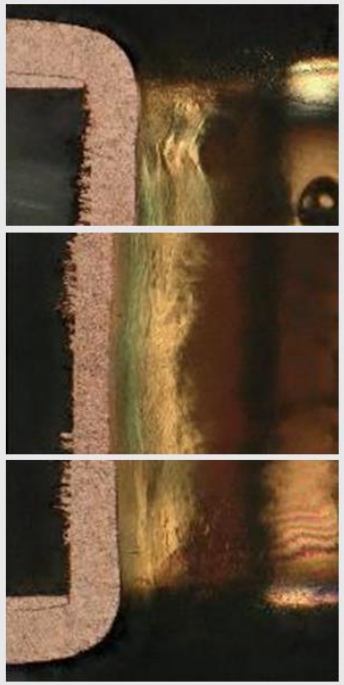
	Break Force [lbf]	Elongation [%]	Tensile Strength [psi]	Thickness Mils
1	77.93	27.77	44281.50	3.73
2	58.46	23.44	41420.72	2.99
3	55.77	18.36	40018.00	2.95
4	53.96	21.23	39628.57	2.88
5	52.95	20.56	39385.47	2.85
6	56.07	26.30	43068.00	2.76
7	49.46	24.84	38857.26	2.69
8	51.31	24.86	42690.83	2.54
Mean	56.99	**23.42**	**41168.79**	**2.92**

- Tested according to IPC-TM-650
- Stable performance and pass IPC Class III

Plating Condition	2.0 ASD	4.5 ASD
Elongation (%)	22.0	20.1
Tensile Strength (PSI)	40400	40000
Internal Tensile Stress (kg/mm^2)	0.87	0.85

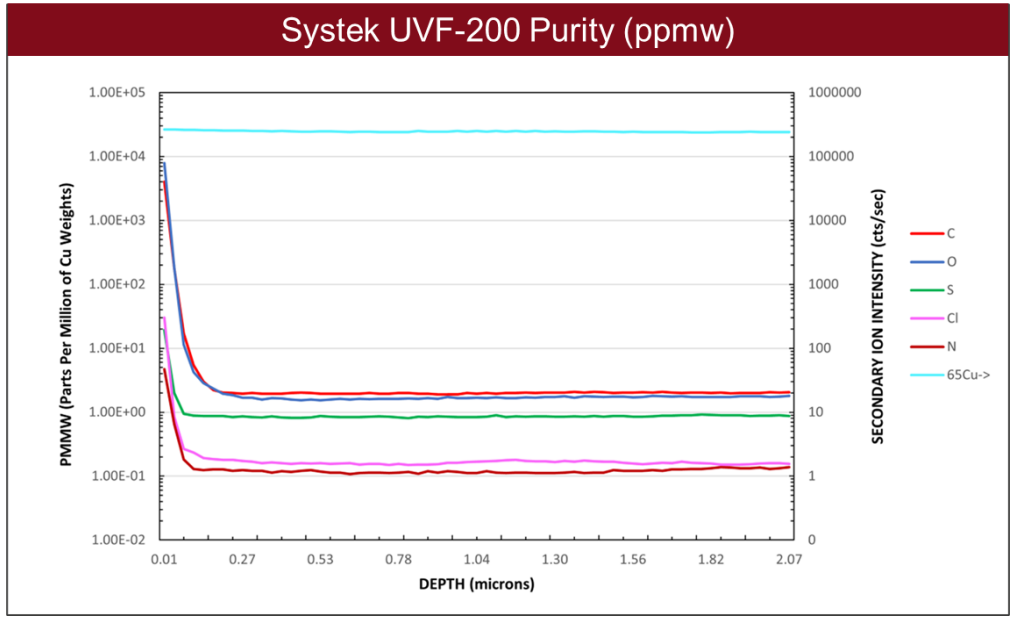
- Physical properties are consistent after plating at various conditions
- Low Internal Stress

6x Solder shock and 10x IR Reflow

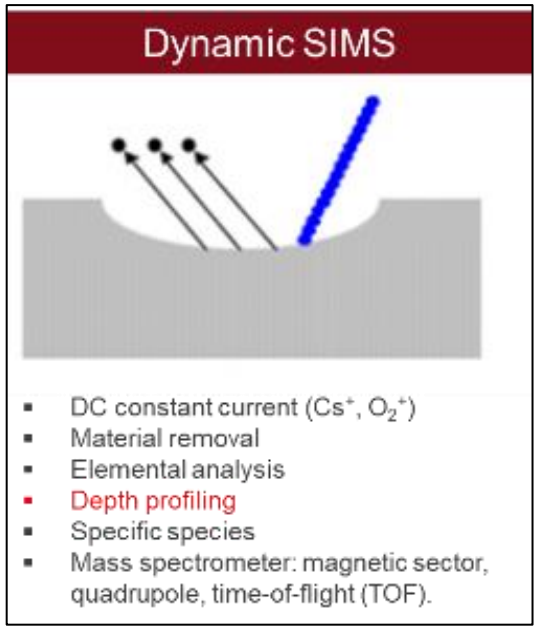
150 AH/L		300 AH/L	
6x solder shock	10x IR Reflow	6x solder shock	10x IR Reflow
			
No cracks	No cracks	No cracks	No cracks

- No cracks or hall wall pull away during thermal reliability testing

Deposit Purity - SIMS Analysis

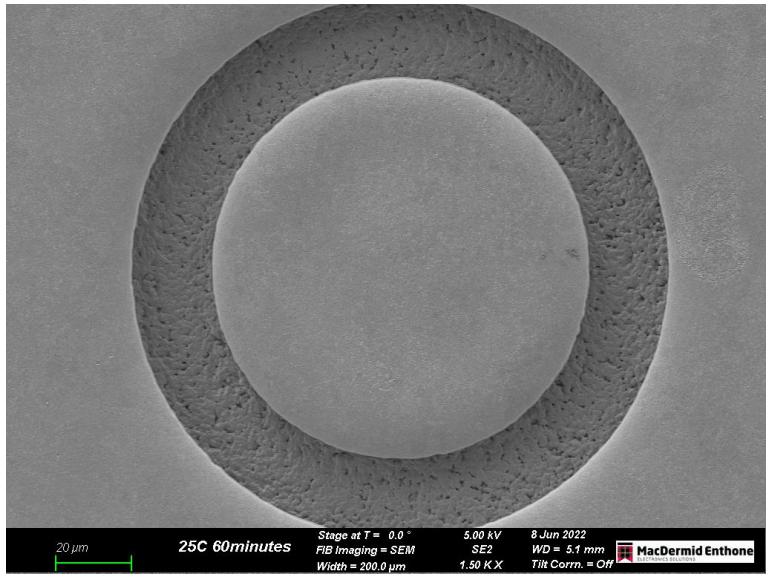


Element	Concentration (ppmw)
Sulfur	0.848
Carbon	1.98
Oxygen	1.66
Chlorine	0.163
Nitrogen	0.114



- Low impurities co deposit with Cu
  - Electrical conductivity, grain structure, Cu reduction during SAP / mSAP, physical properties

Grain structure evaluation



- Deposit had equiaxial grain structure
- Grain structure was consistent under different plating conditions

Conclusion

- **Excellent via fill** capability and **uniformity** in Electroplating for IC Substrates.
- **Tensile strength and elongation** meet IPC Class III standards and showed **low internal stress.**
- **All the additives can be analyzed by CVS**, ensuring defect-free bottom-up fill and stable performance over time.
- The process is **compatible** with cationic **membranes**, further enhancing reliability and application flexibility.
- **Enable higher density connectivity, miniaturization, and performance improvements.**

Contact us

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