

# Electrochemical Plating of Metastable Fine Grain Cu for Cu-Cu Hybrid Bonding Applications

Presented by Thomas Richardson  
on behalf of Pingping Ye

March 5<sup>th</sup>, 2025

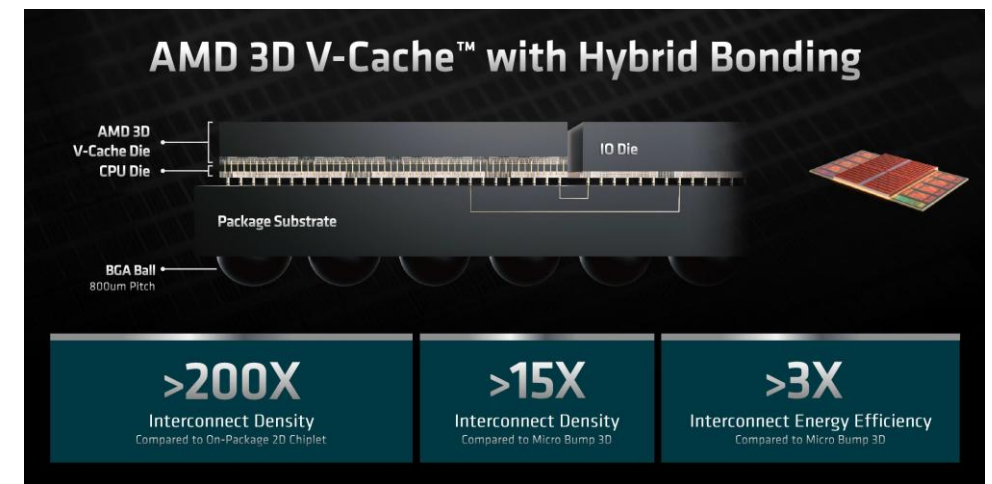
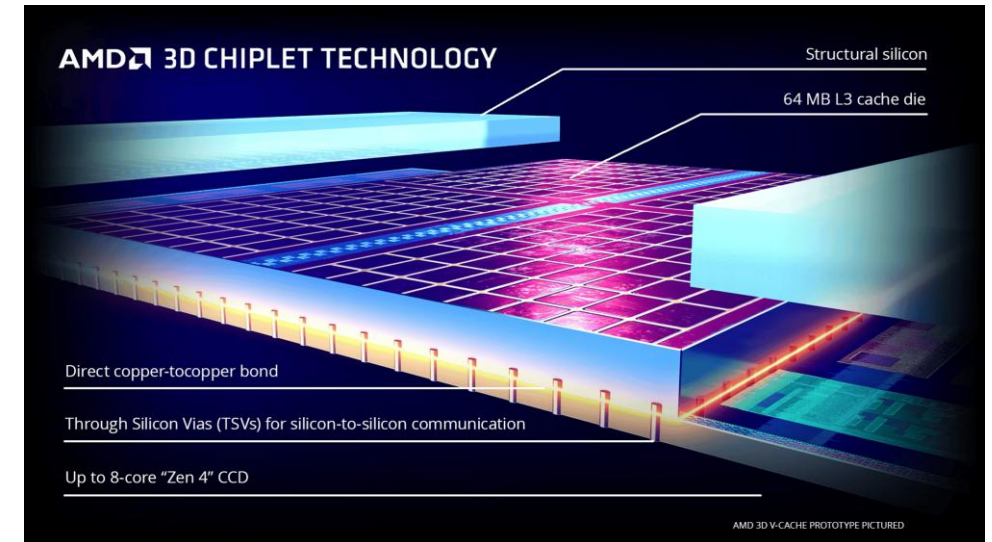
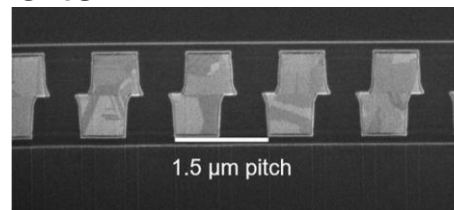


# Outline

- Introduction
- Screening of metastable fine grain on blanket wafer
  - XRD
  - Sheet resistance
- Cu grain evolution of self-annealing
  - Disparity of Cu grain evolution on blanket vs. patterned wafer
  - Disparity of Cu grain evolution on different patterned wafers
- Fabrication of metastable fine grain on patterned wafer
  - Mechanism
  - Examples
- Conclusion

# Introduction

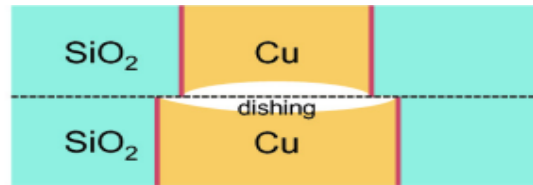
- The need for hybrid bonding
  - Increasing the density of interconnections to enable more functionality in each devices
  - Traditional solder technology is not suitable for pitch size below 10µm
    - Brittle intermetallic compounds (IMCs)
    - Circuit shortage (bridging solder), thermal stress, electromigration
  
- Some of the benefits of hybrid bonding
  - Reducing the resistance due to the Cu-Cu direct bonding without foreign material
  - Reducing the latency due to shorter interconnect



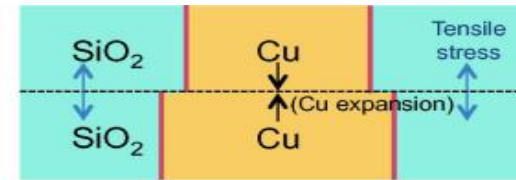
<https://www.amd.com/content/dam/amd/en/documents/epyc-business-docs/product-briefs/3d-vcache.pdf>

# Introduction

## Hybrid bonding process



- CMP with dishing Cu pad
- Room temperature bonding
- Dielectric surface bonding through Vander Waals forces
- Small dishing (gap) between the Cu pad



\*3D Microelectron IC Packaging: From Architectures to Applications, second edition, Springer

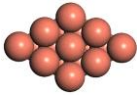
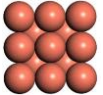
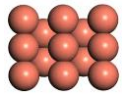
- Higher temperature annealing
- CTE mismatch – Cu expands more than dielectric
- Internal pressure and heat promote the Cu-Cu bonding strength

- Sensitive memory applications (HBM) require a reduction in thermal budget
- Grain engineering - thermal budget reduction paths
  - Modify the microstructure of Cu, particularly the grain orientation, grain size, grain boundary and their distribution
  - Enhance material properties such as mechanical strength, electrical conductivity, and electromigration

# Grain Engineering - Thermal Budget Reduction Paths

## ▪ Nanotwinned Cu:

- Nanotwinned Cu with (111) plane parallel to the bonding interface
- Higher atomic diffusivity of (111)

			
D <sub>surface</sub> (m <sup>2</sup> /s) / Temp(°C)	Cu(111)	Cu(100)	Cu(110)
150	6.85 × 10 <sup>-10</sup>	2.15 × 10 <sup>-14</sup>	6.61 × 10 <sup>-16</sup>
200	9.42 × 10 <sup>-10</sup>	1.19 × 10 <sup>-13</sup>	5.98 × 10 <sup>-15</sup>
250	1.22 × 10 <sup>-9</sup>	4.74 × 10 <sup>-13</sup>	3.56 × 10 <sup>-14</sup>
300	1.51 × 10 <sup>-9</sup>	1.48 × 10 <sup>-12</sup>	1.55 × 10 <sup>-13</sup>

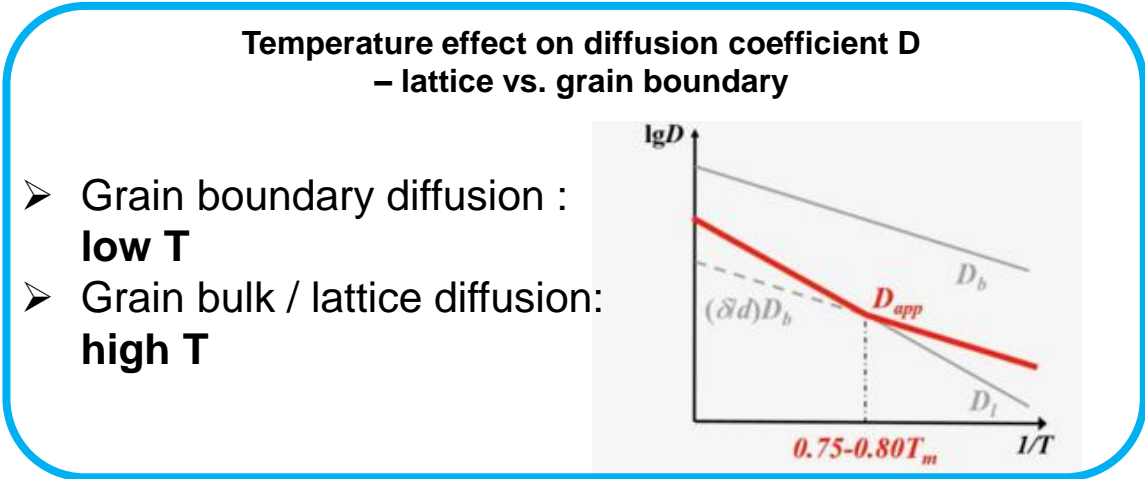
Calculated Cu surface diffusivity on (111), (100), and (110) planes at various temperatures, ranging from 150 °C to 300 °C \*

\* C.-M. Liu et al, Low-temperature direct copper-to-copper bonding enabled by creep on (111) surfaces of nanotwinned Cu. Sci. Rep. 5, 9734 (2015).

## ▪ Metastable Fine-Grained Cu:

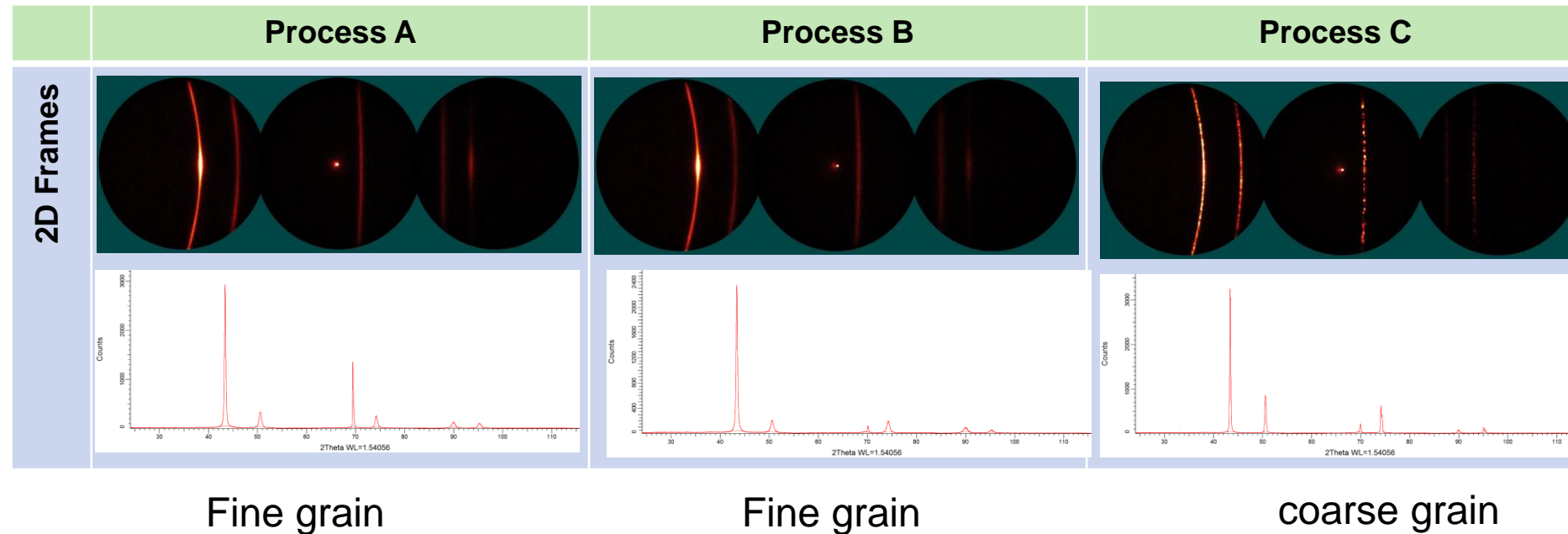
- Grains are stable during queue time before bonding process and grain grows during bonding process
- Energy released during grain growth promote Cu interdiffusion:

$$\Delta E \propto (1/d_i - 1/d_f)$$



# Screening of metastable fine grain on blanket wafer - XRD

- Chemistry and waveform screening
  - Debye rings
  - Peak width



# Mechanism of Cu grain evolution

## ▪ Velocity of a grain boundary $v = M * \Delta G$

- M: grain boundary mobility ;  $\Delta G$ : driving force / chemical potential difference / stored energy

$\Delta G$ : Driving Force – thermodynamics based	
<b>Positive force</b>	<b>Negative force</b>
grain boundaries	Zener pinning $-3\gamma F_v / 2r$ <div style="border: 1px solid black; border-radius: 15px; padding: 10px; margin-top: 10px;"> <ul style="list-style-type: none"> <li>• <math>\gamma</math>: surface energy</li> <li>• <math>F_v</math>: Volume fraction of pinning particles</li> <li>• <math>r</math>: particle radius</li> </ul> </div>
stacking faults	
Dislocation	
surface energy	
elastic strain/stress	
plastic strain/stress	

## M: Mobility – kinetics based - Arrhenius equation

$$M(T) = M(T_0) * \frac{T_0}{T} e^{-\frac{E_a}{K} \left( \frac{1}{T} - \frac{1}{T_0} \right)}$$

Ea: activation energy

- Grain boundary energy vs. misorientation angle

- Special high angle boundary (coincident site lattice)

- high stacking fault energy resulting in effectiveness of intragrain recovery / recrystallization – none-metastable status

# Mechanism of Cu grain evolution

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<b>Positive force</b>	<b>Negative force</b>
grain boundaries	Zener pinning $-3\gamma F_v / 2r$
stacking faults	
Dislocation	
surface energy	
elastic strain/stress	
plastic strain/stress	

## ■ Chemistry design:

- lower the positive driving force
- Rely less on Zener pinning to extend the self-annealing duration.

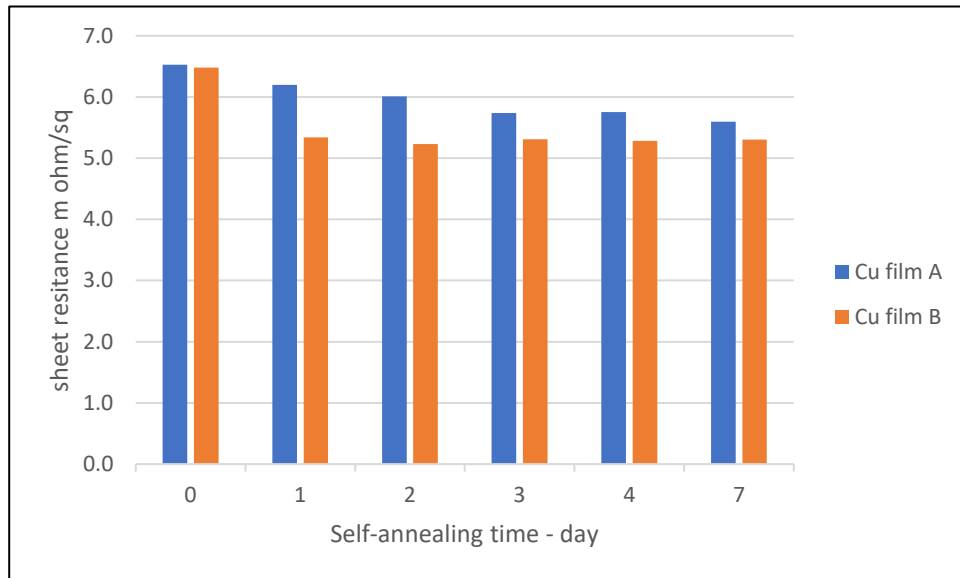
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Ea: activation energy

# Screening of metastable FG on blanket wafer – Sheet resistance

## ■ Waveform screening



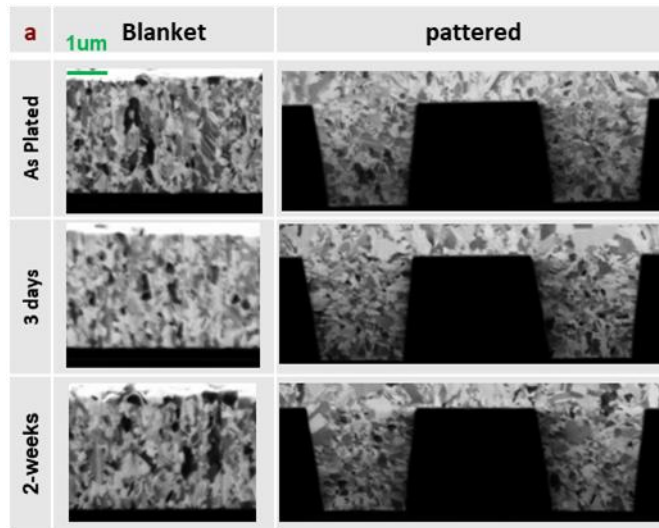
- In the case of Cu film A, the sheet resistance gradually decreases throughout the 7- day period – metastable fine grain Cu
- Conversely, for Cu film B, there is a significant decrease in sheet resistance by the second day, followed by a stable level thereafter – rapid thermodynamic stability



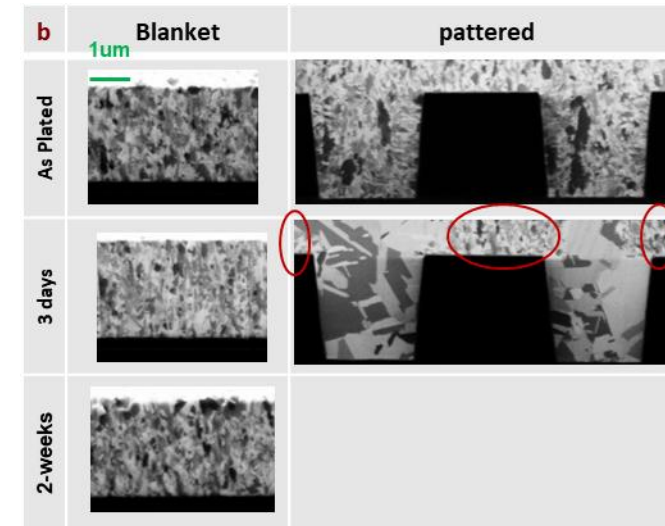
# Disparity of Cu grain evolution on blanket and patterned wafer

FIB / ion image for grain size characterization

## ■ Process A



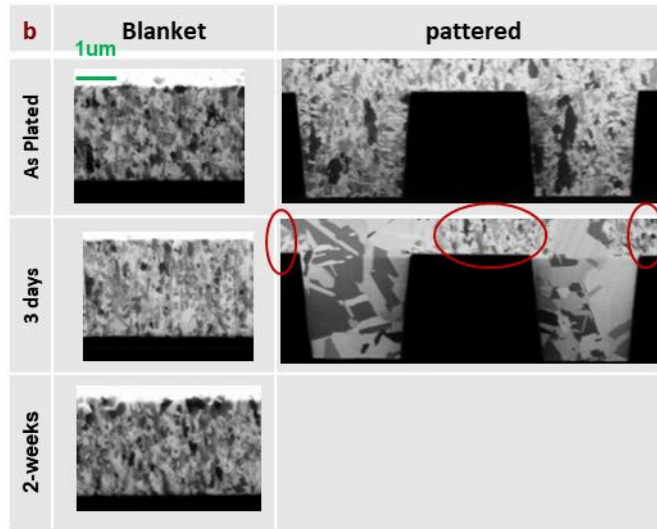
## • Process B



- In the case of Process, A, the fine grain exhibits stability for 2 weeks of room temperature self-annealing on both types of wafers.
- Conversely, Process B demonstrates stable fine grain on the blanket wafer, but on the patterned wafer, grain growth occurs inside the vias after 3 days of self-annealing.
- Not all the Cu structure evolution on the blanket wafer can transfer to the patterned wafer

# Disparity of Cu grain evolution on blanket and patterned wafer

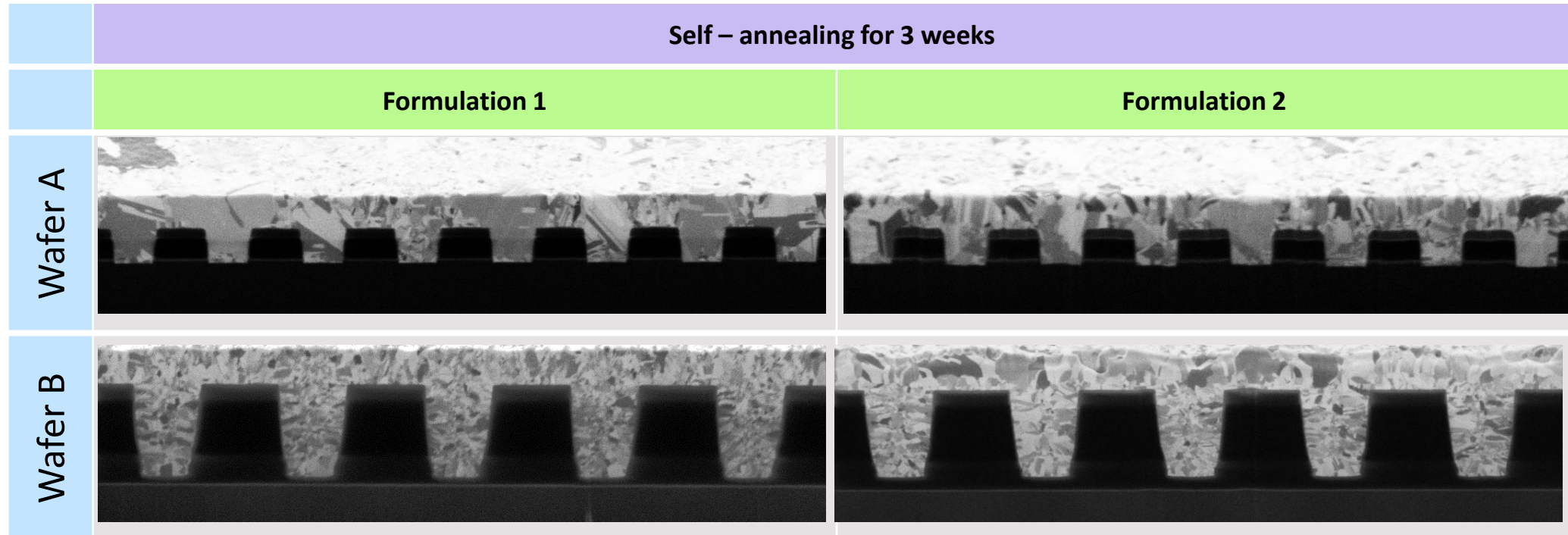
- Velocity of a grain boundary  $v = M * \Delta G$ 
  - M: grain boundary mobility;  $\Delta G$ : driving force



- Mobility is similar on both blanket wafer and patterned wafer (inside the via) at room temperature
- Difference in driving force: stress relieved constrained inside the via served as additional force

# Disparity of Cu grain evolution on different patterned wafers


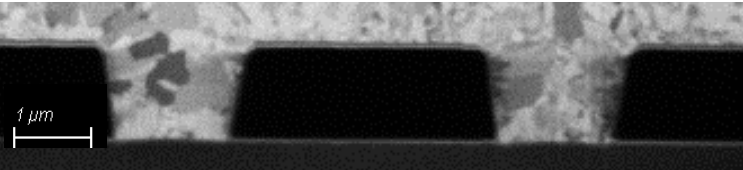
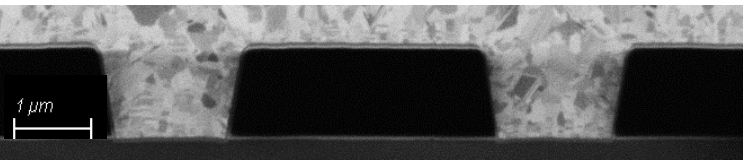
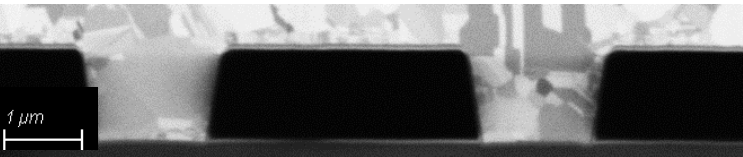
- Factors that affect grain stability : via density, via CD, and aspect ratio
  - For wafer A, grain grows with both formulation #1 and #2
  - For Wafer B, grain is stable with both formulation #1 and #2



# Fabrication of metastable FG on patterned wafer

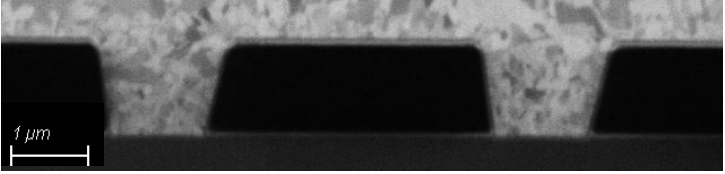
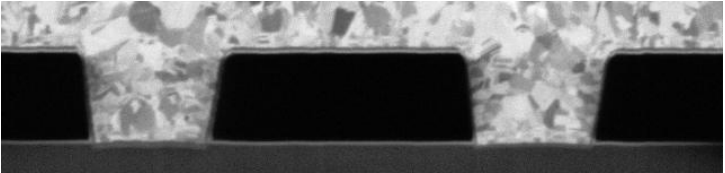
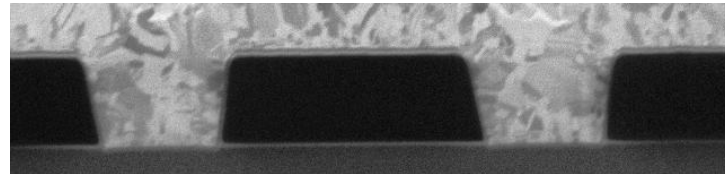
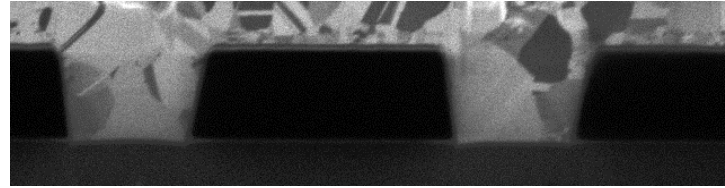
- Key grain stability criteria from different customers / processes
  - Metastable fine-grain Cu capable of maintaining its fine-grain structure at room temperature for at least 3 to 4 weeks
  - Grain growth at bonding temperatures, typically around 200 to 250°C
- Requirement of grain stability at medium temperature
  - Grain stability at medium temperature with different time frame according to integration process
- Impurity requirement
  - The lower the amount of inclusions, the better

# Example #1 of metastable fine grain

Annealing condition	Ion images	Grain size
As plated <b>stable</b>		~ 100 nm
4 weeks self - annealing <b>stable</b>		~ 100 nm
150 °C - 2 h <b>stable</b>		~ 100 nm
250 °C - 2 h <b>growth</b>		> 200 nm

- Fine grain on as plated and self-annealing
  - Minimization of the positive driving force
- Fine grain - 150°C annealing
  - Limited grain boundary mobility
- Grain grows at 250°C
  - higher mobility at 250 °C promote the grain growth
- Expect to enhance bonding strength at 250°C

# Example #2 of metastable fine grain

Annealing condition	Ion images	Grain size
As plated <b>stable</b>		~ 100 nm
170 °C - 40 min <b>stable</b>		~ 100 nm
170 °C - 40 min + 210 °C - 5min <b>stable</b>		~100 nm
280 °C - 2 h <b>growth</b>		> 200 nm

- Fine grain : as plated
- Fine grain : 170°C - 40 min
- Fine grain : 170°C - 40 min and followed by 210°C - 5 min
- Grain grows at 280°C
- Expect to enhance bonding strength at 280°C

# Conclusion

- Screening of metastable fine grain on blanket wafer through the XRD and sheet resistance
- Disparity of Cu grain evolution on blanket and patterned wafer could be due to the stress building up inside the patterned wafer
- Factors that affect grain stability on patterned wafer: via density, via CD, and aspect ratio
- Mechanism of fabrication of metastable FG on patterned wafer
- Showcase our metastable fine grain examples

# Acknowledgement

## ■ Thanks to my colleagues

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