Enabling High Aspect-Ratio Interconnects for Advanced Packaging of MEMS and Sensors

Matt Weimer, Director of R&D
mweimer@forgenano.com

TP4: Emerging Technologies: MEMS/Sensors, Additive Manufacturing, mmWave/RF, 5G/6G/High Frequency, Glass Track

Corporate headquarters located in Denver, Colorado

Recognized as the market leader in particle atomic layer deposition (PALD)

01

World-leading materials science company specializing in the development of Atomic Layer Deposition (ALD) equipment and processes

02

120+ employees including subject experts in materials science, chemistry and physics

03

65,000 sq ft facility with 20+ ALD tools, full demo capabilities, battery testing lab, and manufacturing. Class 10-100 clean room recently completed.

04

Fully Staffed Tech Service Team
Installation and Training
Service Contract Support

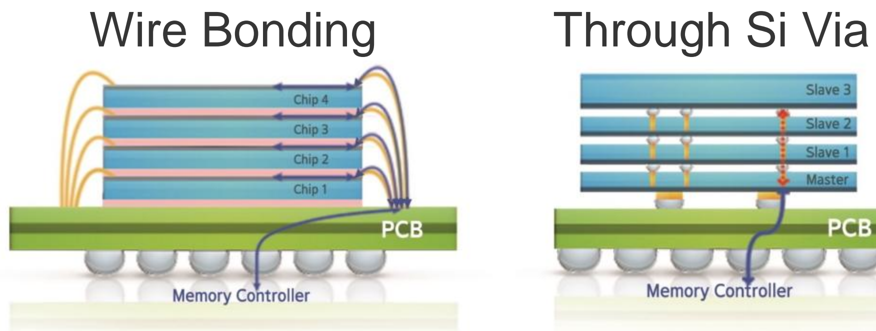
05

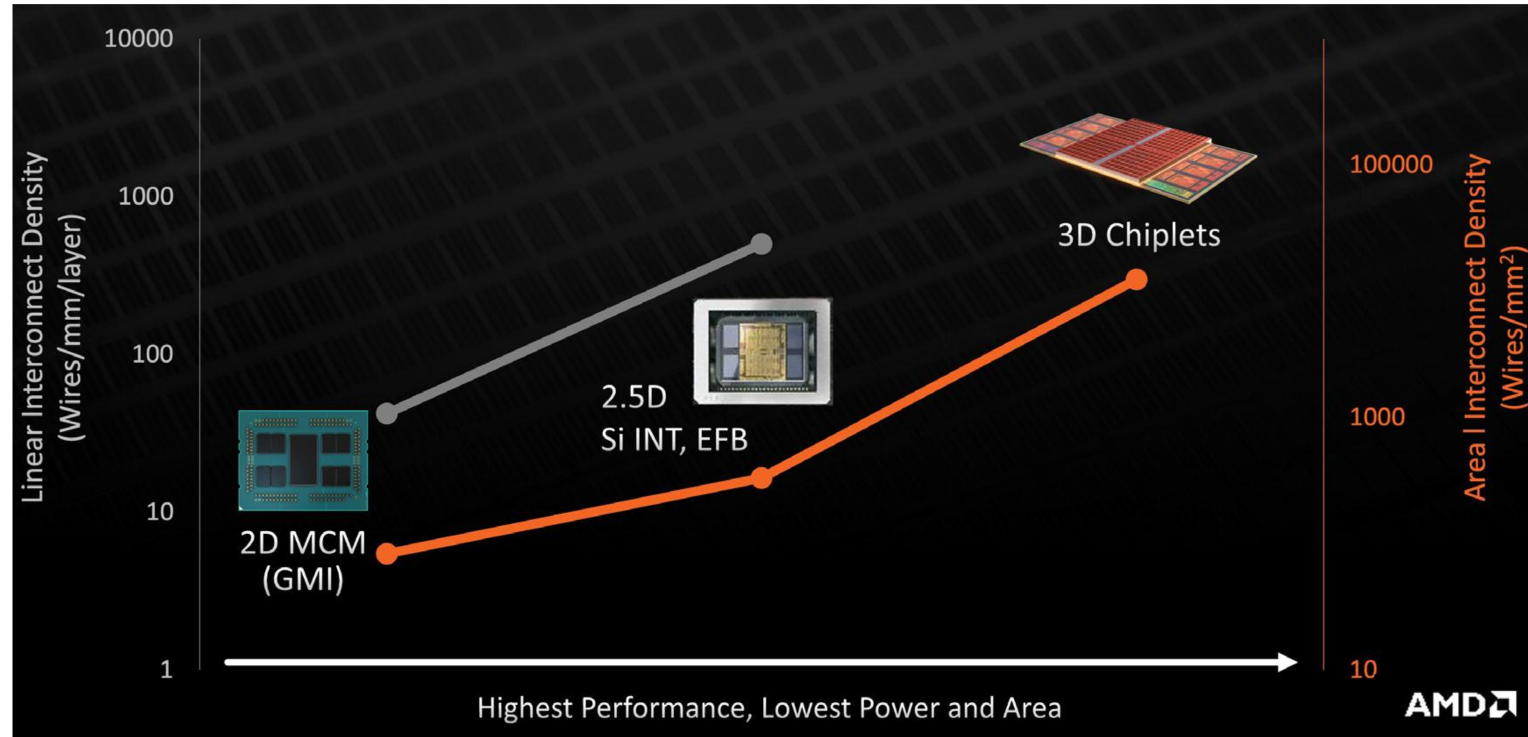
Winner of R&D 100 and Deloitte Fast 500 awards for innovative tech and rapid growth

Advancements in Packaging Require Advancements in Metallization

Performance and energy efficiency boosts are moving out of the transistor and into the package

Moving to 3D Chiplets and heterogeneous integration requires higher pitch (and aspect ratio) interconnects

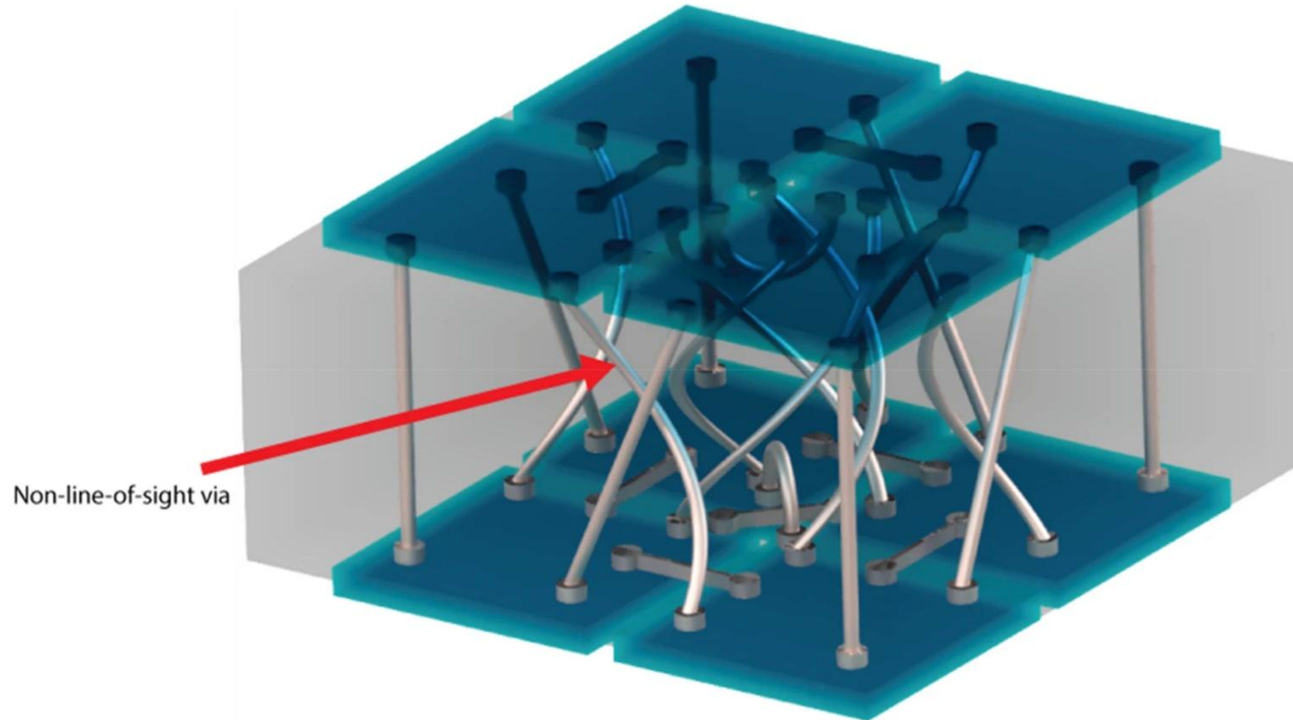




Microelectronics and Advanced Packaging Technologies Roadmap, 2023, Semiconductor Research Corporation

Next-Gen TSV, TGV and interposer technologies need a high AR metal barrier seed solution, currently limited to 10:1

Move Beyond Line-of-Sight Limitations

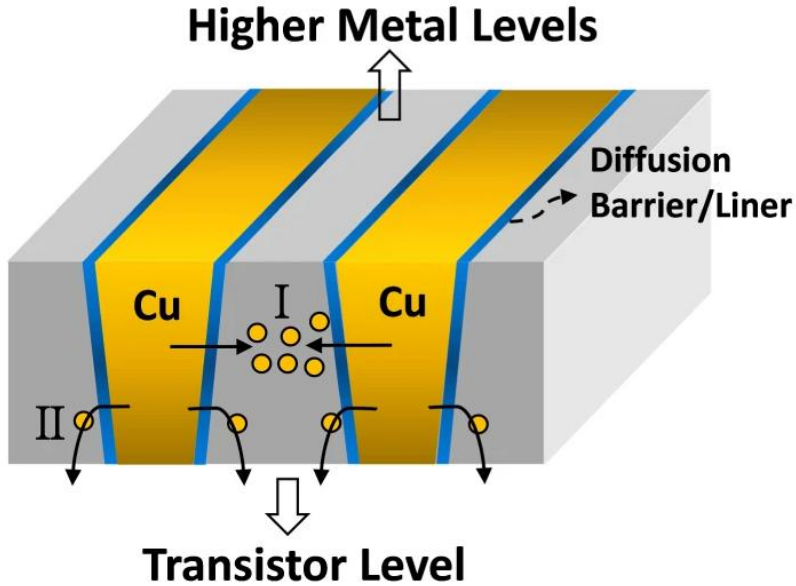


What would be possible if vias were not restricted to line of site architectures?

Metallization is a critical barrier

Payne, J.E., Nyholm, P., Beazer, R. *et al.* Fabrication of high aspect ratio, non-line-of-sight vias in silicon carbide by a two-photon absorption method. *Sci Rep* **14**, 2176 (2024).

Why Does Cu Need So Much Help?

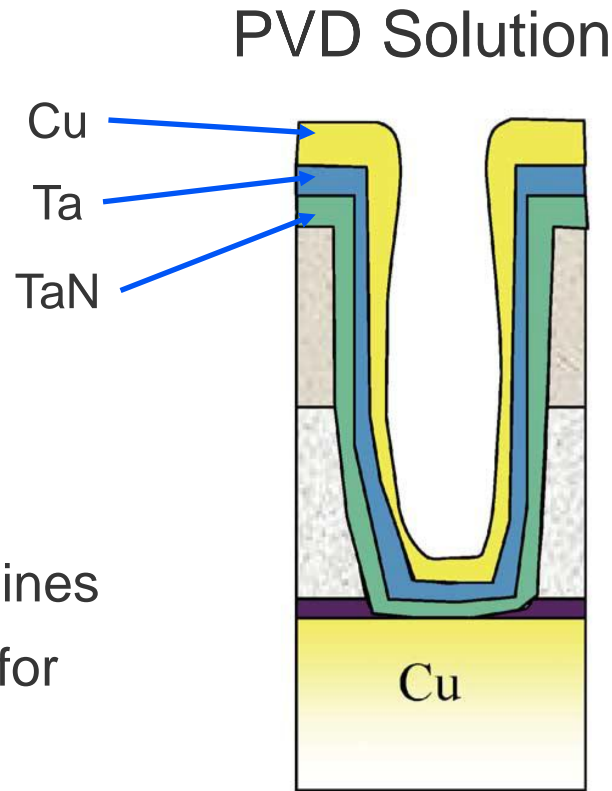


Cu can diffuse between interconnect lines

Cu needs a highly conductive seed for electrodeposition

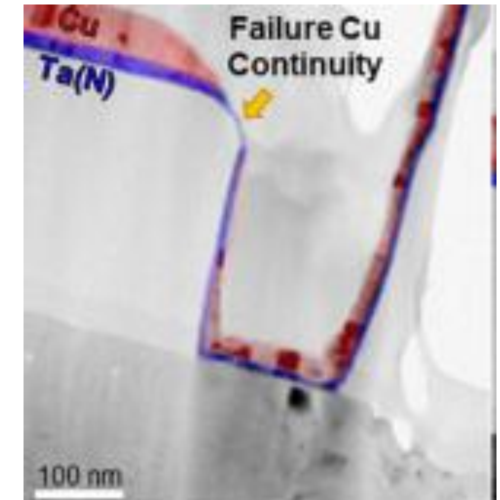
Seed layer needs adhesion layer

PVD Solution



Kim, H., et al., Surf. Coat. Tech., 200, 3104–3111 (2006)

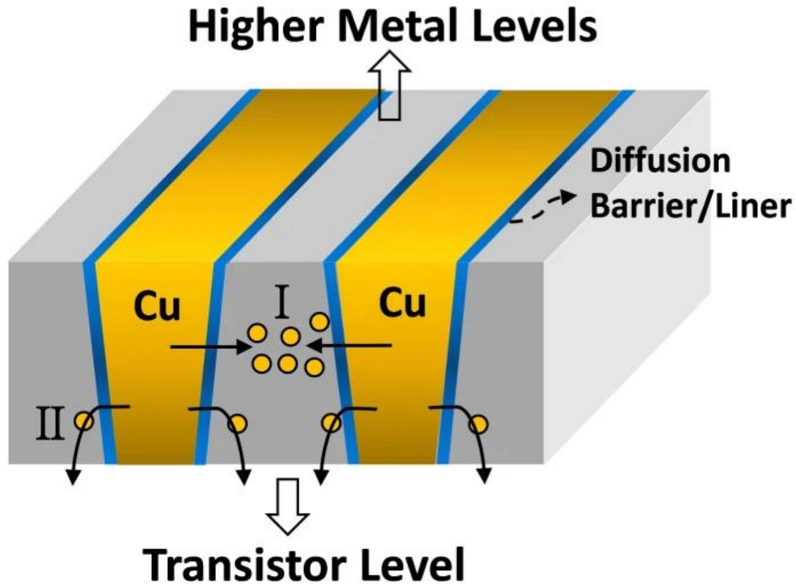
PVD Failure



Pegoraro, E., et al., Microelect. Eng., 256, 15,111717 (2022)

Current PVD solutions for Cu barrier seed are limited to 10:1 aspect ratio vias

How is Atomic Layer Deposition Different?



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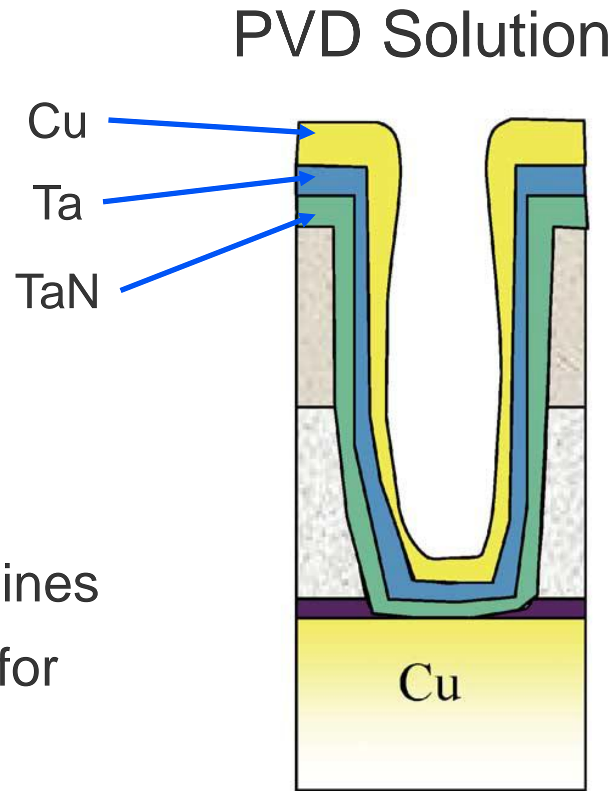
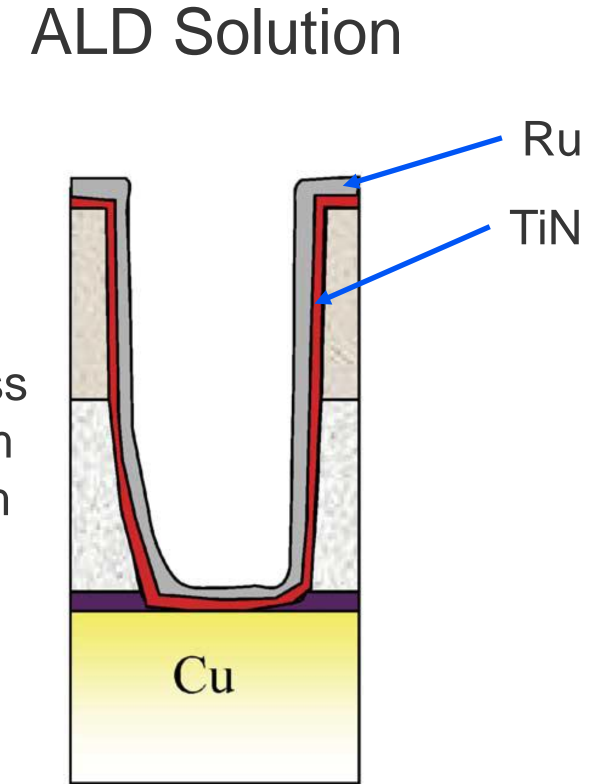
PVD Solution



Kim, H., et al., Surf. Coat. Tech., 200, 3104–3111 (2006)

Total Thickness
PVD = >60nm
ALD = <12nm

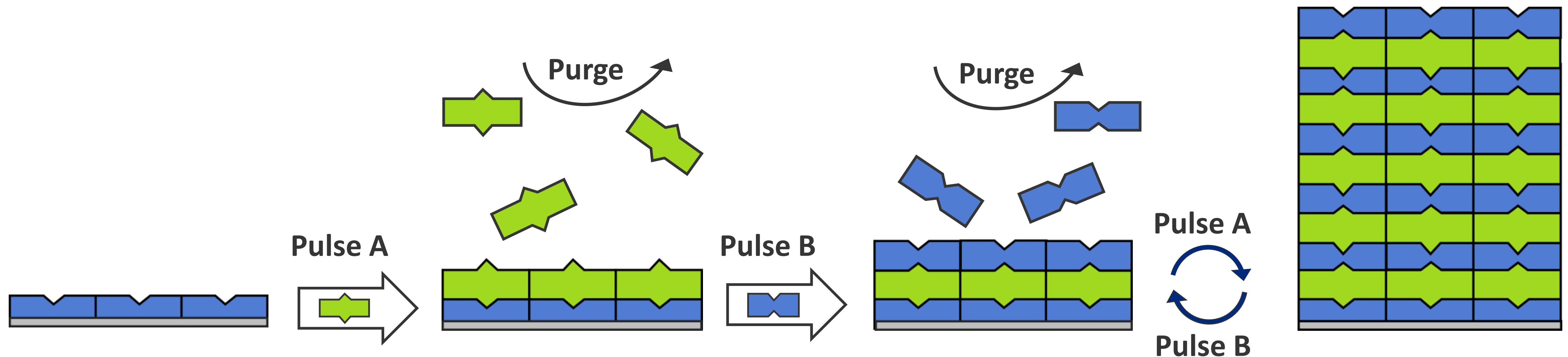
ALD Solution



ALD provides a conformal coating that is high quality and pinhole free

Atomic Layer Deposition is Surface Chemistry

ALD is all about sequential surface reactions to deposition thin films **atomic layer** by **atomic layer**



What is a good way to visualize ALD?

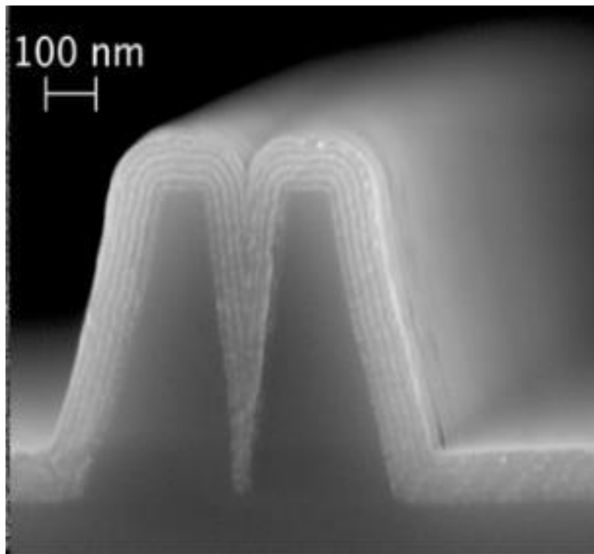
How to Visualize Atomic Scale Manufacturing

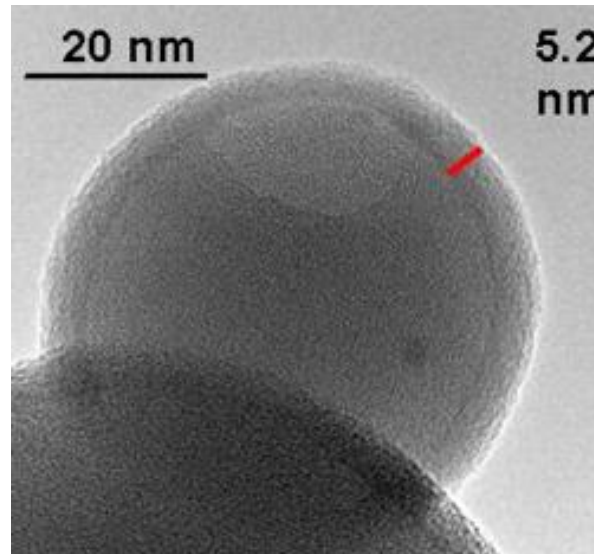
http://whiteapronblog.com/2017/06/02/north-carolina-thirteen-layer-cake/

Who doesn't love cake!?!

Atomic Layer Deposition is Surface Chemistry

Based on spontaneous, sequential, self-limiting
thermal reactions that add material with atomic level control



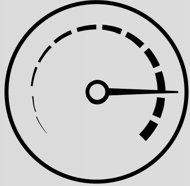
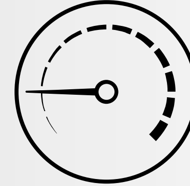


- Conformal Coating
- Precision Thickness Control
- Tailored Multilayers
- High Surface Adhesion
- High Quality Films
- Low Temperature Process

ALD can provide conformal, pin-hole free, high density films, for a range of applications, but is slow and expensive

Why isn't ALD more Broadly Adopted?

Traditional cross-flow ALD reactors are stuck in a tradeoff

Reactor pressure increase	Reactor pressure decrease
 Precursor use improves	 Precursor use degrades
Purge time longer	Purge time shorter

One must choose between efficient precursor use (~50% ALD CoO) or high throughput

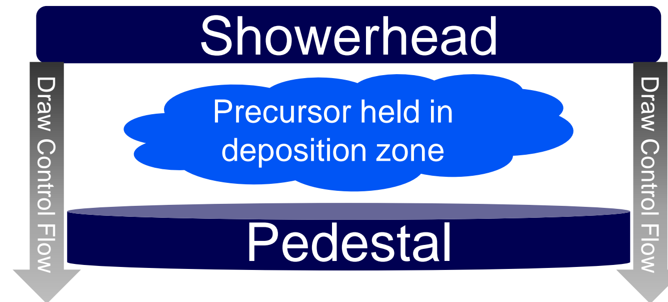
Forge Nano ALD^X Difference

The Hardware

Fast Pneumatic Valves (FPVs)

For precision dosing and efficient precursor use

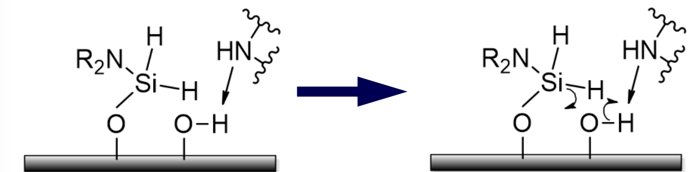
The Chamber



Synchronously Modulated Flow & Draw (SMFD)

For quick deposition rates, efficient purges and minimal maintenance

The Chemistry



Klaus, J., Sneh, O., George, S.M., Science, *1997*, 278, 5345, 1934-1936

Catalyzing Reactions for Induced Surface Process (CRISP)

For easy process integration without plasma

ALD^x allows for faster ALD cycle time, more efficient precursor use, improve wafer throughput and cost

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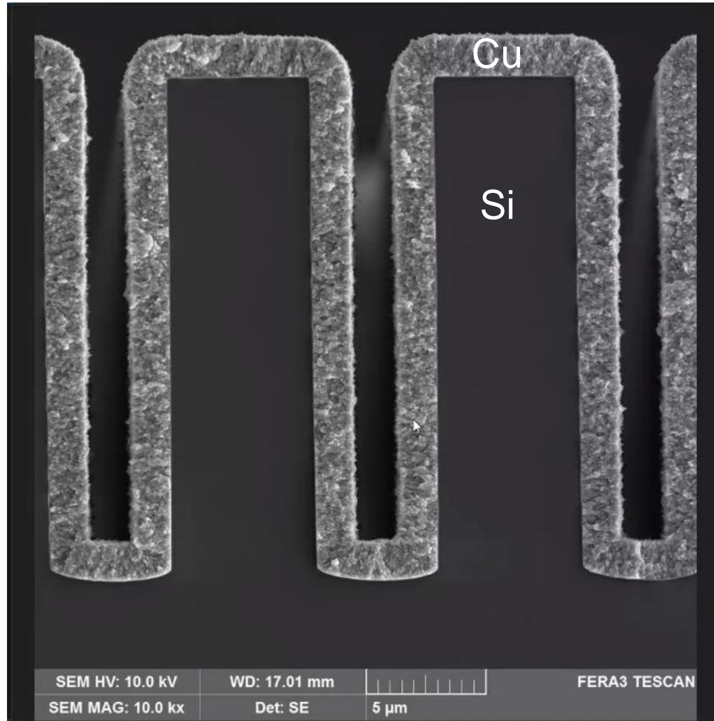
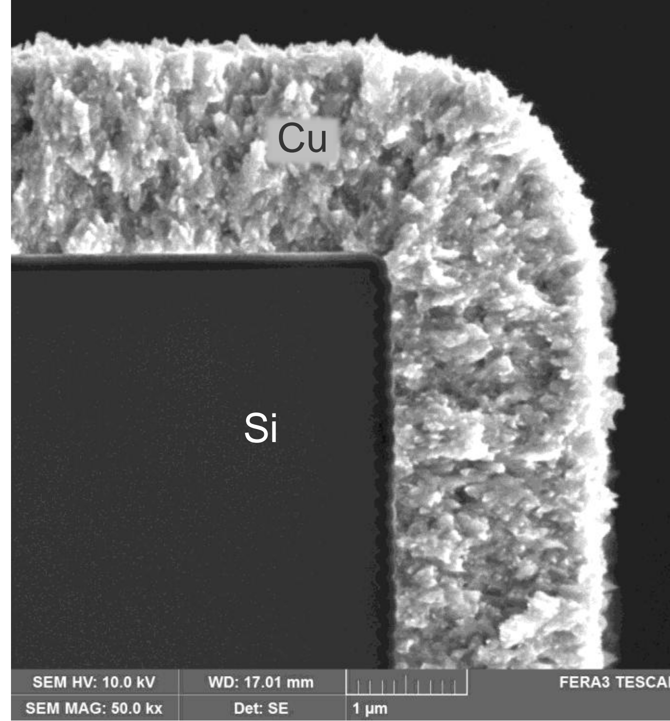
Successful Demonstration of Conformal Cu Electrodeposition on ALD





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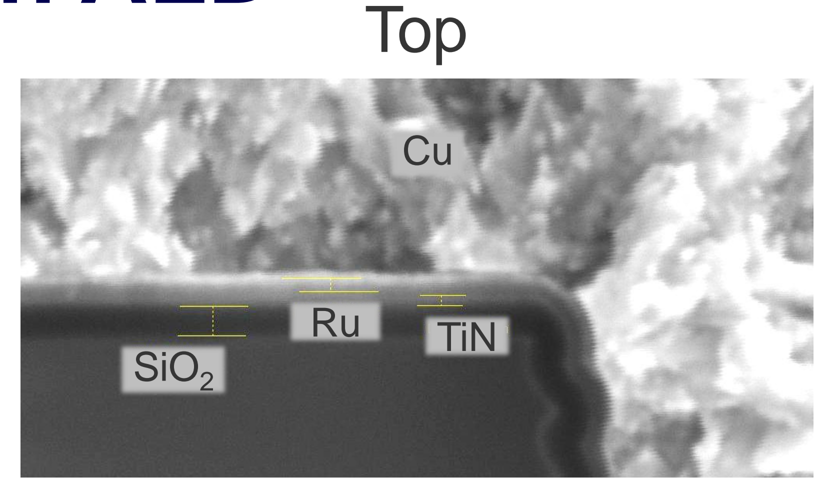

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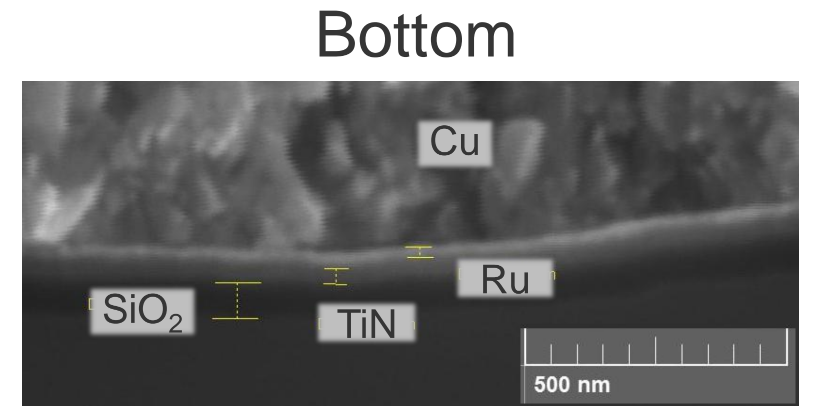

Full stack successful conformal electrodeposition at C2MI

Oxide/Barrier/Seed Layers

- ✓ 100nm SiO_2 CRISP
- ✓ 50nm TiN
- ✓ 20nm Ru

Demonstrated on up to 25:1 TSV and 30:1 TGV, total deposition time ~1.5 hours

CRISP SiO_2 shows superior performance to PEALD

PRODUCTIVITY	FILM QUALITY	DIELECTRIC PERFORMANCE
Shorter Deposition time by 3x **42 min for CRISP** vs 126 min for PEALD (Deposition time for 100nm on 200mm)	***Increased Film Density by 6%*** **2.32 g/cm^3 for CRISP** vs 2.19 g/cm^3 for PEALD	***33% Higher Breakdown Voltage*** **>12 MV/cm for CRISP** vs >9 MV/cm for PEALD
Reduce Precursor Waste by 66x **275 Torr·s for CRISP** vs 18,175 Torr·s for PEALD (Si Consumption per 100nm)	***Maintain RI and Dielectric Constant*** **1.44 & 4.0 for CRISP** vs 1.45 & 4.1 for PEALD	***No Change in Leakage Current*** **<10^{-10} A/mm^2 for CRISP** vs <10^{-10} A/mm^2 for PEALD (@ 2MV/cm)

All results at 275 °C

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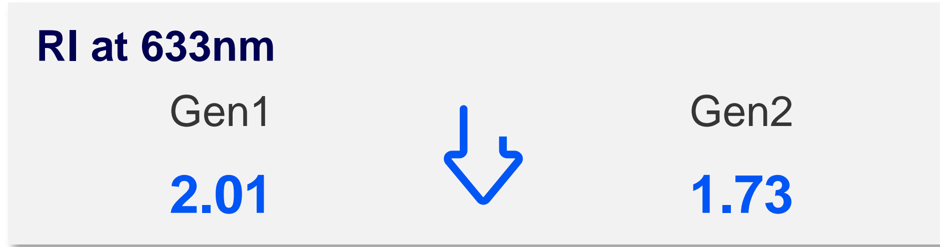
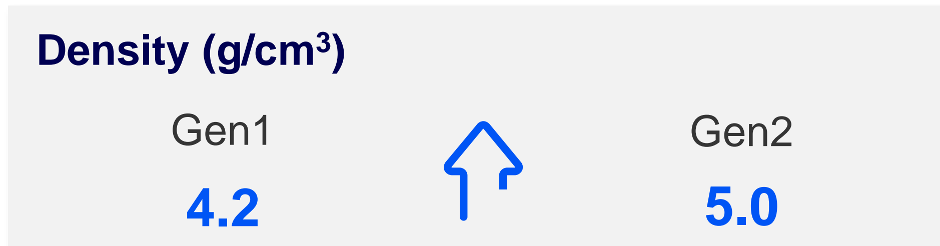
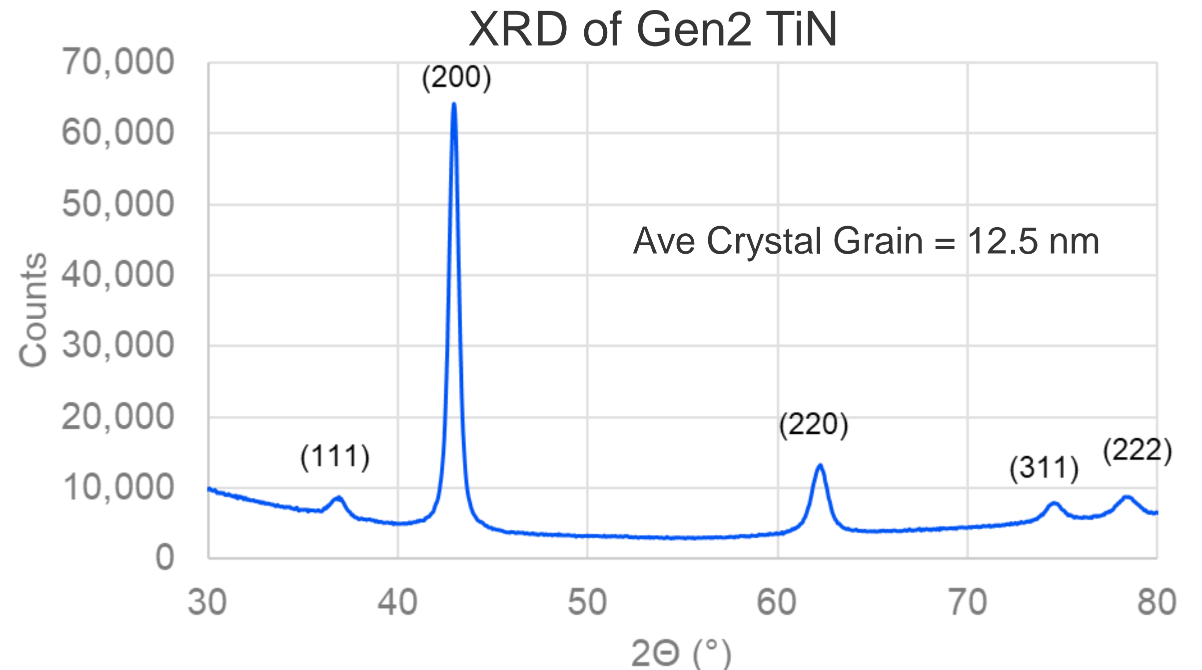
ALD^X TiN Improvement

Gen 2 Improvement





Resistivity



Gen 2 TiN is a significant improvement over Gen 1, need to test Cu barrier performance

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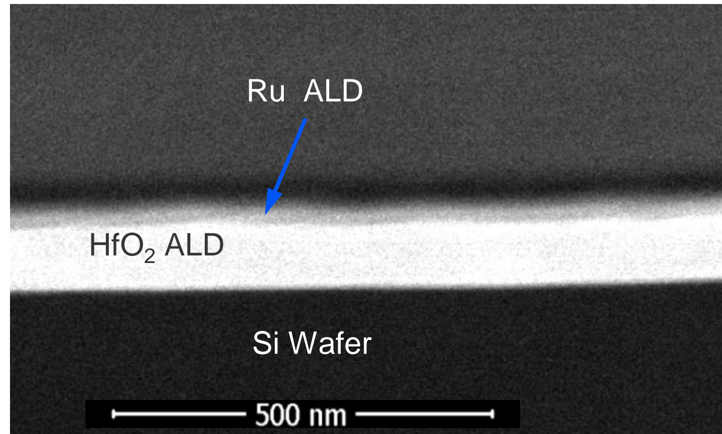
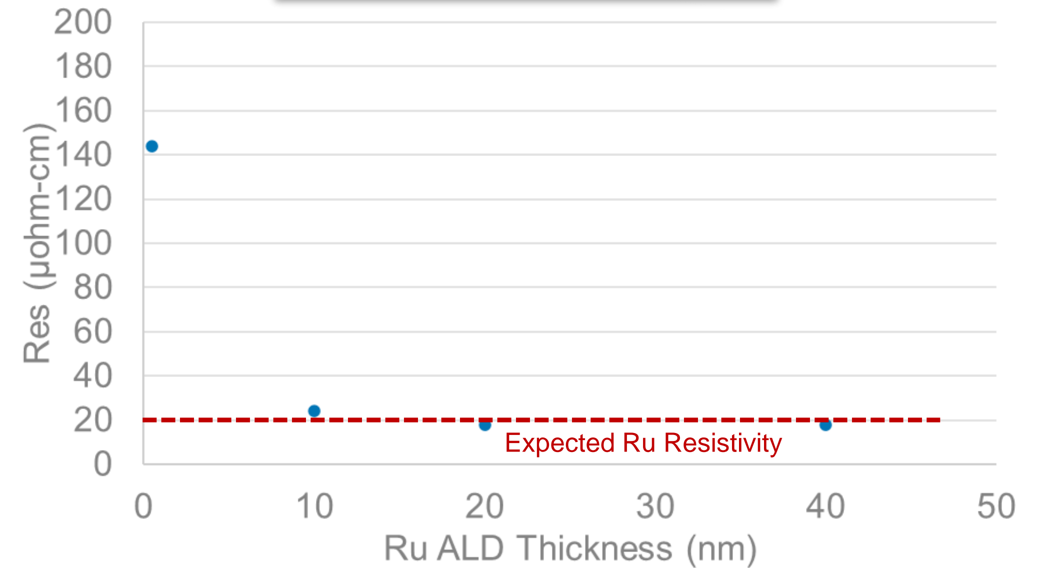
High quality Ru ALD in the ALD^x Platform





Deposited on a range of surfaces

- Pt, Au, HfO_2 (ALD), TiO_2 (ALD), TiN (ALD), SiO_2 (ALD/thermal)

- **GPC on TiN = 0.45 Å/cy**
  - ~5s/cycle (unoptimized)
  - 0.5 nm/min deposition rate
- **Demonstrated on 25:1 AR features**

Low resistivity continuous between 5-10 nm

- <20 *u*Ω·cm to plateau above ~20nm

- **High film density**
  - 12.0 g/cm^3 by XRR
- **Small Ru crystal grains**
  - 8.5 nm average grain size

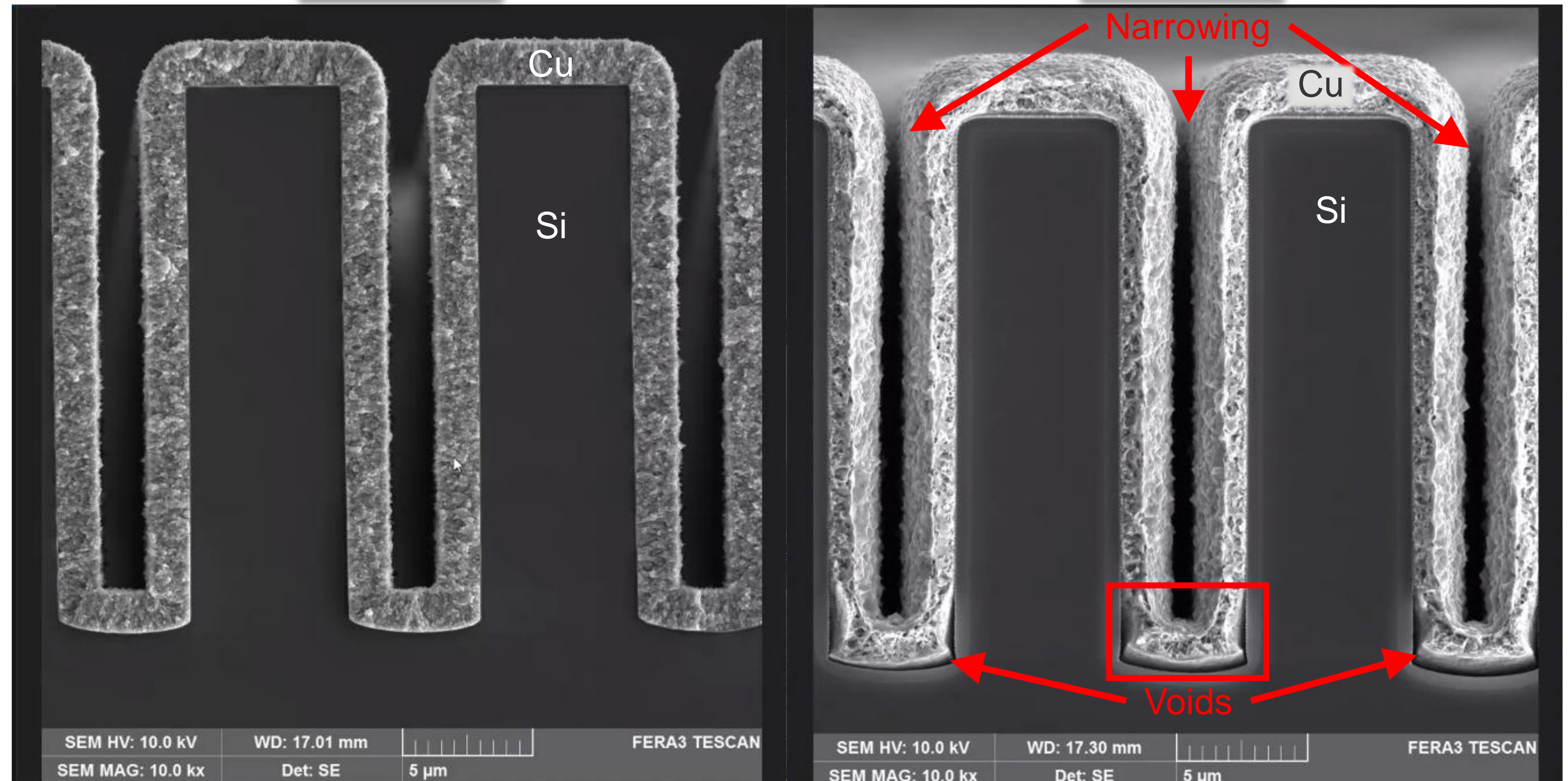
ALD^x Ru film provides a low resistivity conformal ALD metal film under 10nm

Cu Barrier/Seed for Next Gen Vias

4:1 Aspect ratio features
- 5 μm opening and 20 μm depth

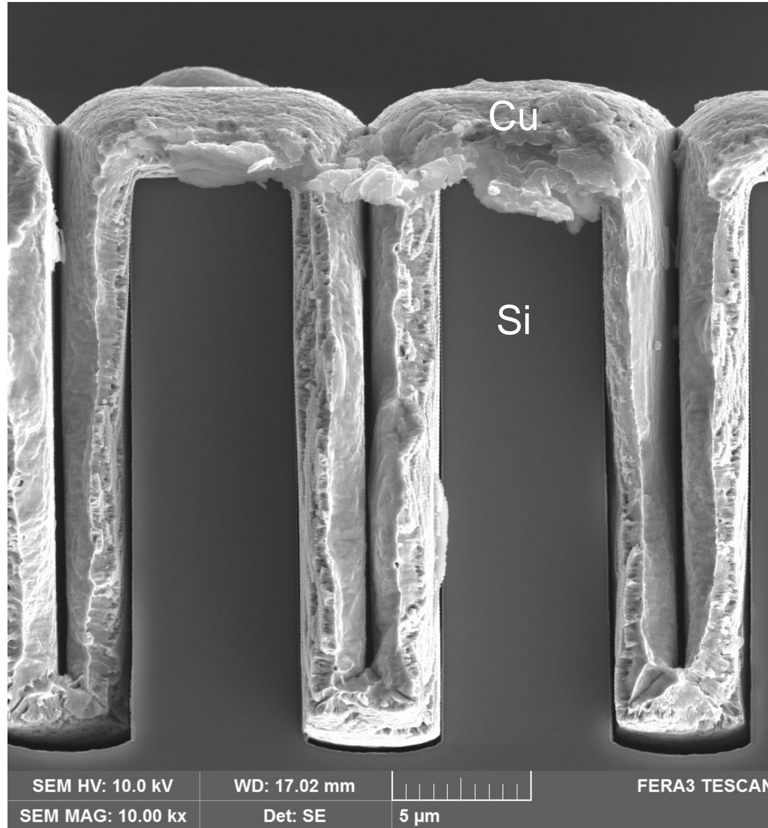
Sputtering fails at the bottom of vias
- Ti/W adhesion and Cu seed
- Leads to device failure

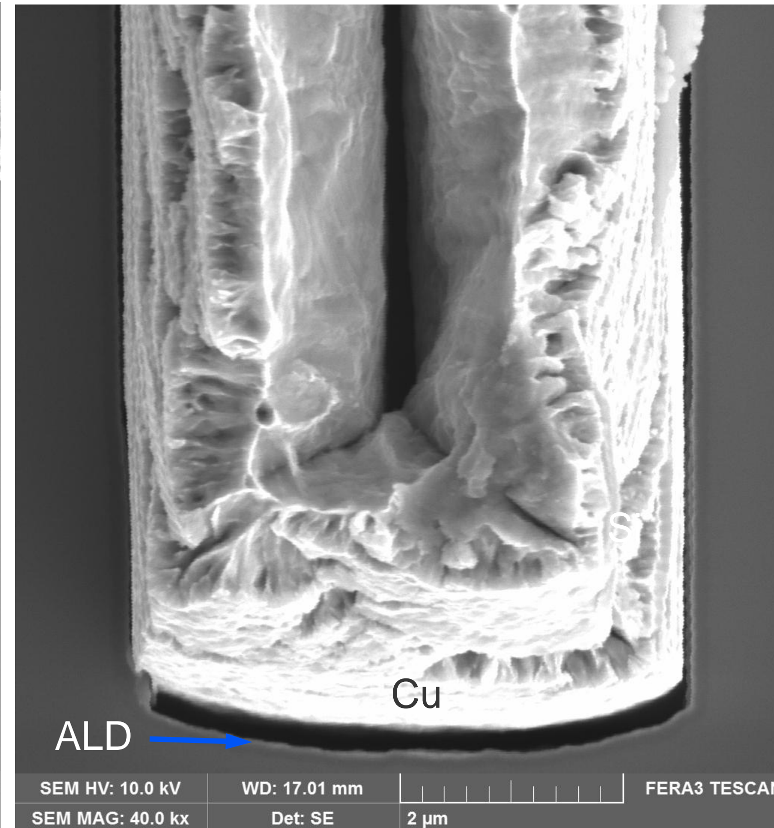
Currently measuring via fill resistance



ALD provides conformal, well-adhered Cu electroplate seed layer

Ru is NOT Cu, but that's OK





Failure of Cu adhesion on ALD stack due to RuOx formation over >2 week in ambient

Must drive to much lower potential
- -0.2 to -0.4 V SCE in $CuSO_4$

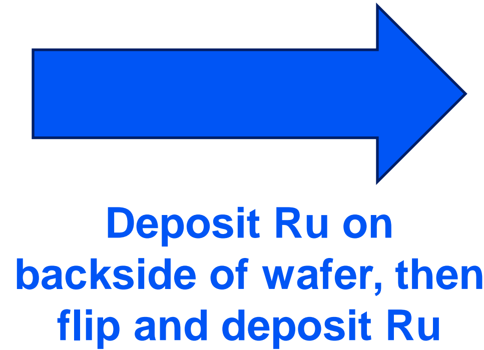
Ru oxidizes more quickly than Cu
- RuOx is still conductive
- Cu adhesion is poor
- RuOx formation is reversible
  - H_2 reduction in vacuum
  - H_2 addition into bath
  - Special thanks to Tom Moffat and Dan Jessell at NIST
    - T. P. Moffat, et al., Electrodeposition of Cu on Ru Barrier Layers for Damascene Processing. *Journal of the Electrochemical Society*, 153(1), 2006, pp. C37-C50

Ru can oxidize, but does not necessarily require a change in device process flow

Global Adhesion of Cu ECD on Through Vias

ALD Applied to Single Side

Clear delamination of Cu ECD



Deposit Ru on backside of wafer, then flip and deposit Ru

ALD Applied to Both Sides

Full wafer adhesion

ALD Ru must be applied to both sides of a wafer with through vias

ALD Ru Enabling High AR Via Seed

Cu ECD in >25:1 AR vias
- ALD Ru can provide >50:1

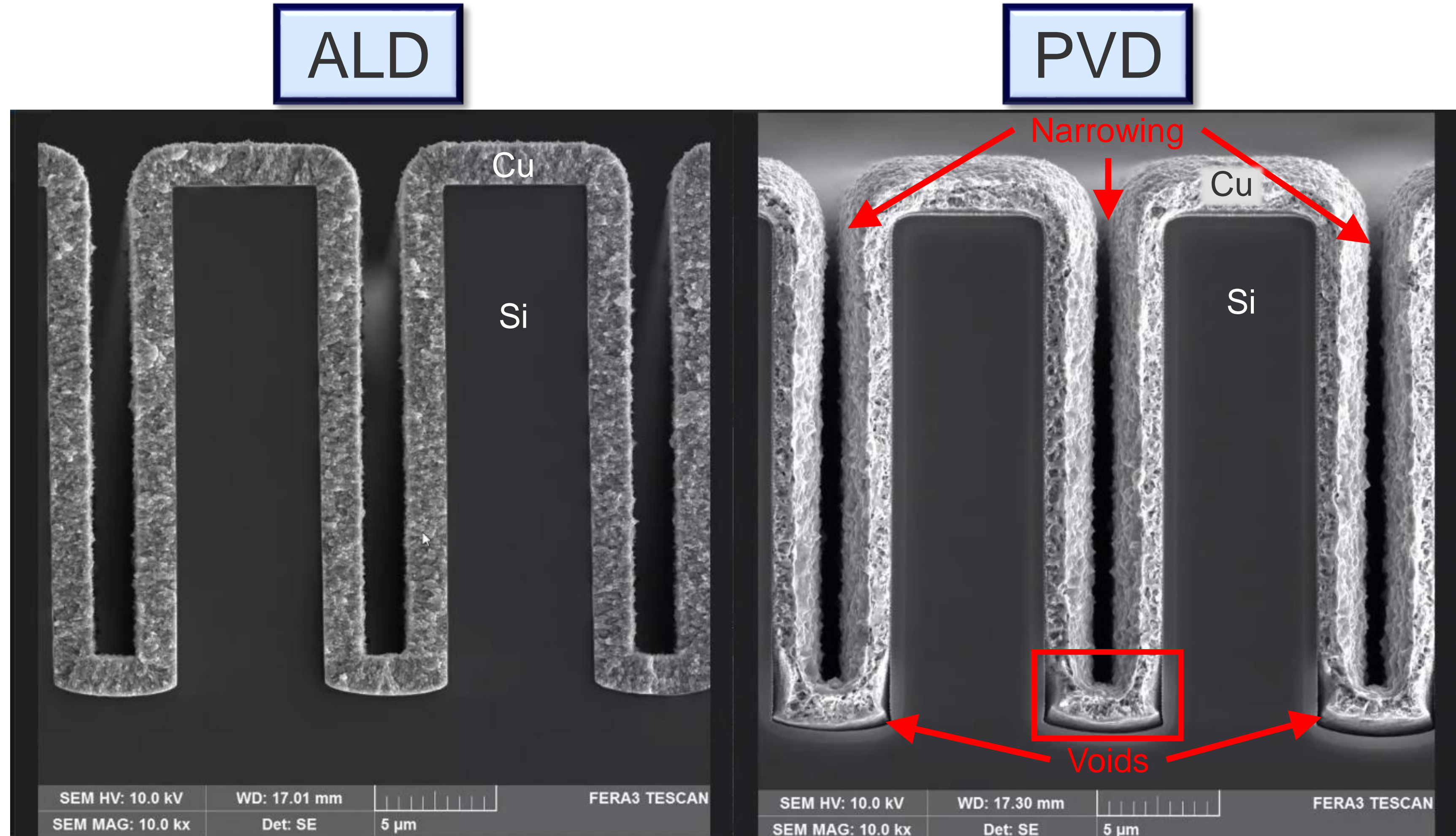
TEPHRA ALD^x chamber
- Enables high wafer throughput Ru ALD

Cu ECD is different,
- More negative voltage

Ru oxidation must be considered
- Avoiding or removing oxide

Blind vs through vias
- Single vs double side ALD

Currently measuring via fill resistance



Connect with our team during the conference!

Dr. Matthew Weimer
Director of R&D

Ray Burghard
Semiconductor Sales Manager

Kevin Person
Equipment Sales Manager

Craig Steinroeder
VP, Sales & Marketing

To set a meeting or receive more information about our ALD solutions, please message us at

marketing@forgenano.com

ATOMIC LAYER DEPOSITION SYSTEM

Back-up Slides

Matt Weimer, Director of R&D
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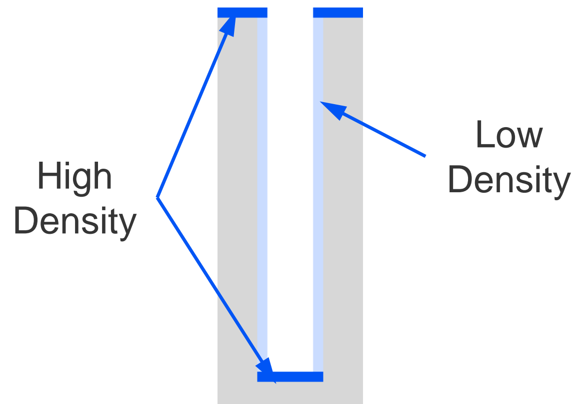
TP4: Emerging Technologies: MEMS/Sensors, Additive Manufacturing, mmWave/RF, 5G/6G/High Frequency, Glass Track

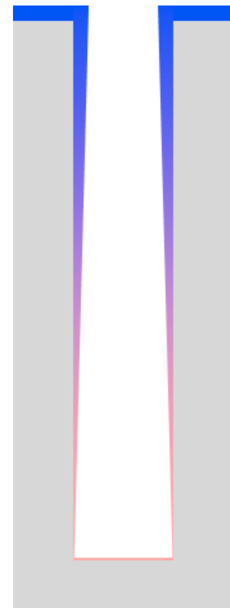
Limits of Thermal and Plasma Enhanced ALD

Loss of thickness conformality

Change in film composition down the features

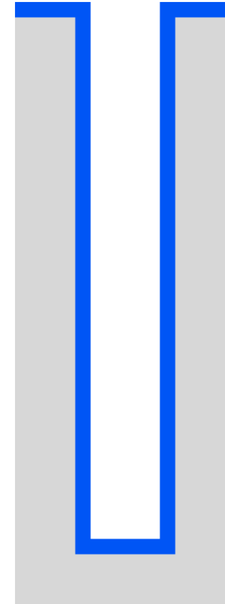


Plasma-Enhanced ALD



vs

Thermal ALD

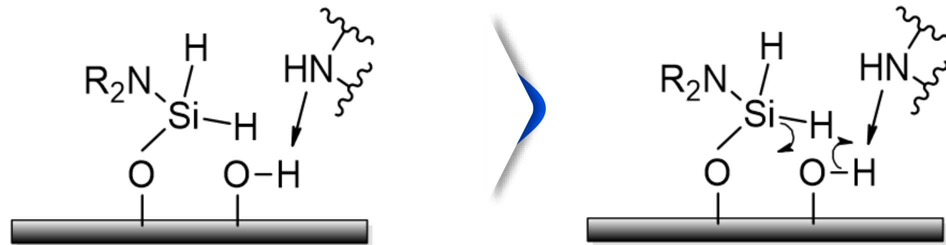


Requires higher energy as temperature

Undesired chemical reactions leave impurities

PEALD provides low temperature and hard-to deposit materials but **struggles** to provide conformal films for **aspect ratios greater than 10:1 for some materials**

SiO_2 Catalyzing Reactions for Induced Surface Process (CRISP)



Klaus, J., Sneh, O., George, S.M., Science, *1997*, 278, 5345, 1934-1936

Addition of N-based Lewis Base as a catalyst
- Unique chamber design and FPVs allow non-metal catalyst use in standard 2-step ALD process
- Post-dep analysis shows no catalyst contamination

BENEFITS

Deposition range – 75-300°C

Density over that range – 2.18-2.32 g/cm^3

Time/cycle – 0.8-2.5s

CRISP Chemistries in Development

Oxides: SiO_2, HfO_2, TiO_2, Al_2O_3

Nitrides: TiN, AlN

Elements: Ru

Fully characterized and in production

SiO2 CRISP is a high-quality dielectric, with low impurities

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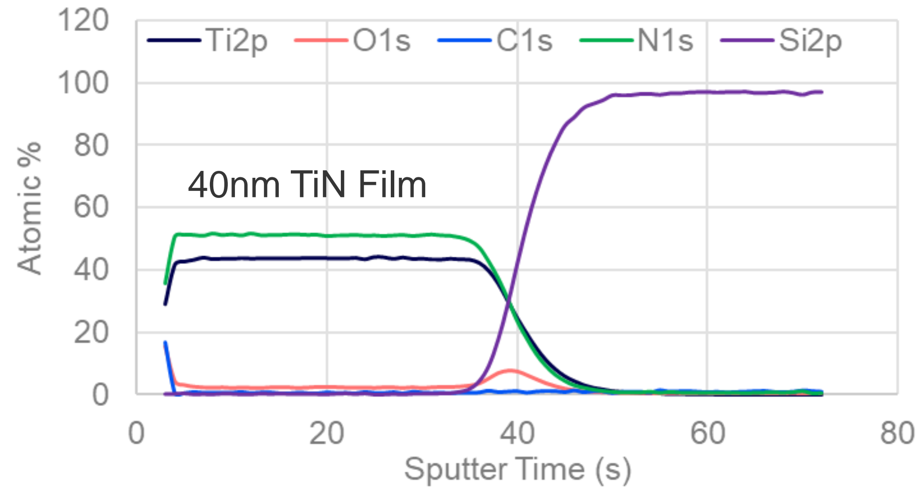
Next Step: Improving the ALD Films

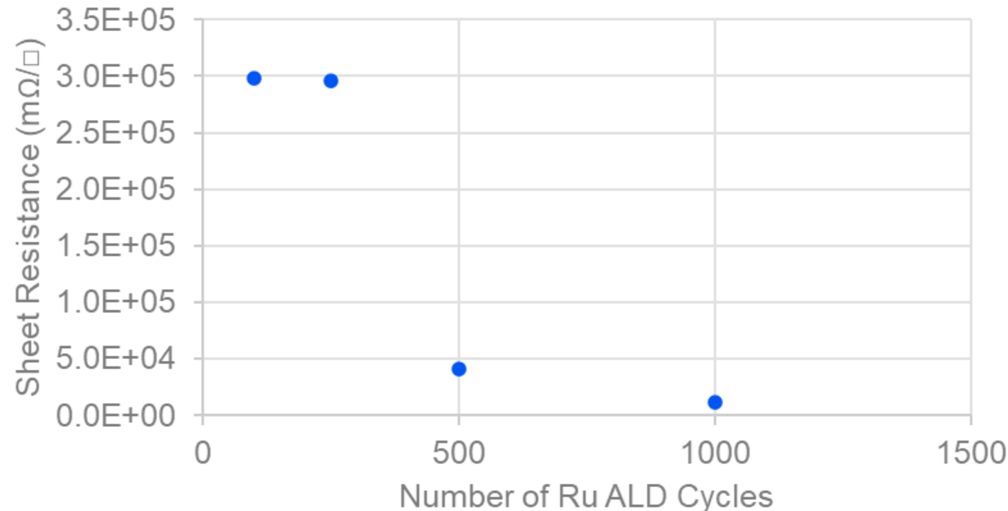
TiN ALD Improvement



Impurity content in TiN too high

- O content is hurting resistivity
- Ti:N ratio is 0.85
  - Excess N
- Dedicated nitride chamber
- New ALD processes possible (CRISP)

Ru Improvement



Nucleation delay on TiN problematic

- Big decrease in sheet resistance between 250 and 500 cy
- Nucleation delay and film coalescence
- New ALD processes possible (CRISP)

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