A Nanopackage for Silicon Nanowire-Based Sensor Applications

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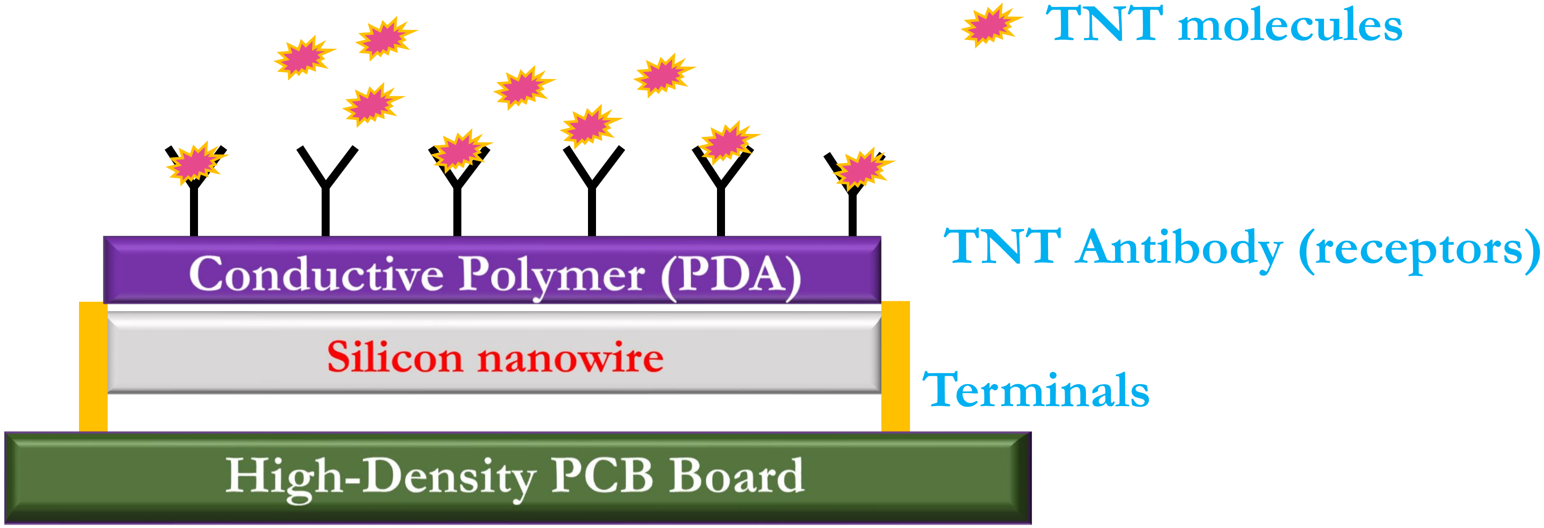
Outline

- Introduction to SiNW integrated sensors device
- Synthesis and cleaning of Silicon Nanowires
- Fabrication of sensor chips
- Packaging the chip
- Surface functionalization
- IV measurements

Introduction to SiNW-based nanosensors device

Conductive Conjugated Polymer is required on SiNW



TNT molecules

TNT Antibody (receptors)

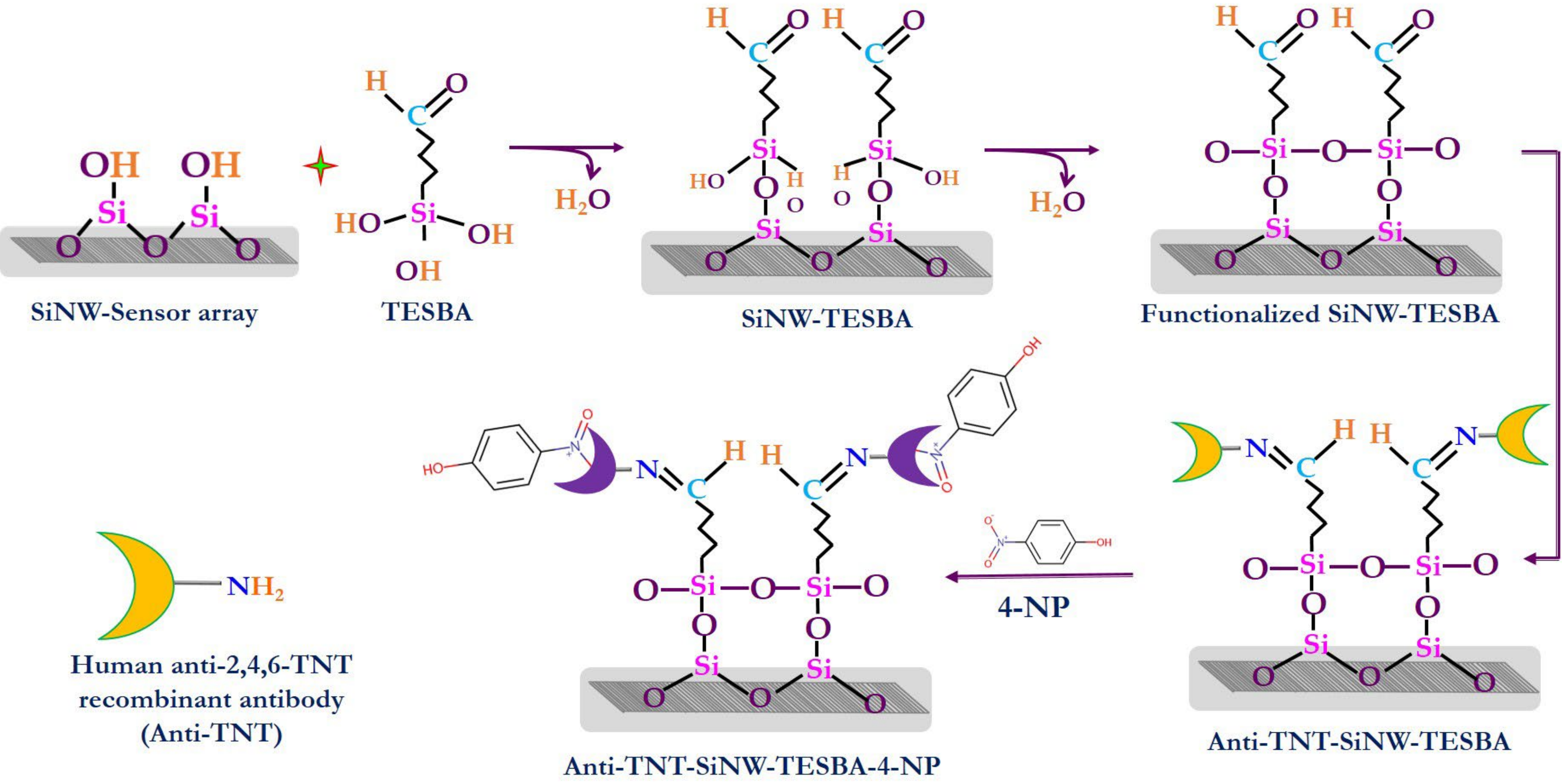
Conductive Polymer (PDA)

Silicon nanowire

Terminals

High-Density PCB Board

Work Structure and Methodology



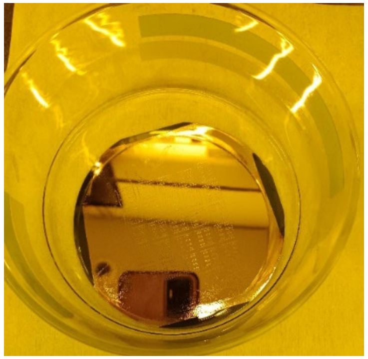
Scheme for the fabrication and functionalization of TESBA-Silicon nanowire-based nanosensor device for the selective detection of 4-nitophenol.

Detailed Steps in Chip Fabrication

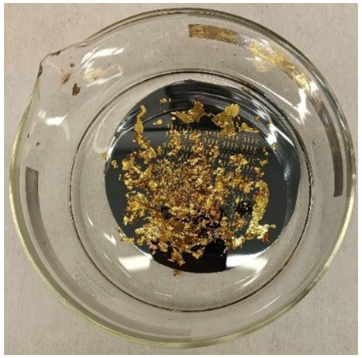
Lift-off process

Remover PG

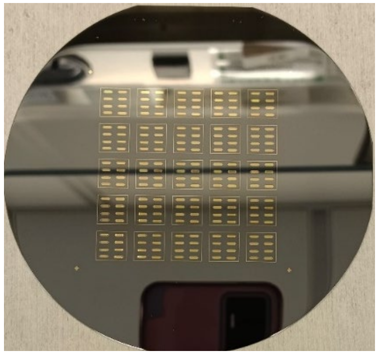
Remover PG (80 °C)



Remover PG / 2hrs



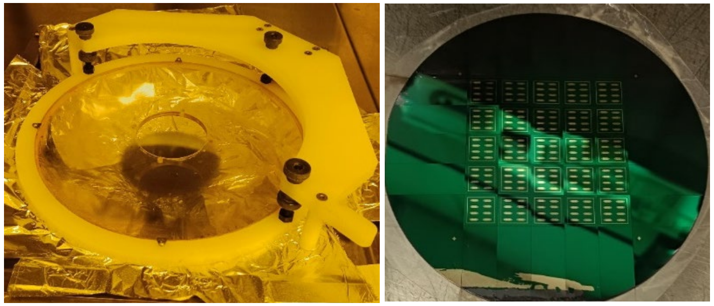
Remover PG / 18hrs



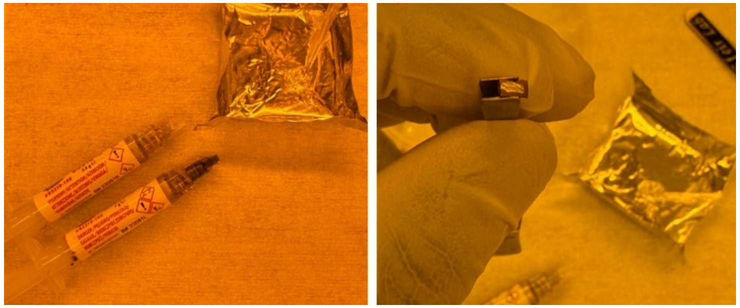
SiNW-sensor array

Dicing & Paste Preparation

Pre-Post-soft baking
Mir 701 photoresist



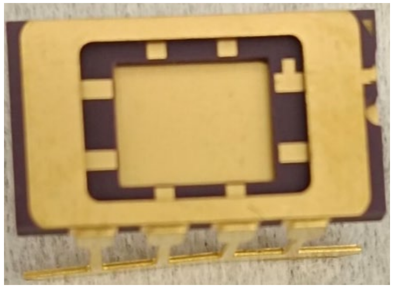
Photoresist coating and dicing of pattern



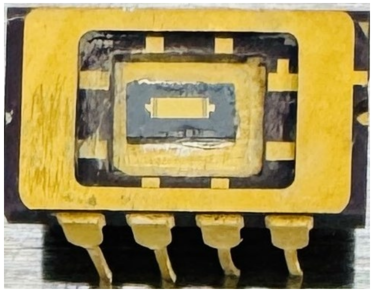
Silver –Epoxy Paste preparation

Packaging & Wire bonding

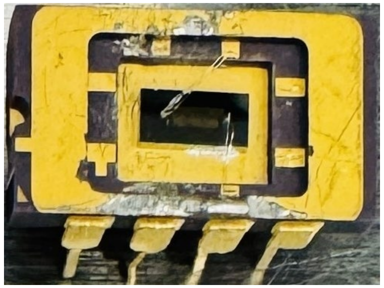
Silver –Epoxy Paste
Mount the chip



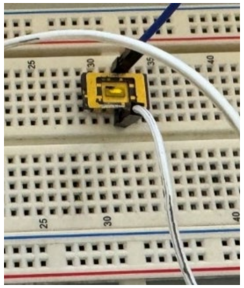
CDIP Chip carrier



Mount the chip

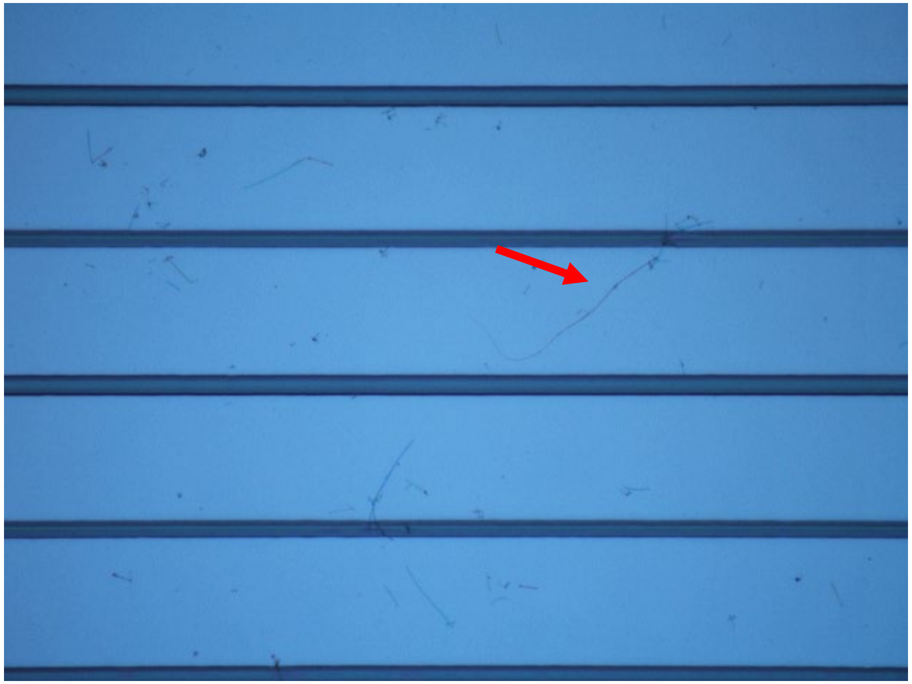


Wire-bonded device



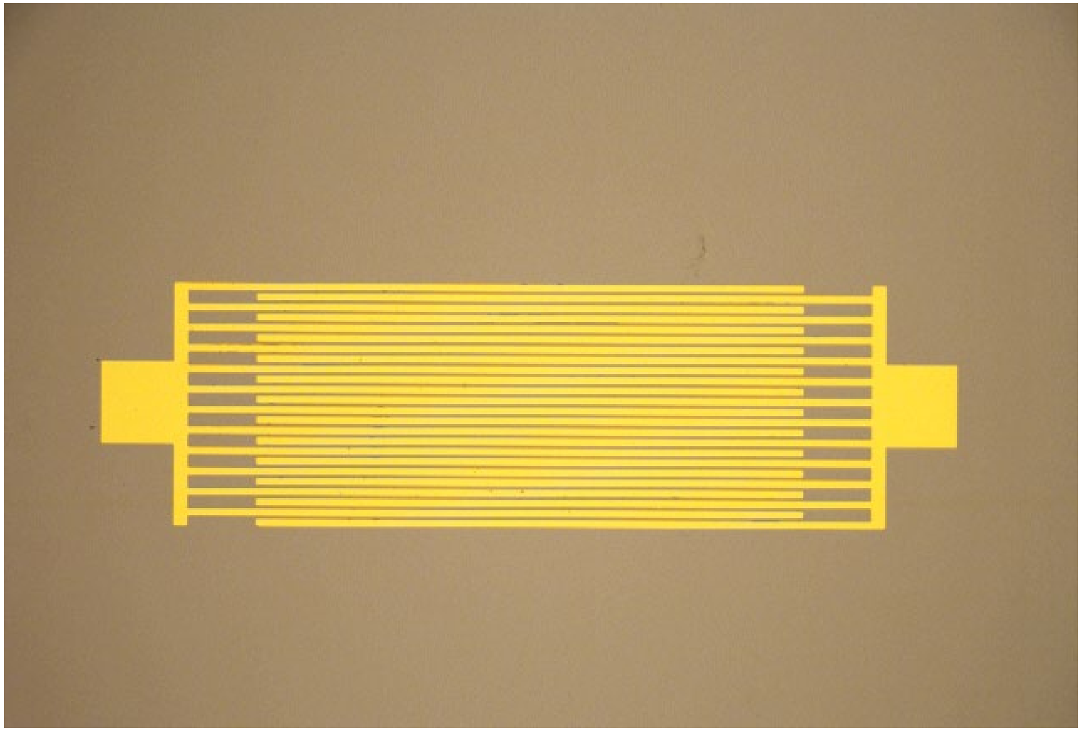
IV analysis of sensor chips

Microscopic Images of sensor chips



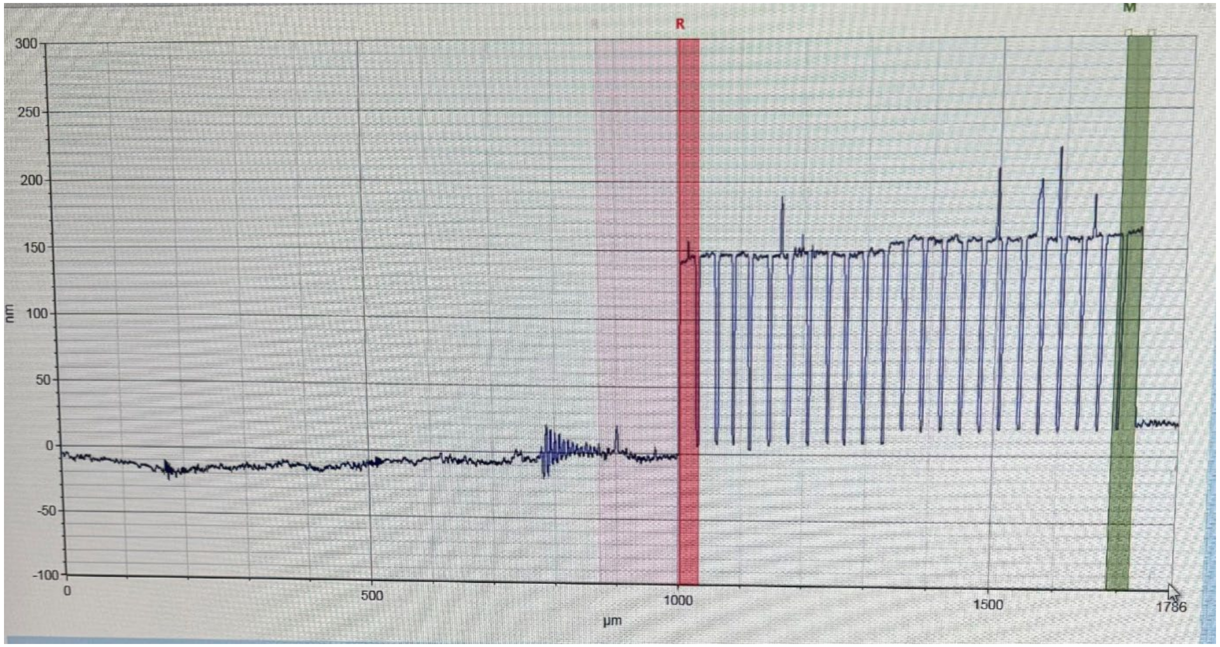
- The optical image shows the SiNW integrated sensor array before metal deposition.
- The patterns are well-defined, and the terminals are clearly visible and connected.
- The sensor array are well-defined, and the terminals are clearly visible.
- The senor array shows no visible defects, and the terminals remain clean.

Microscopic Images of sensor chips



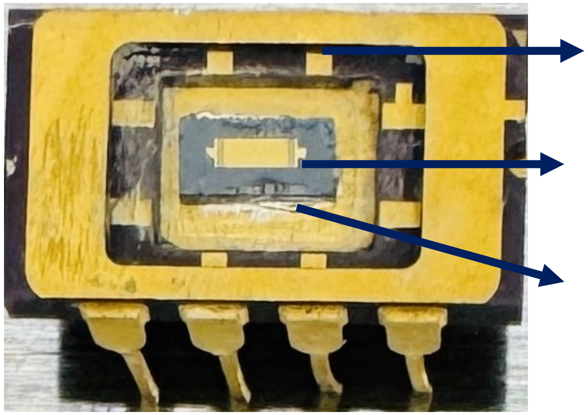
- Optical microscope images of SiNW-integrated sensor array after the metal lift-off.
- The SiNW is connected to both terminals, ensuring proper electrical continuity.
- The sensor array are well-defined, and the terminals are clearly visible.
- The senor array shows no visible defects, and the terminals remain clean.

Sensor Array Thickness Measurement Profilometer



- ❖ A diced sensor chip was used to analyze the thickness of the sensor array.
- ❖ A profilometer was employed to measure the average thickness of the sensor array.
- ❖ The average thickness of the sensor array was found to be 158nm.
- ❖ The thickness comprises 150nm of gold (Au) and 6nm of chromium (Cr) layers.

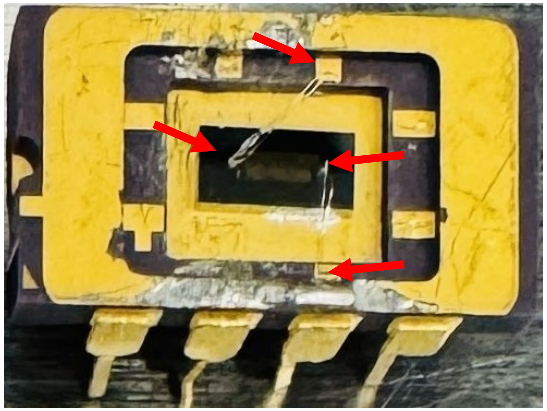
Packaging and wire bonding of Sensor Array



C-DIP carrier

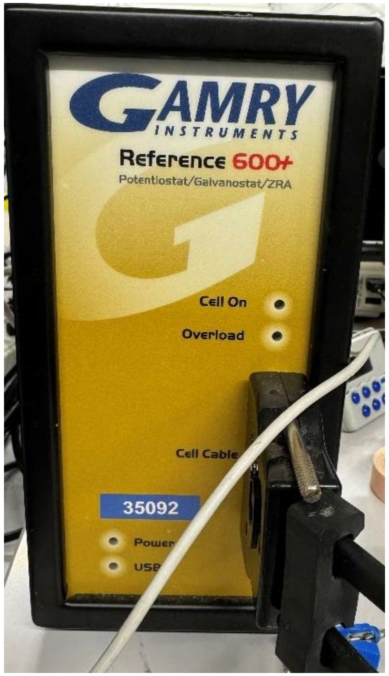
Sensor array

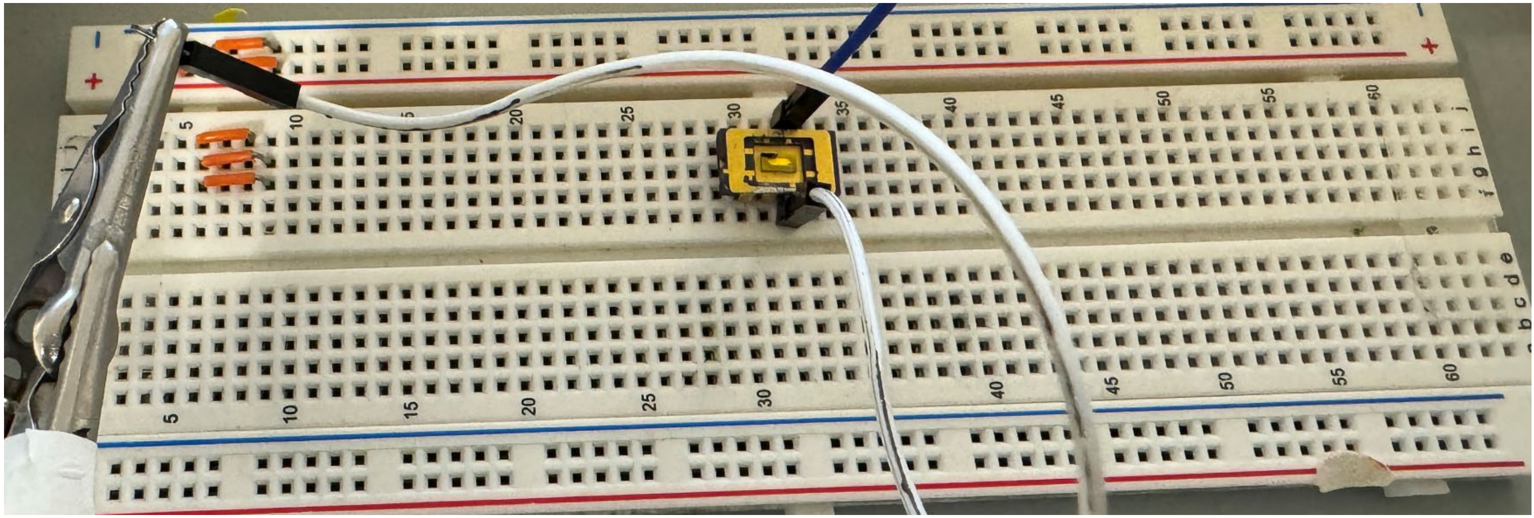
Silver epoxy paste

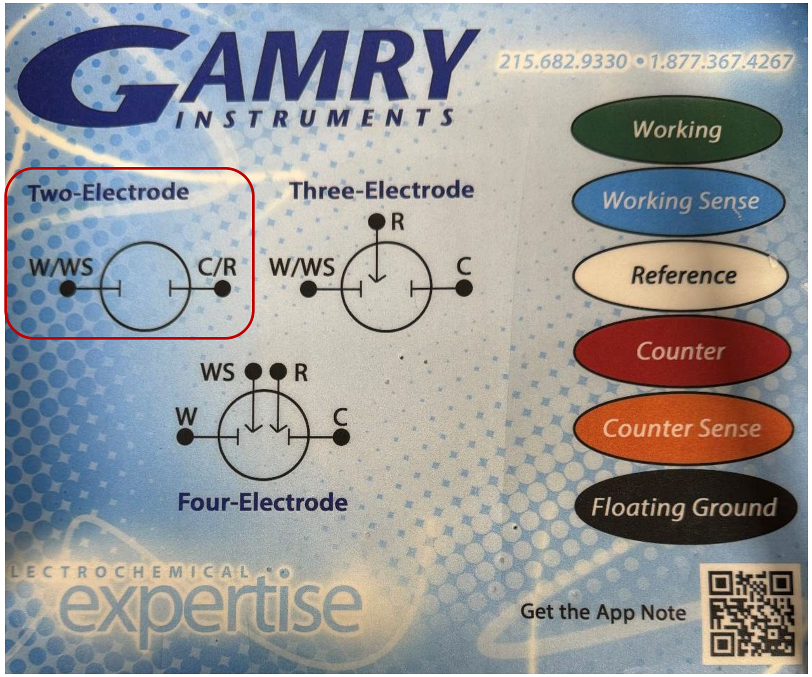


- The photographic image of the ceramic dual inline packaging (C-DIP) carrier
- The DIP carrier offers excellent electrical and mechanical stability.
- Ensuring robust performance and protection of sensitive components.
- The SiNW-integrated sensor array securely fixed on the C-DIP carrier.

IV measurement setup

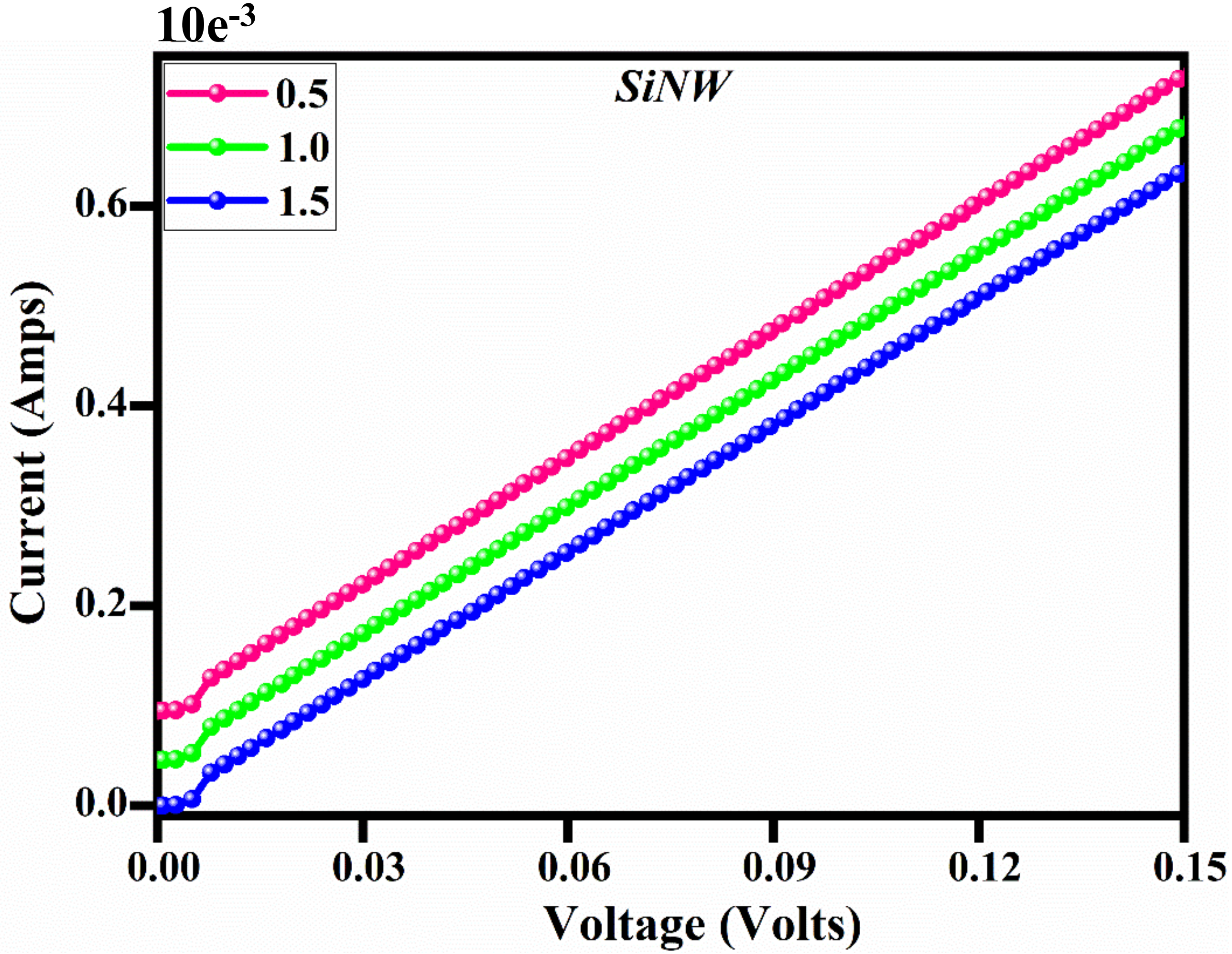






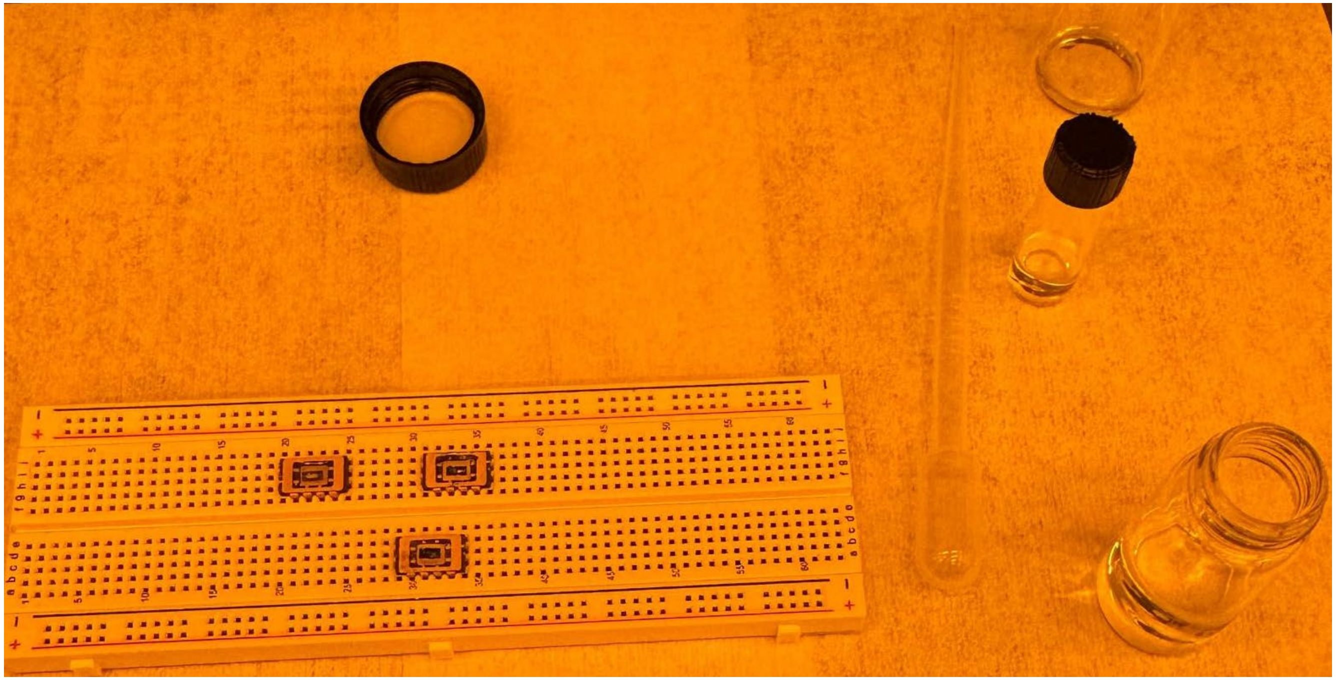
❖Two electrode method was used to analyze the electrical response of the sensor array

IV measurement of SiNW based sensor array



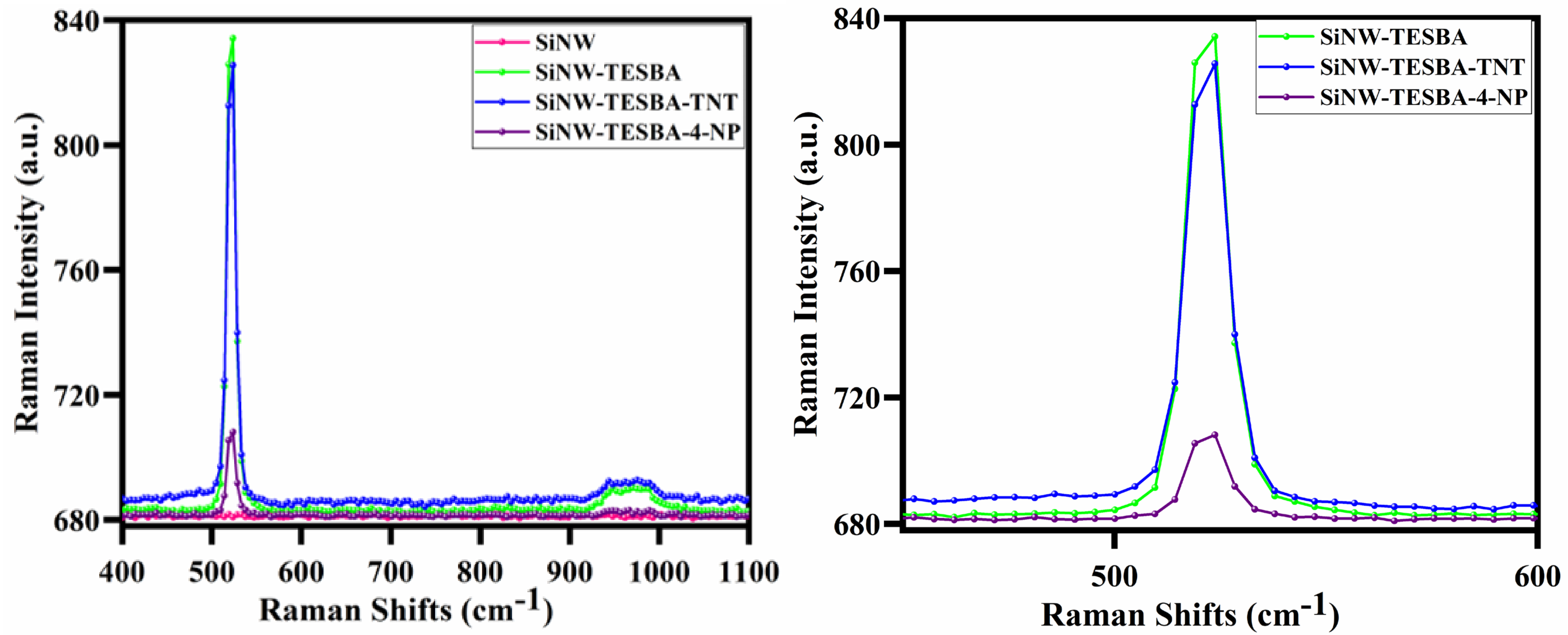
- The IV curve shows the electrical characteristics of the C-DIP SiNW integrated sensor chip under different scan rates.
- The data from the IV curves helps in understanding the electrical behavior, including current-voltage relationships and any potential non-linearities.

Surface functionalization of SiNW based sensor array



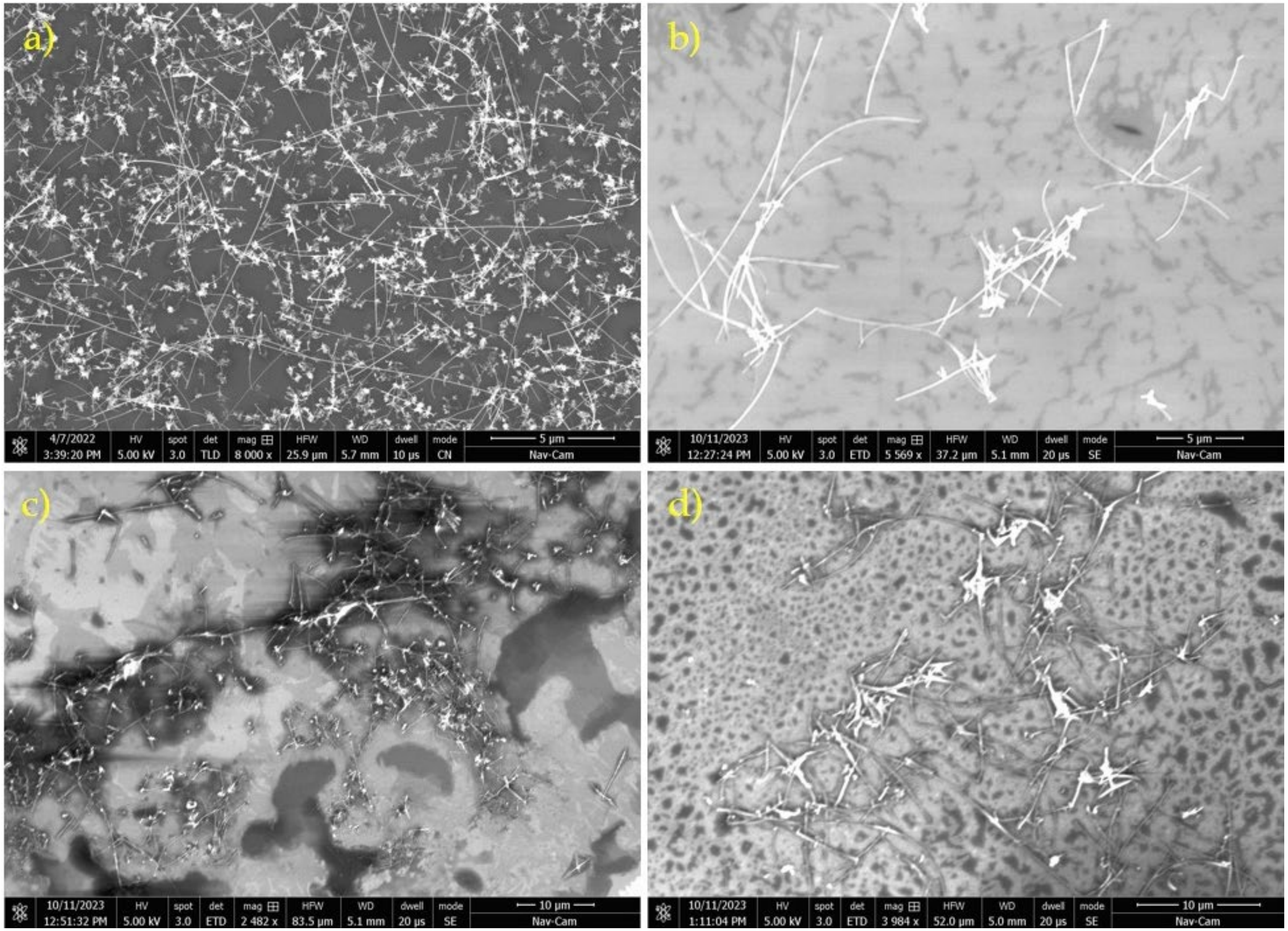
- The SiNW was functionalized with triethoxysilylbutyraldehyde (TESBA) via self-assembly through covalent interactions.
- The human anti-2,4,6-TNT recombinant antibody (anti-TNT) was immobilized onto the SiNW surface through covalent interactions.
- Sensitivity studies were conducted using 4-NP as the target detection molecule to evaluate the sensor's performance.

Raman Spectra of SiNW based sensor array



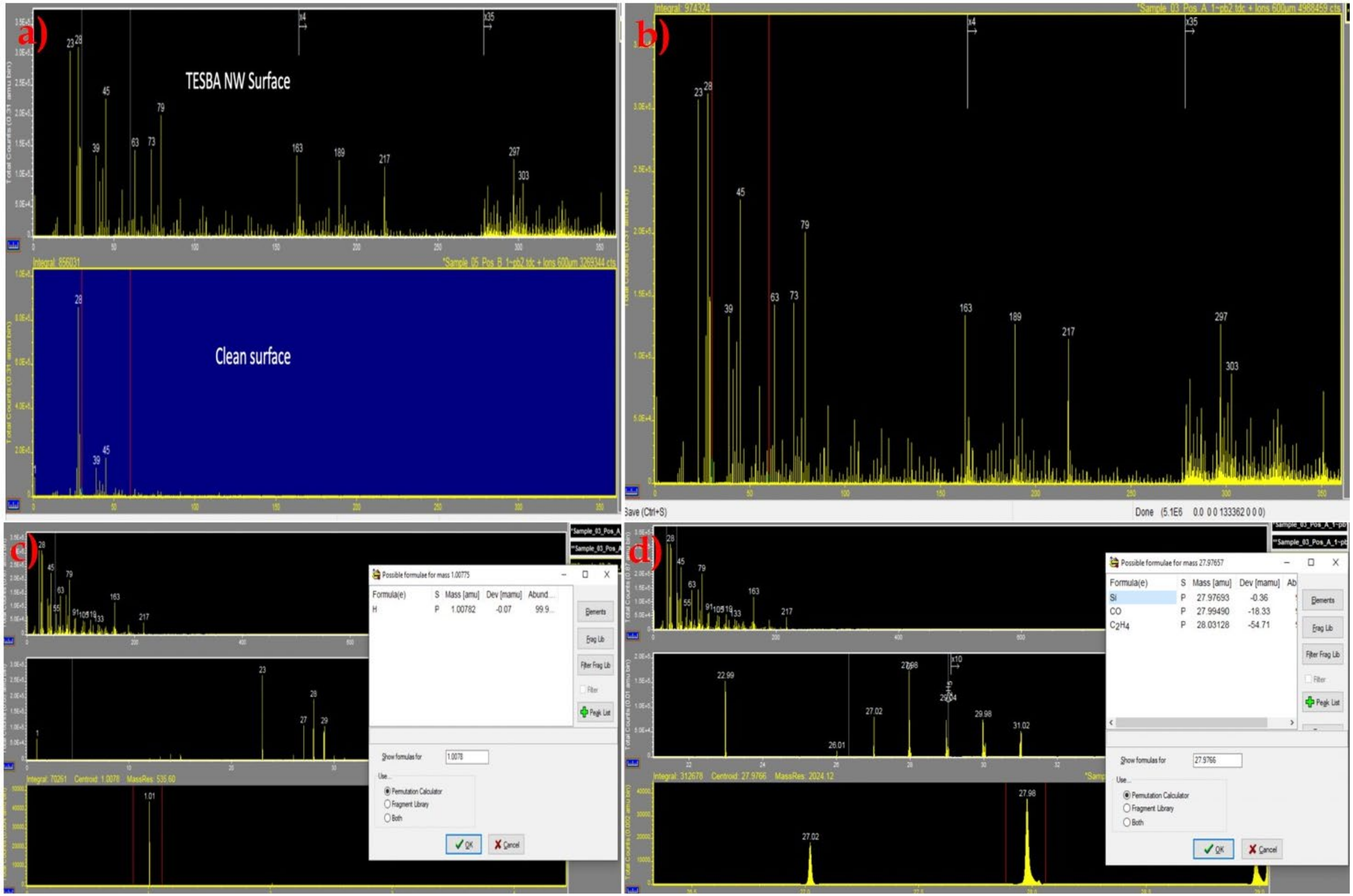
- ➢ The Raman spectrum of SiNW shows the characteristic peaks of unfunctionalized silicon nanowires.
- ➢ After functionalization, TESBA was covalently and self-assembled over the surface of the SiNWs.
- ➢ This interaction is reflected in the Raman spectra, showing changes in the spectral features.
- ➢ The TESBA- anti (TNT) conjugated SiNW shows the successful attachment of the TNT molecule.
- ➢ After the conjugation with TNT, the functionalized SiNW-TNT was used to detect 4-NP molecules.

FE-SEM images of SiNW based nanosensor



- ❖ The surface morphology and size of SiNW, SiNW-TESBA, and SiNW-TESBA-4NP were analyzed using a field emission scanning electron microscope.
- ❖ The wire-like structure has an average diameter of 50-80 nm and a length from 1.46 to 3.6 μm.
- ❖ This micrograph indicates that the nanowires are highly pure and free of impurities.

TOF-MS analysis of SiNW based sensor array



Possible formulae for mass 1.00775

Formula(e)	S	Mass [amu]	Dev [mamu]	Abund...
H	P	1.00782	-0.07	99.9...

Show formulas for 1.0078

Use...
● Permutation Calculator
○ Fragment Library
○ Both

Possible formulae for mass 27.97657

Formula(e)	S	Mass [amu]	Dev [mamu]	Ab
Si	P	27.97693	-0.36	
CO	P	27.99490	-18.33	
C_2H_4	P	28.03128	-54.71	

Show formulas for 27.9766

Use...
● Permutation Calculator
○ Fragment Library
○ Both

TOF-MS images of TESBA functionalized SiNWs, (a) TESBA functionalized SiNWs and clean surface of a silicon wafer, (b) TESBA functionalized SiNW, (c) hydrogen peak (total mass 1.007amu), and (d) silicon peak (total mass 27.97amu).

Summary

- **Silicon nanowires (SiNWs) were synthesized with p-type atoms to precisely control their conductivity and size.**
- **The SiNWs were functionalized with triethoxysilylbutyraldehyde (TESBA) using a self-assembly and covalent conjugation method.**
- **TESBA-functionalized SiNWs were conjugated with the TNT (antibody) via covalent linkages, enabling selective detection.**
- **The cleaning process for the SiNWs was highly labor-intensive, ensuring the removal of impurities and preparing the surface for functionalization.**
- **Current-voltage (IV) measurements were performed to verify the functionality and electrical response of the sensor.**
- **The SiNW-based nanosensor was packaged for hardware integration on the PCB board, making it ready for use in practical applications.**