ASE

Warpage Evaluation in Embedded Bridge Package for Advanced Package Solutions

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Outline

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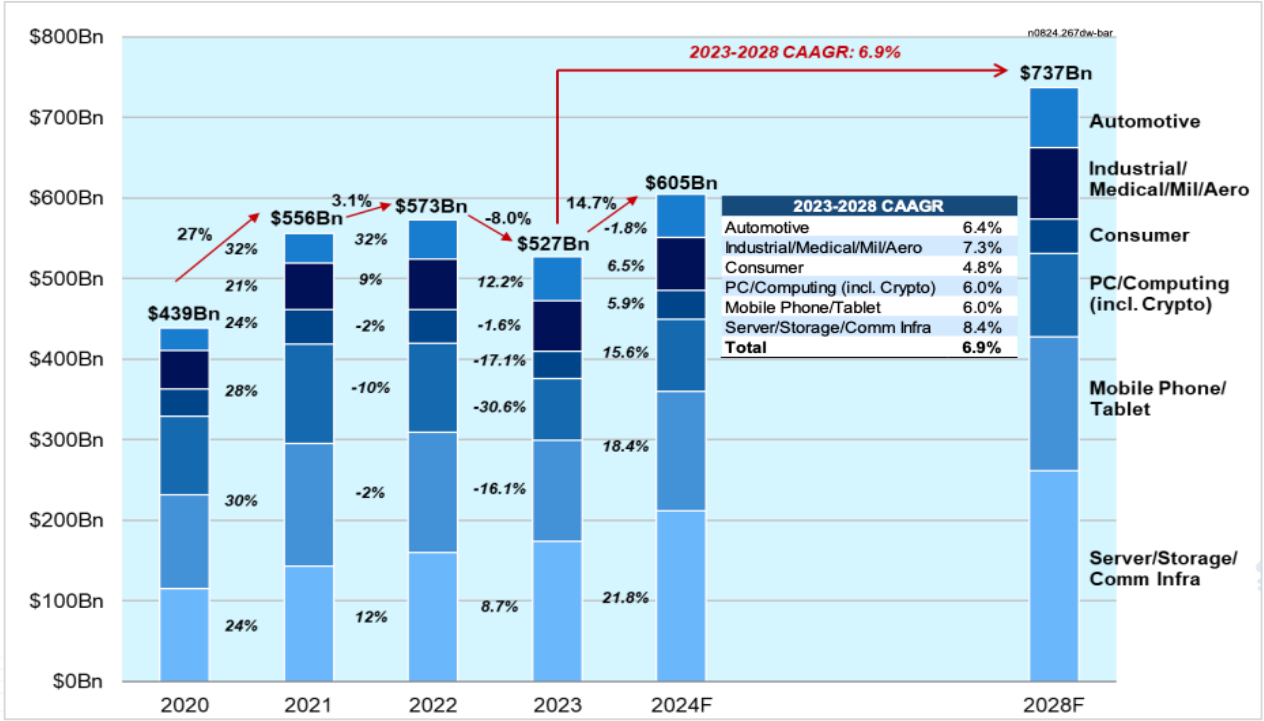
- **Advanced Embedded-Bridge Package development**
  - Embedded-Bridge Package Advantage
  - Embedded-Bridge Process Flow
  - Embedded-Bridge Key Challenges
  - Case study for Warpage evaluation
- **Conclusion**

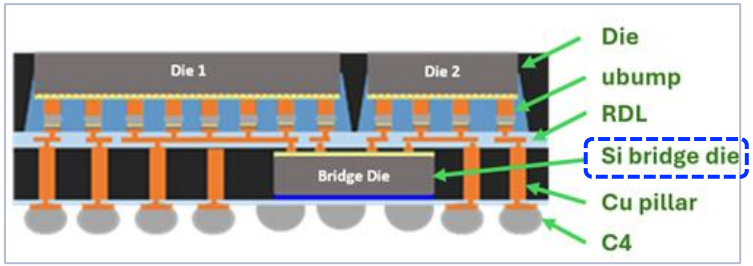
Semiconductor Market Trend

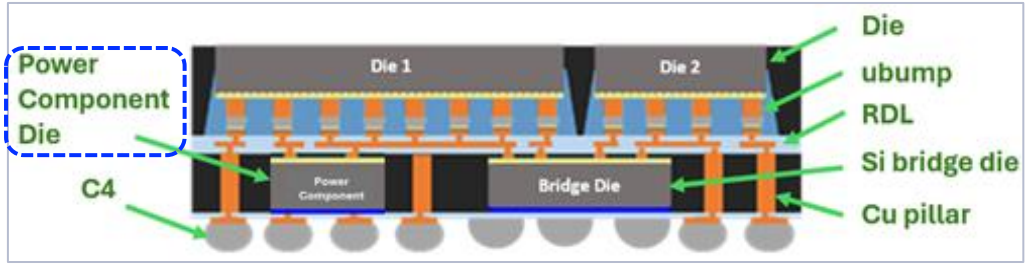
- High-end products (AI/HPC/ Networking/Auto…) shows strong growth in next 5 years
- Advanced packaging technology and chiplets heterogeneous integration are key enablers

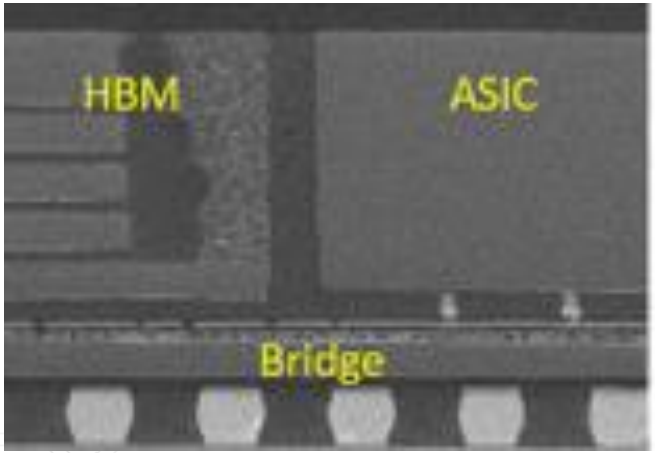


Source: Prismark 2024

Advantage of Embedded Bridge Packaging Technology



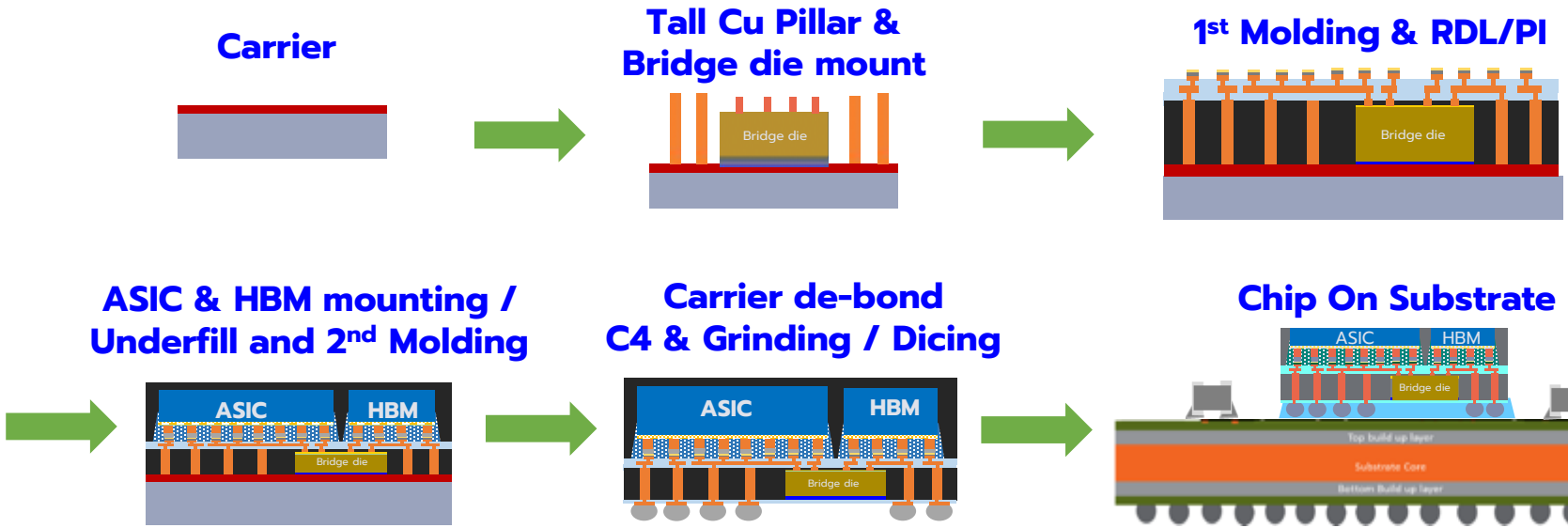




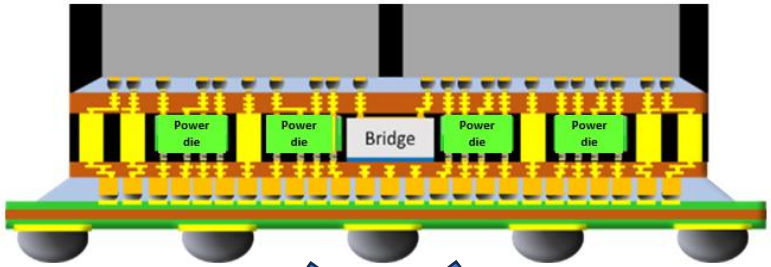
- Bridge dies can do the Die-to-Die connections directly.
- Bridge die can have the smaller L/S < 1um that's the high-density design to replace pure RDL layers.
- Power components are always embedded in advanced Pkg to enhance the power performance.

Process flow of FO Embedded Bridge Technology

➢ FOCoS-B Chip Last Embedded-Bridge Process Flow



Key Challenges for High-end Embedded Bridge technology



1. Larger FO/ Body Size Requirement

- More chiplets and diverse components:
  - Large ASIC die size
  - Large FO reticle size >5.5x
  - More HBMs
  - Embedded dies (IPD, DTC…)

2. Larger Warpage

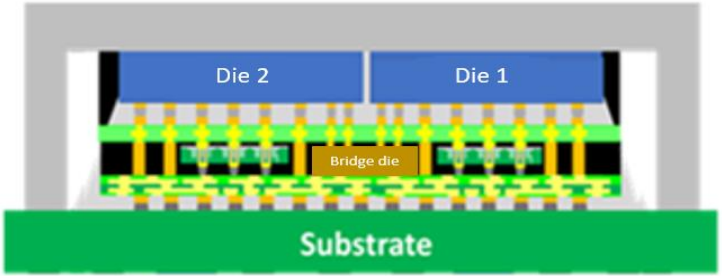
- CTE mismatch with different material properties
- It requires optimization:
  - Pkg platform structure design
  - BOM selections
  - Process routing/recipe optimizations

Warpage & Stress Analysis - Case Study

➢ Test Vehicle information

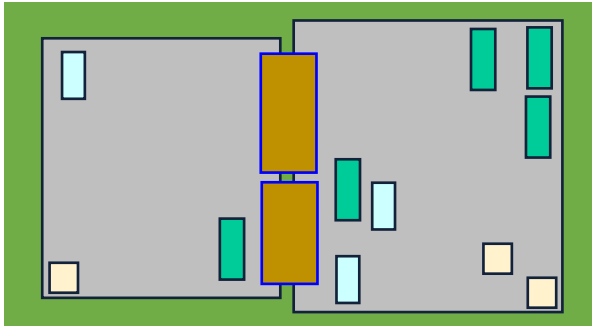
Package size	2925 mm2
FO size	865 mm2
Die 1 size	23*16 mm2
Die 2 size	26*13 mm2
Bridge die 1 size	3*12 mm2
Bridge die 2 size	3*10 mm2

Power component	Matrix die
Matrix die 1x1	1.4*1.4mm2
Substrate	8L (3/2/3)
Lid type	1pc forging lid



➢ Package structures DoE study

DoE study		1st	2nd	3rd	4th
Bridge Die		2 pcs	2 pcs	2 pcs	2 pcs
Power component	1x1 Matrix	---	3 pcs	---	---
	1x3 Matrix	---	---	3 pcs	---
	1x4 Matrix	---	---	---	5 pcs



*Bridge die
: 2pcs (3*12 & 3*10mm2)

*Power component
: 3pcs (1x1 Matrix)
: 3pcs (1x3 Matrix)
: 5pcs (1x4 Matrix)

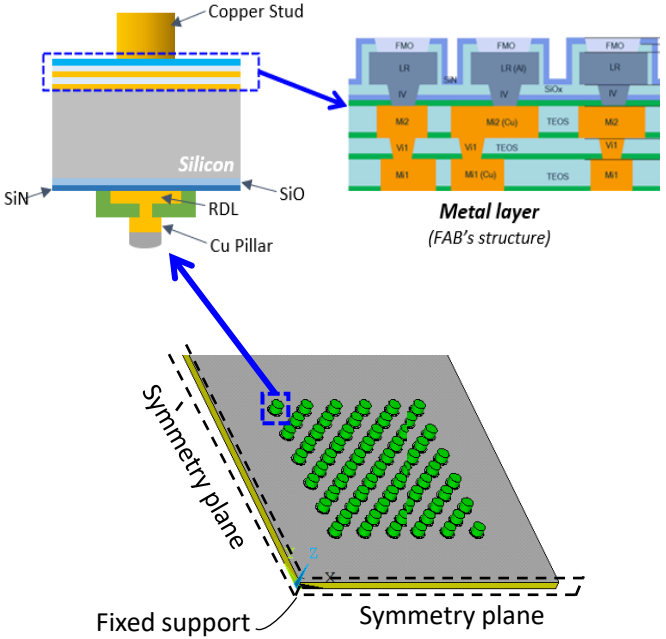
Warpage & Stress Analysis - Case Study

Simulation for Power Component

- Material properties of power components are listed as below table.
- Temperature change follows mass reflow conditions for FCB process.

Components	Type	Modulus (GPa)	CTE (ppm/°C)	Poisson's Ratio
Si	Silicon	131	2.8	0.27
FAB's structure assumption	Metal	117	16.9	0.3
	USG	70	0.50	0.3
ILD	SiOx	70	0.48	0.3
	SiN	225	3.2	0.3

FEA modeling X-Section



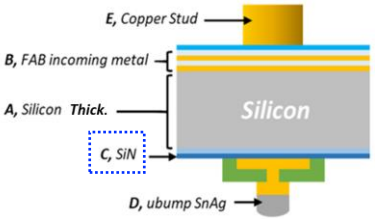
Boundary condition

Warpage & Stress Analysis - Case Study

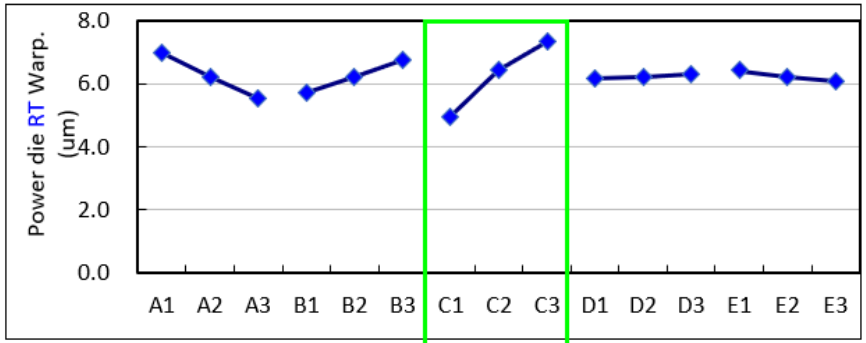
➢ Simulation for power component

- Power components warpage @25℃ & @260℃.
- HT warpage: Critical factors are identified as:
  - #1: SiN thickness (C).
  - #2: Fab metal total thickness (B).
  - #3: Silicon thickness (A).

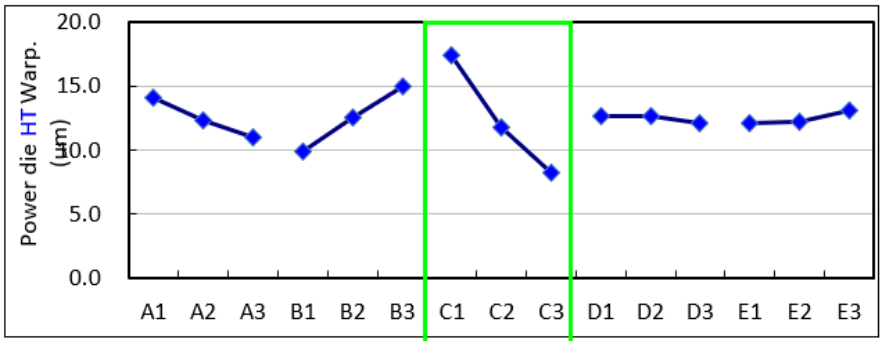
Factor	Item	Level 1	Level 2	Level 3
A	Silicon thk (um)	40	42.5	45
B	FAB metal thk (um)	8	10	12
C	SiN thk (um)	0.7	1.0	1.2
D	BS SnAg thk (um)	21.5	25	28.5
E	FS Cu stud thk (um)	40	66	80



Response Chart



	Silicon thk	Metal thk	SiN thk	BS SnAg thk	Cu stud thk
Effect	1.40	1.04	2.41	0.16	0.34
Rank	2	3	1	5	4

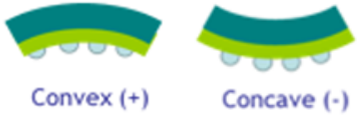


	Silicon thk	Metal thk	SiN thk	BS SnAg thk	Cu stud thk
Effect	3.13	5.01	9.13	0.58	1.09
Rank	3	2	1	5	4

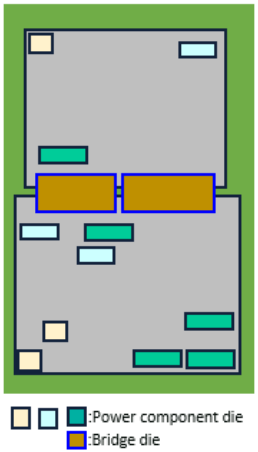
Warpage & Stress Analysis - Case Study

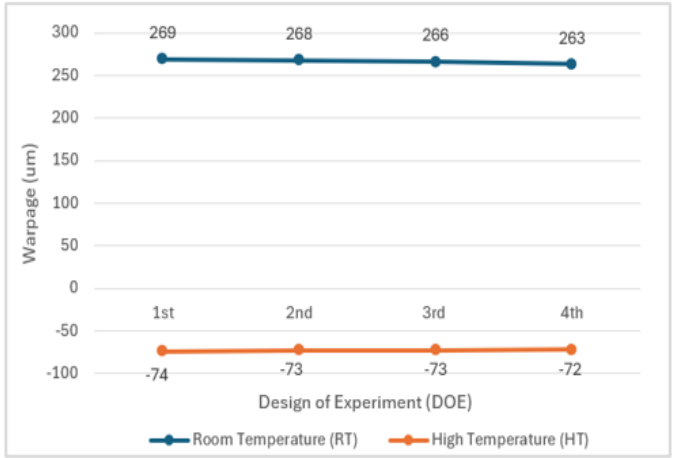
➢ Simulation results of DoE study

DoE study	1st	2nd	3rd	4th
FOM Warpage @RT & HT (um)	+269 / -74	+268 / -73	+266 / -73	+263 / -72
PKG Warpage @RT & HT (um)	-211 / +128	-211 / +128	-211 / +128	-211 / +128

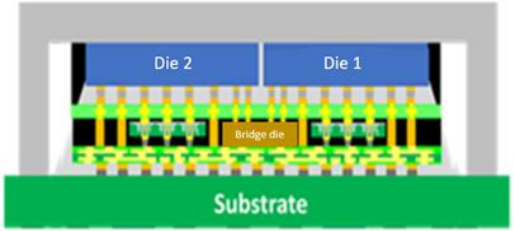


FOM Warpage





PKG Warpage

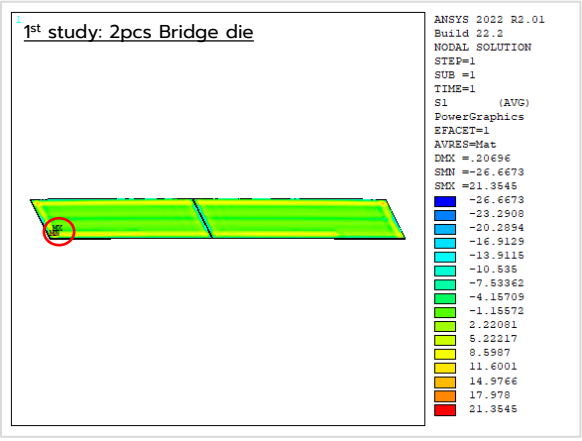


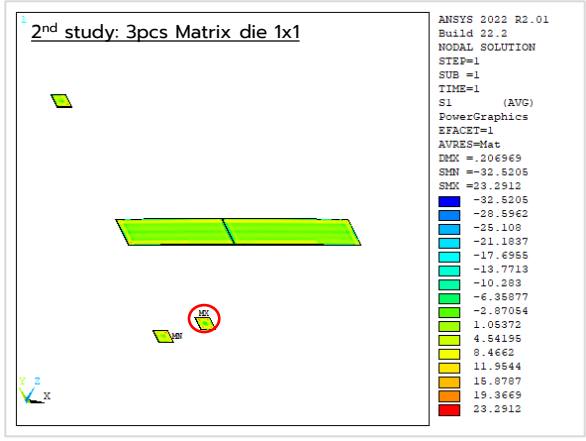
- No impact embedded bridge configurations on FO module warpage in both RT and HT.
- PKG warpage are also comparable.

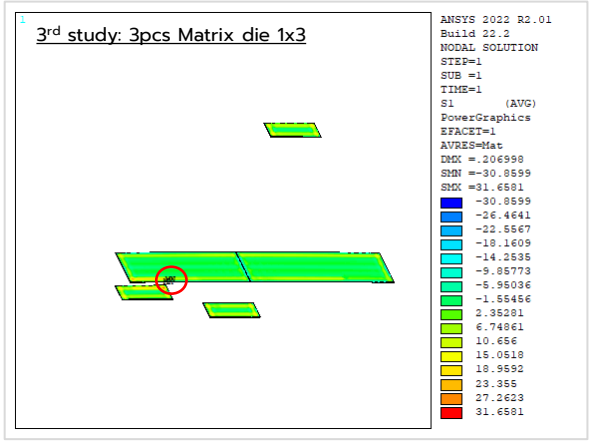
Warpage & Stress Analysis - Case Study

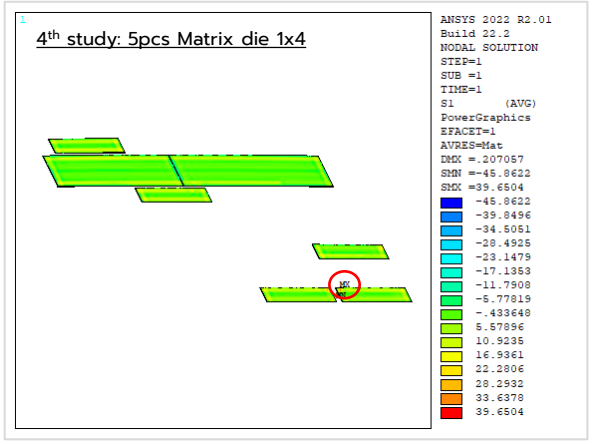
➢ Simulation results of DoE study

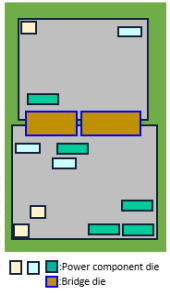
DoE study	1st	2nd	3rd	4th
Bridge die / Power component Stress (MPa)	21.35	23.29	31.66	39.65



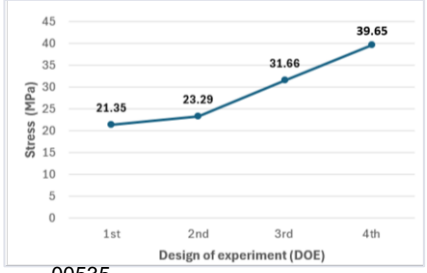








- Power module size and count increase with the stress levels rise significantly.
- The highest stress observed in the 4th DOE lot , reaching 39.65 MPa.



Conclusion

- Advanced FO Embedded Bridge packaging technology has become a key enabler for chiplet integration for HPC / AI application.
- Warpage and stress have shown a significant impact on FO embedded bridge configurations with varying power module designs
- With the size and number of embedded power modules increase, stress levels rise significantly, especially near the corners of the FO module.
- Effective design and simulation from device to system level are crucial to reducing warpage and stress in chiplet integration with advanced FO embedded bridge packaging.

~ Thank you very much ~

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