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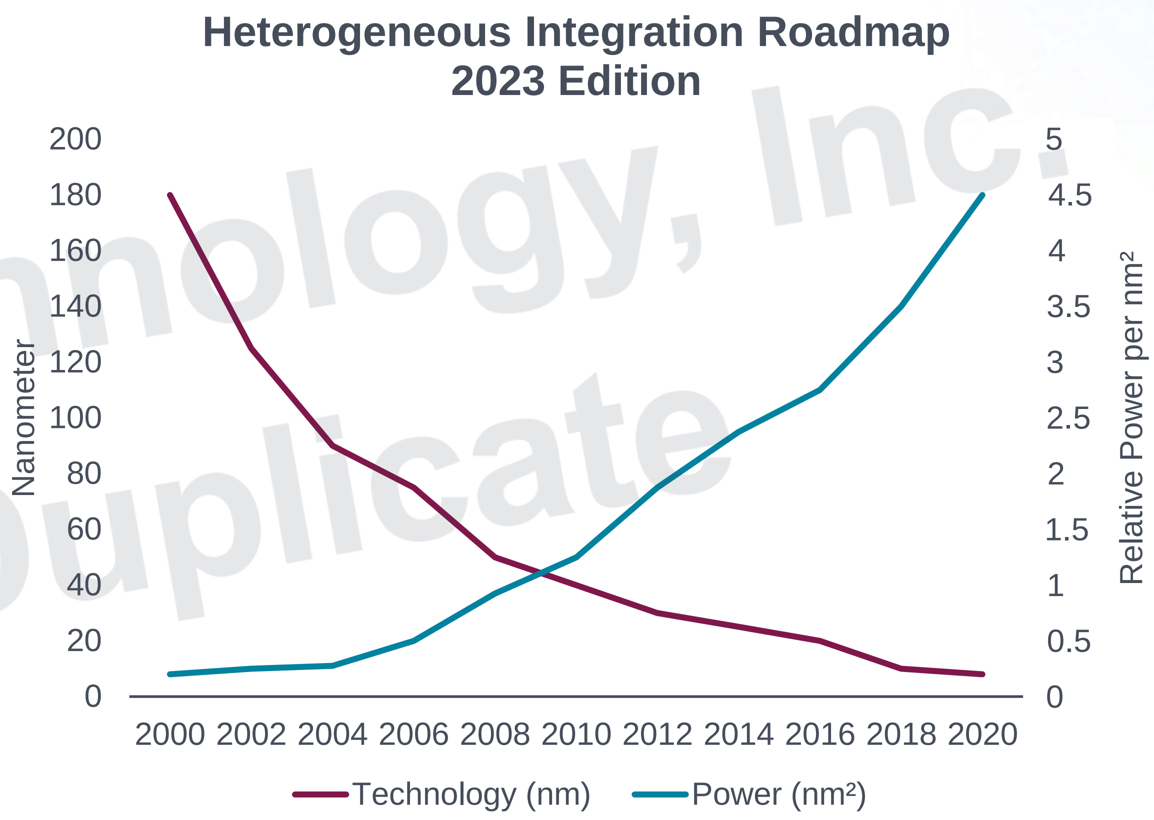
Novel Package Structure for Enhancing Power Integrity Performance & Cost Efficiency

MinWon Park l Director, Process/Material Research

Agenda

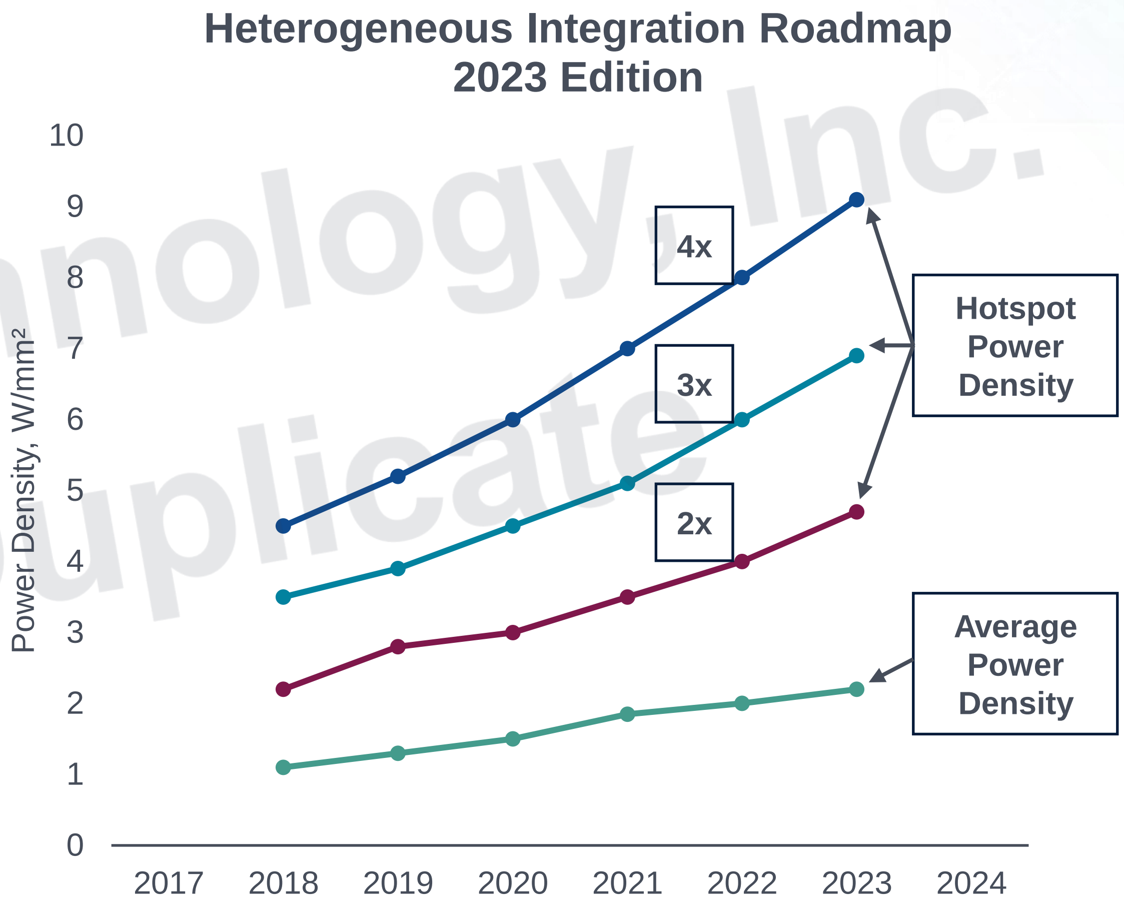
Importance of Power Integrity in Modern Electronics

- Miniaturization of components
  - As frequency increases, for signal processing and power consumption efficiency
- Increased functionality
  - Functional integration in small form factor pkg
- Improved sensitivity of integrated circuits to power fluctuations
  - Multiple power supplies ensure stable and consistent signal processing
- Enhances reliability and EMC compliance
  - High-frequency applications increased and miniaturized electronic devices become more densely integrated



Power Integrity Requirements in Modern Packages

- Optimization of Power Delivery Network (PDN) design
  - Maintaining low PDN impedance and minimizing voltage drops is essential, requiring electrical simulations from the early stages of design
  - Advanced components with multiple power rails need parallel regulators and feedback loops to ensure stable voltage output
- Support for high speed and high-performance packages
  - To support high speed signals and high-power consumption, the wiring length within the package must be minimized, and both power and signal integrity must be managed effectively
  - Technologies like silicon interposers or Embedded Multi-die Interconnect Bridge (EMIB) improve die-to-die connectivity
- Requirements for multi-die and 3D packaging
  - Multi-die integration demands the ability to handle high power consumption (up to 1kW) while also addressing noise coupling and thermal management
- Utilization of simulation and verification tools
  - Tools such as Ansys SIwave and Cadence Sigrity are used to comprehensively verify Power Integrity (PI), Signal Integrity (SI), and Thermal Integrity (TI)



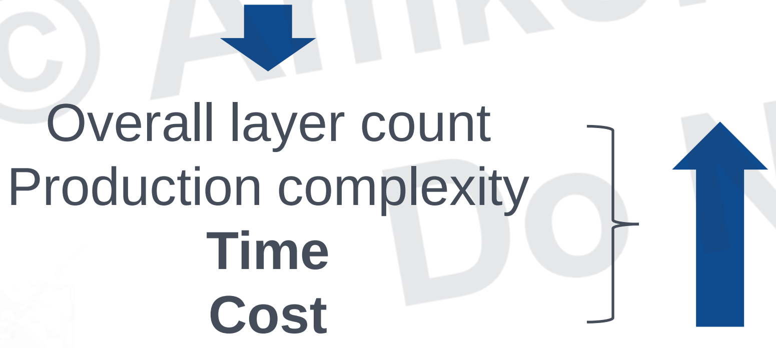
Why Power Integrity Is Important

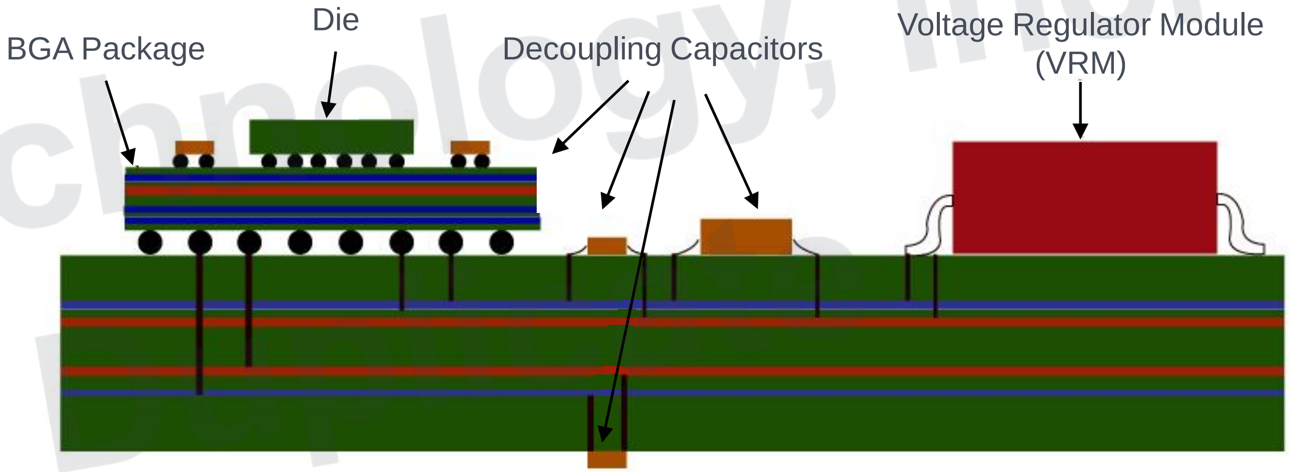
System Instability	Degraded Component Performance and Failures	Signal Integrity Issues	EMI Issues
▶ Unpredictable behavior of critical components ▶ Compromised usability and stability	▶ Overheating or damage to components ▶ Shortening the overall lifespan of the board	▶ Data transmission errors ▶ Loss of information and system failures ▶ Signal distortion and malfunction	▶ Interference with nearby electronic components and systems ▶ Generation of unwanted electromagnetic fields

Optimize PDN Design

Flip Chip Packages

- Importance of flip chip molded packages
  - Offer high performance and compact solutions
- Challenges of traditional flip chip packages
  - Increasing demand for higher power integrity and cost-effective manufacturing
  - Multiple internal metal layers required





Source: What is Power Integrity and PDN? I Sierra Circuits

- Objective of the proposed design
  - Simplify the package architecture
  - Reduce the layer count

Challenges With Traditional Flip Chip Packages

Complex Architecture

- Utilizing multiple internal metal layers to route power and ground connections, leading to increased layer count and fabrication complexity

Power Integrity Issues

- High current densities leading to voltage drops and signal integrity degradation

Cost-effective Manufacturing Challenges

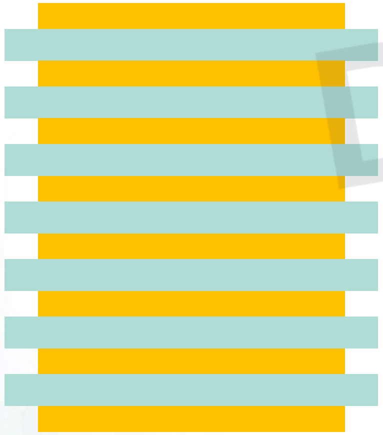
- The need to reduce production costs while maintaining high performance

Thermal Management Concerns

- Difficulty in dissipating heat generated by the high-power density

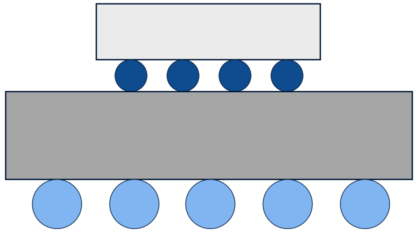
Current Solutions

- Multilayer substrates
  - **(+)** Reduces PDN impedance and enhances power integrity
  - **(-)** Increases manufacturing complexity, production time and cost



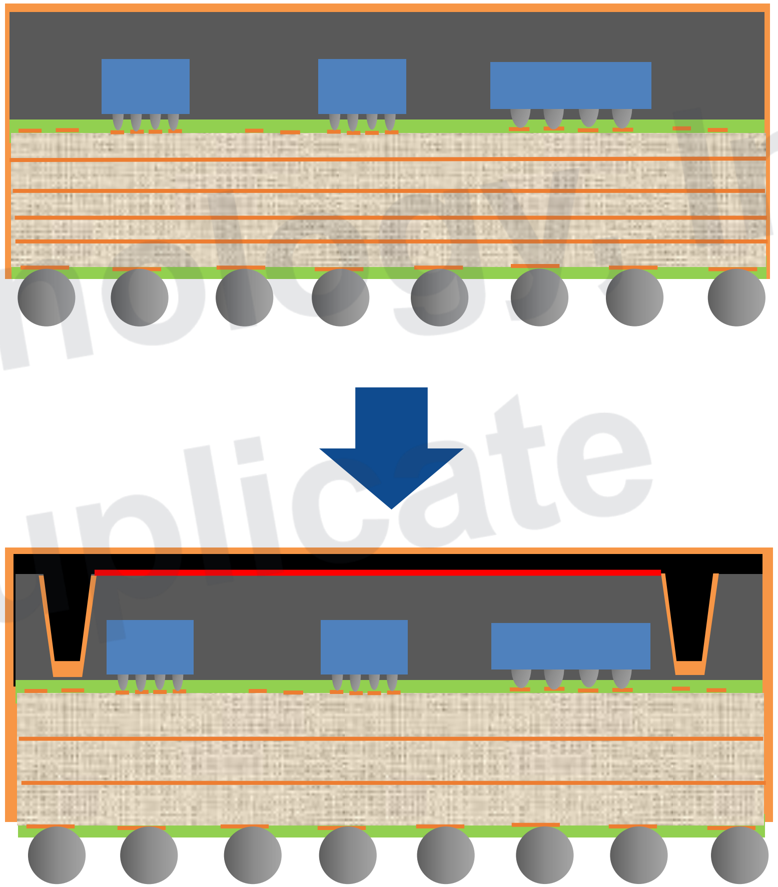
- On chip power integrity solutions
  - **(+)** Considering the entire power delivery system, including the package and PCB, to enhance power integrity
  - **(-)** Increases design complexity and incur design and manufacturing costs

- Flip chip bump interconnects
  - **(+)** Direct electrical path between die and substrate, reduces the power delivery network and minimizes parasitic R & L
  - **(-)** Increases production complexity and cost due to precise bump placement and alignment

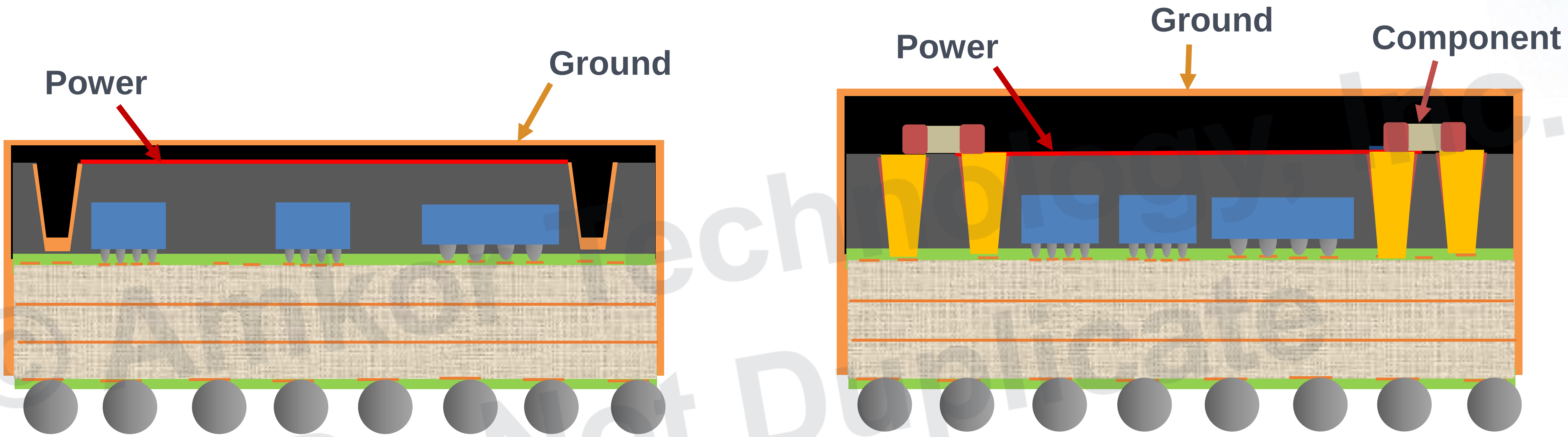


Proposed Solution

- Simplify architecture
- Enhance power integrity
- Optimize impedance
- Increase manufacturing efficiency



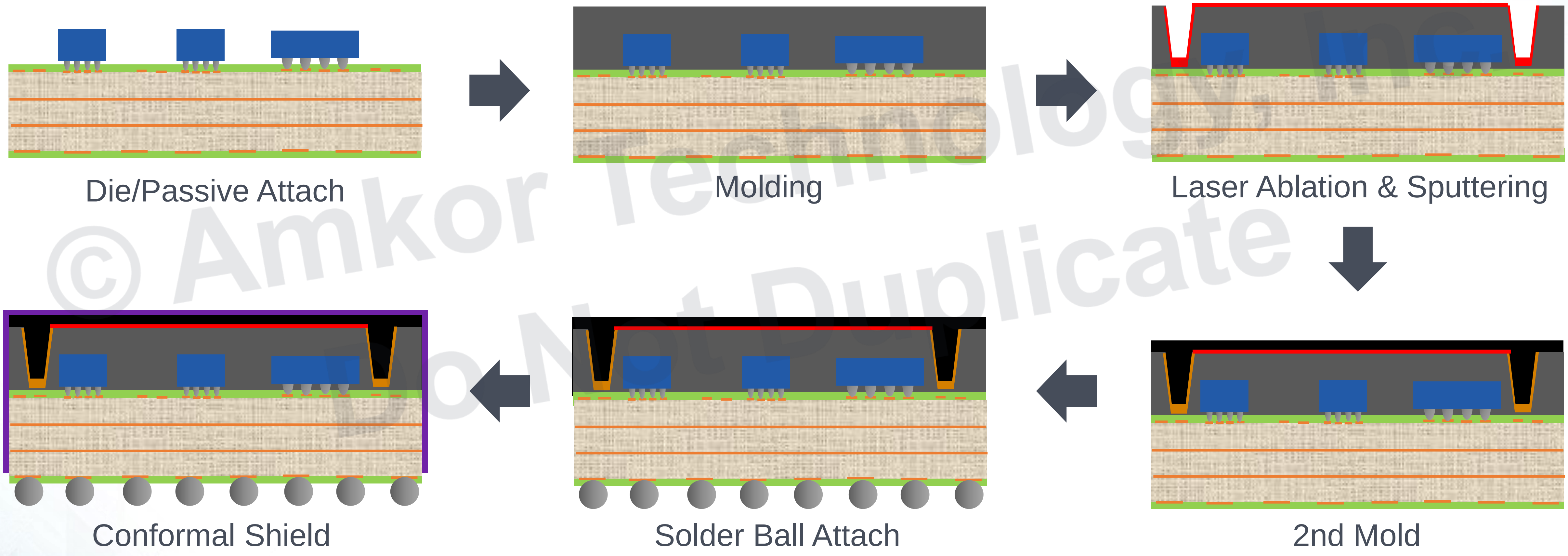
Design Details



- Overcome spatial constraints
- Higher capacitance between power and ground planes
- Reduce layer count while maintaining excellent power integrity performance

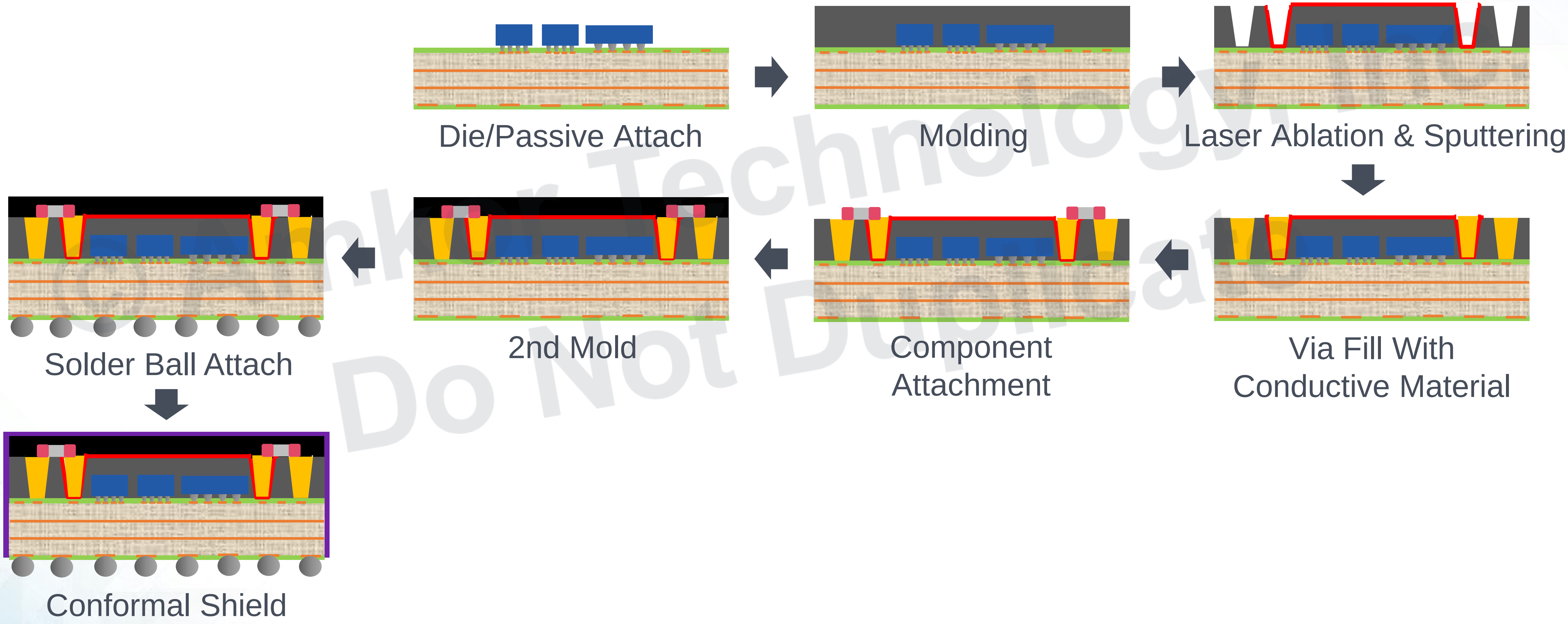
Implementation Process: Power Plane on Mold Layer

Power Plane on Mold Layer

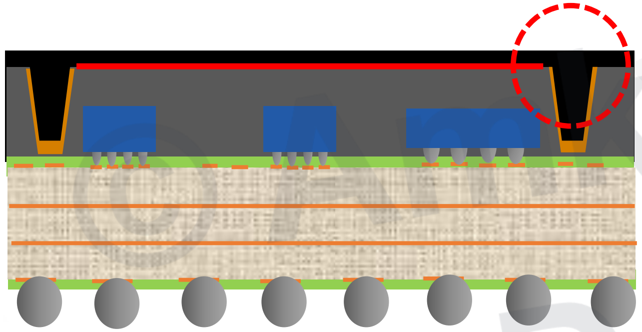


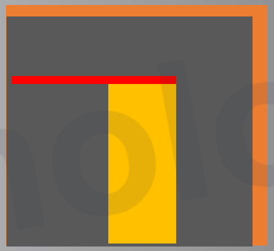
Implementation Process: Component Attached Structure

Component Attached Structure



Electrical Connection Methods

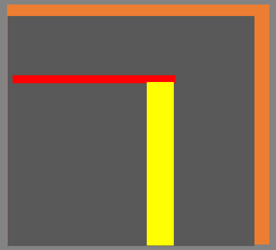




Option 1: Cu Post (CCC) & Sputter

Option 2: Solder & Sputter

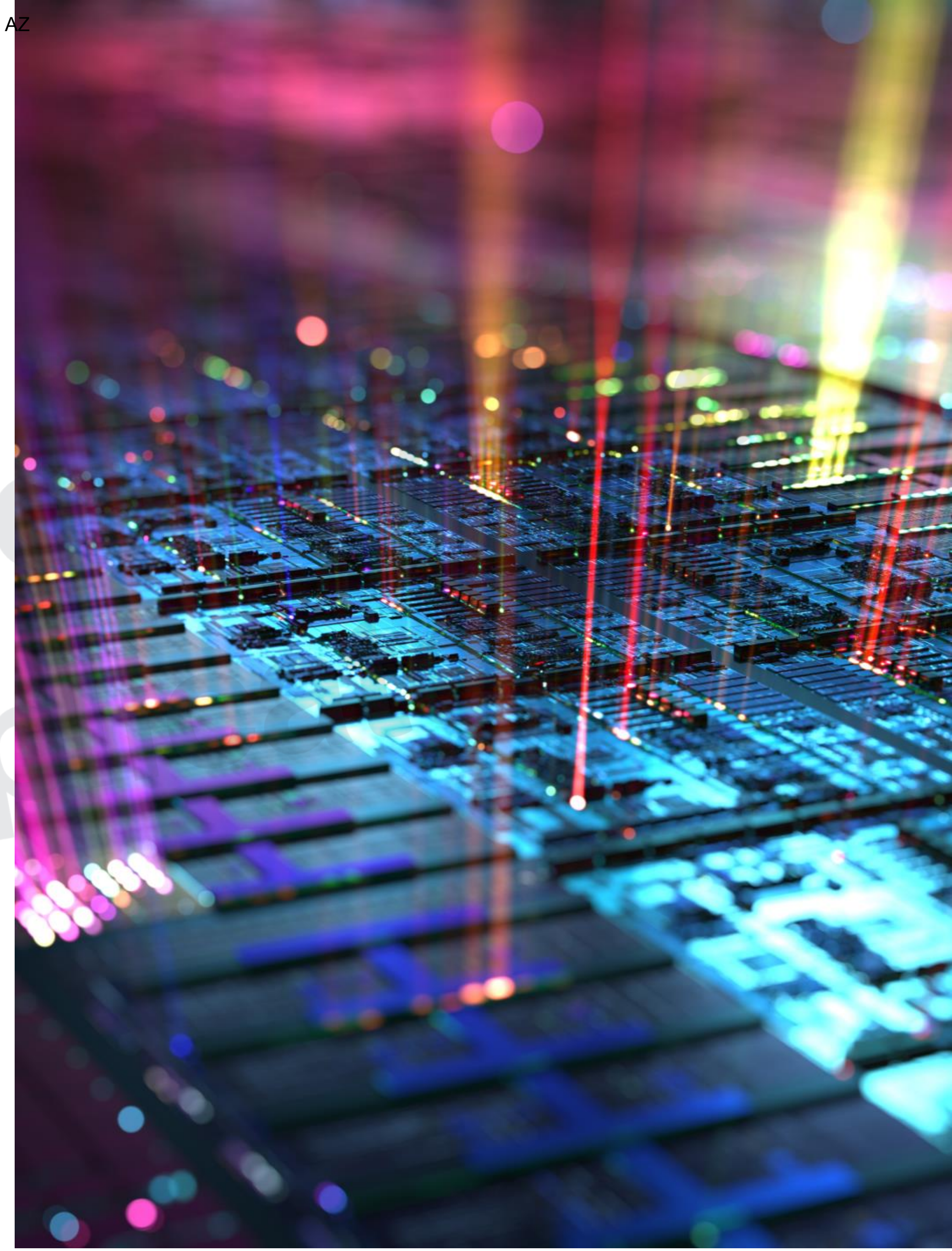
Option 3: Stacked Bump



Option 4: Vertical Wire

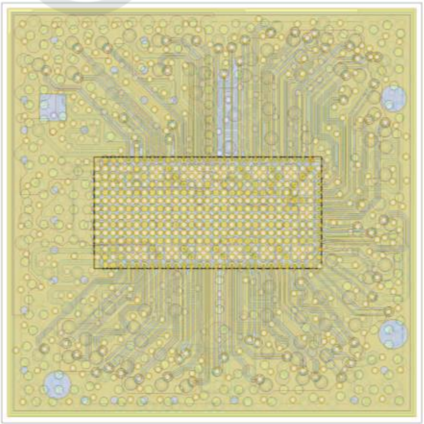
Key Benefits of Novel Structure

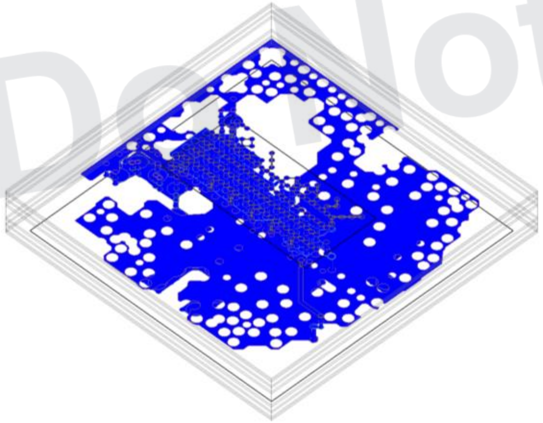
- Reduces layer count
  - Simplifies package architecture
  - Lowers production complexity and cost
- Optimizes impedance characteristics
  - Lowers parasitic inductance and resistance
  - Maintains efficient power delivery in high-frequency applications
- Enhances capacitance
  - Overcomes spatial constraints
  - Increases inherent capacitance between power and ground planes
  - Acts as a built-in decoupling capacitor
- Improves manufacturing efficiency
  - Reduces material usage
  - Less processing steps
  - Shorter production time



Simulation Conditions

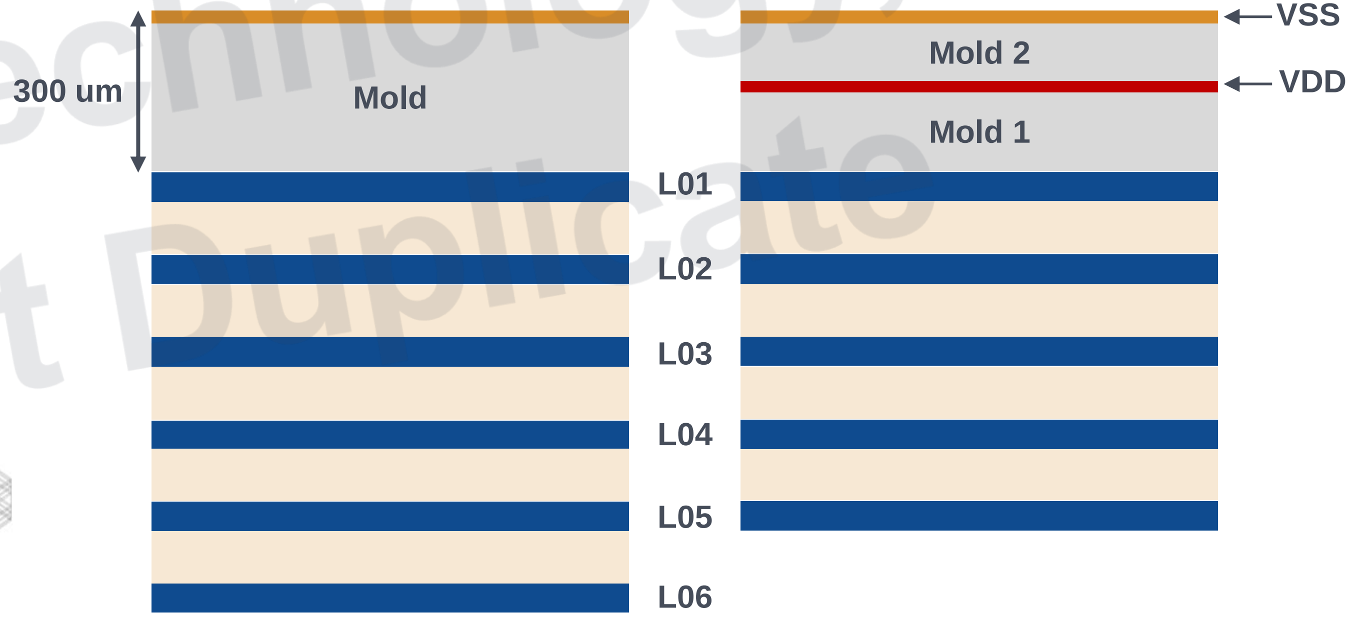
- Simulation tool: Ansys SIwave 22R2
- Analysis frequency: 0~1 GHz
- Package type: fcCSP
- Body size: 7 x 7
- Ball count: 169
- Application: HPC





Stack Up Information

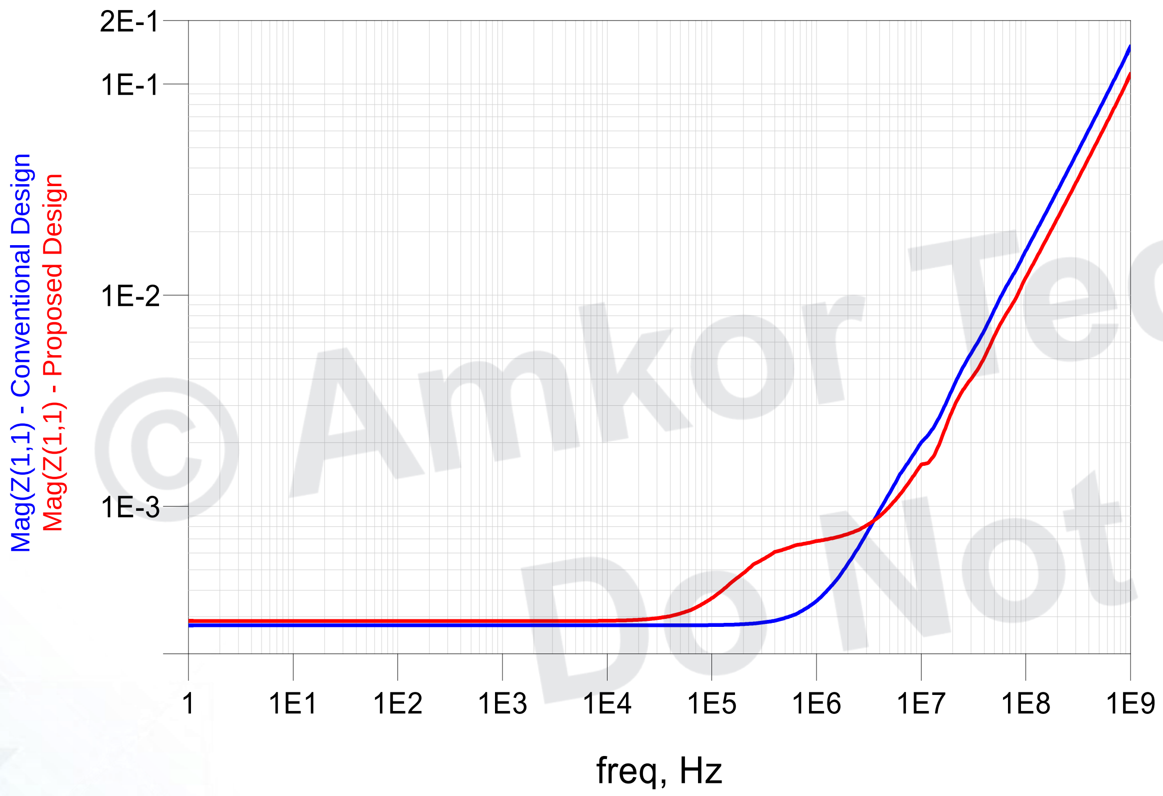
Conventional Design | Proposed Design



Total Thickness: 641 µm

Total Thickness: 618 µm

Simulation Results



Parameter	Conventional Design	Proposed Design	Δ (%)
DC Resistance	0.1121 mΩ	0.1131 mΩ	+0.0010 mohm (0.88%)
AC Resistance	2.426 mΩ	2.265 mΩ	-0.161 mohm (6.64 %)
Loop Inductance	0.025 nH	0.019 nH	-0.006 nH (24%)
Capacitance	40.83 pF	65.02 pF	+ 24.19 pF (59.25%)

Conclusion

- Summary of proposed design
  - Novel approach for flip chip packages
  - Power and ground planes on mold layer
- Key benefits
  - Reduced layer count while maintaining excellent power integrity performance
  - Enhanced capacitance and loop inductance
  - Manufacturing and cost advantages
- Simulation results
  - Comparable DC resistance
  - Improved AC resistance, inductance and capacitance
  - Similar impedance characteristics to traditional designs
- Future work
  - Further optimization of the design
  - Verification feasibility in actual processes
  - Exploration of wider application possibilities

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Thank You