LODX

METALLIZATION OF HIGH-ASPECT RATIO VIAS ON ADVANCED IC-SUBSTRATES USING A NOVEL LIQUID METAL INK

IMAPS DPC | March 4th, 2025

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1. LQDX's metallization technology for ultra fine lines and vias (LMI$_x$®)
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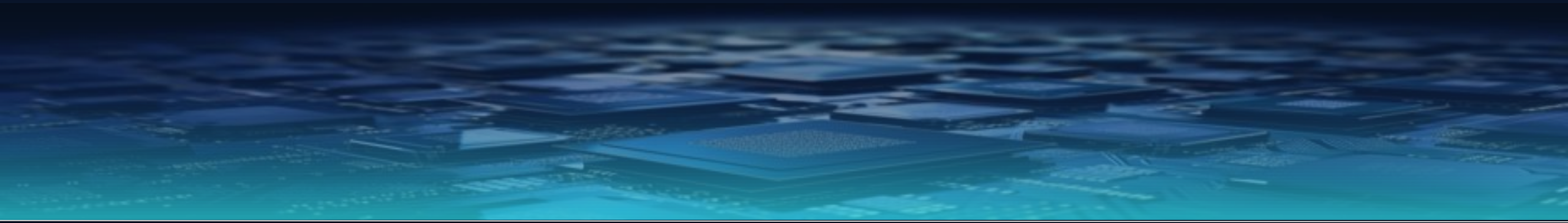
4. Metallization of glass substrates and high-aspect ratio Through Glass Vias (TGV)

1. LQDX’s Metallization Technology



LQDX is a Silicon Valley Nanomaterials Innovator Focused on Ultra High-Density PCB & Advanced Semiconductor Packaging

Incubated at Stanford Research Institute

Engineered at LQDX Santa Clara

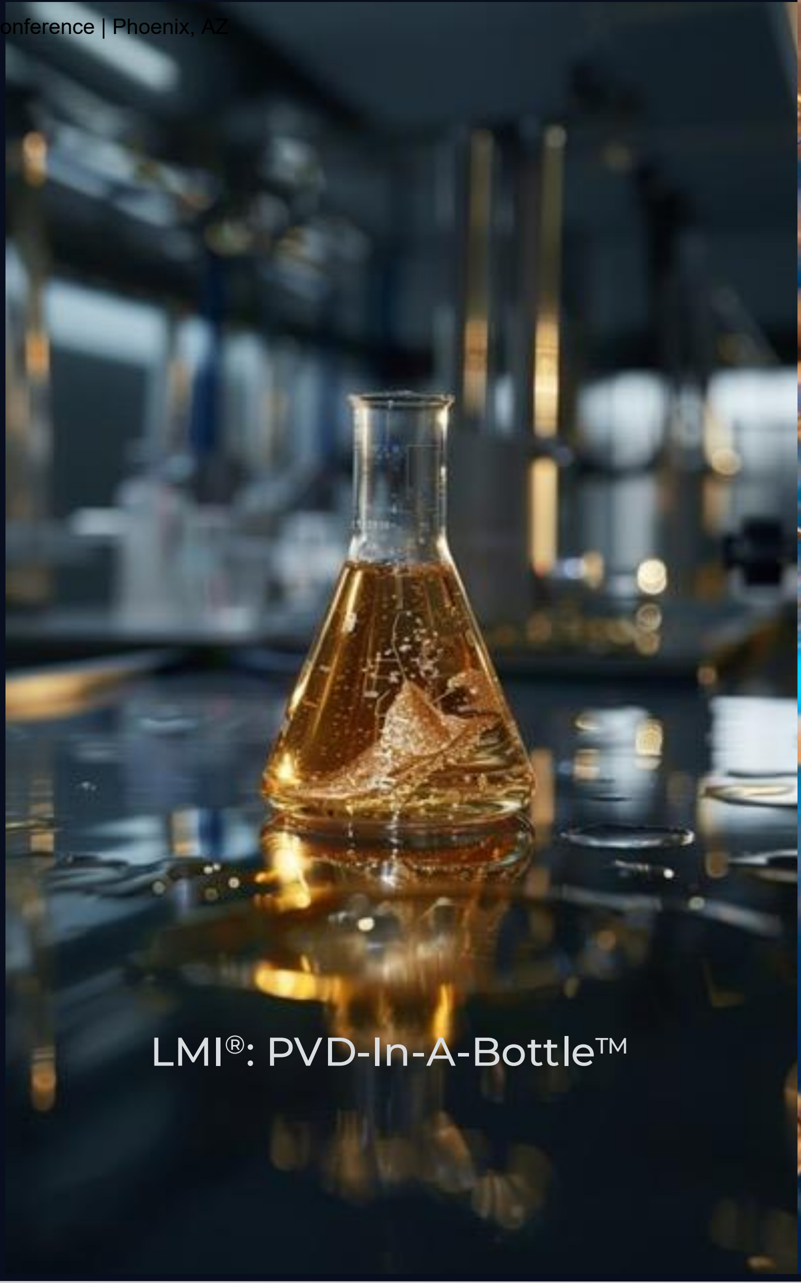
Patented Nano-Inks for AI and Datacenter-Driven PCB & Advanced Semiconductor Packaging

The Tech: LMI$_X$® | PVD-in-a-Bottle™

A unique atomic seed metallization chemistry suite enabling thin, conformal deposition of palladium, gold, copper and other PCB, semiconductor and bio-compatible metals by dipping, spraying, spinning or printing methods.

Palladium (the most common product) is the bedrock of every printed circuit made, including the most advanced substrates and semiconductor packaging techniques, and the industry roadmap demands features of 1um and below.

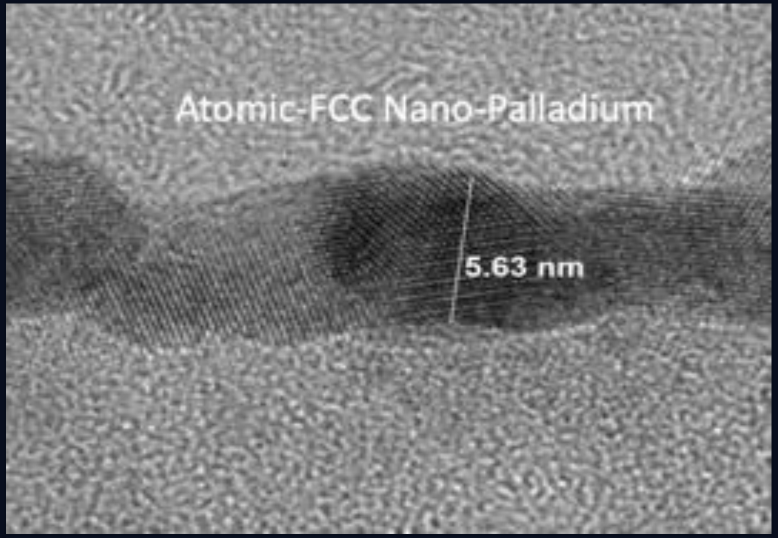
LQDX' patented Liquid Metal Ink (LMI$_X$®) technology is proven to meet this need without Physical Vapor Deposition (PVD)



LMI®: PVD-In-A-Bottle™

What is Unique about LMI_x® ?

- Atomic: 5nm+ nano-layers of pure metal deposition (unlike existing aqueous chemistries)
- Conformal: coats complex topologies and materials (unlike PVD)
- Organic: highly wetting tailored rheology (unlike aqueous chemistries)
- Low Viscosity Ink: designed for low-cost application (dipping, printing, spinning, spraying)



LMI® has a unique molecular composition enabling ultra-thin conformal atomic deposition on complex features and a broad range of substrate materials at low temperature.

Enabling the Highest Density Circuits on the Widest Range of Materials

Ultra Thin: a few nanometers thick

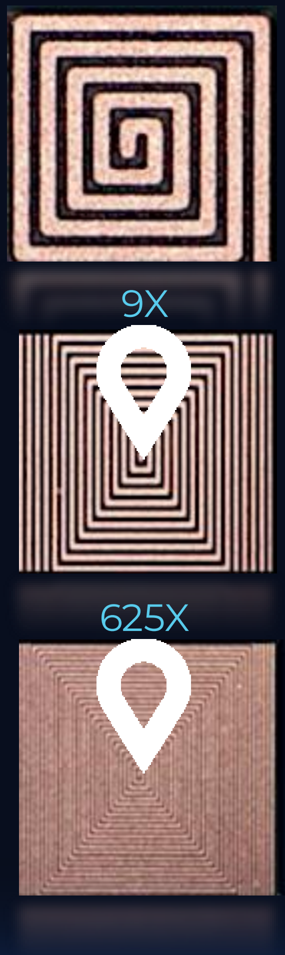
Ultra Dense: uniform atomic metal deposition

Ultra Conformal: high wettability to complex features

Ultra Compatible: adheres to any advanced substrate

Ultra Flexible: available in multiple metals and alloys

Lowest cost of adoption easily integrates into existing wet-chem back-end lines vs. PVD (Physical Vapor Deposition (PVD) front-end) manufacturing lines

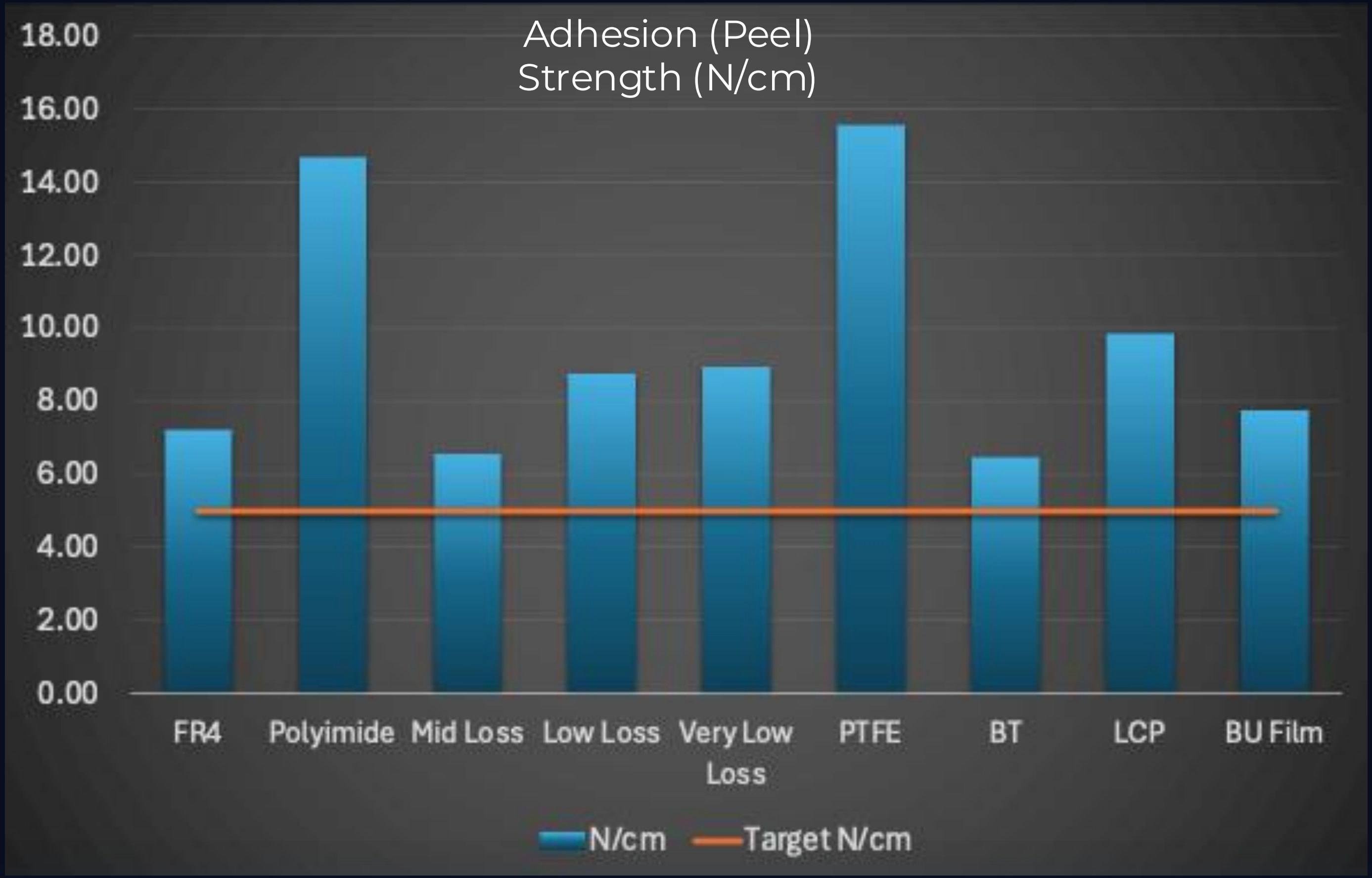


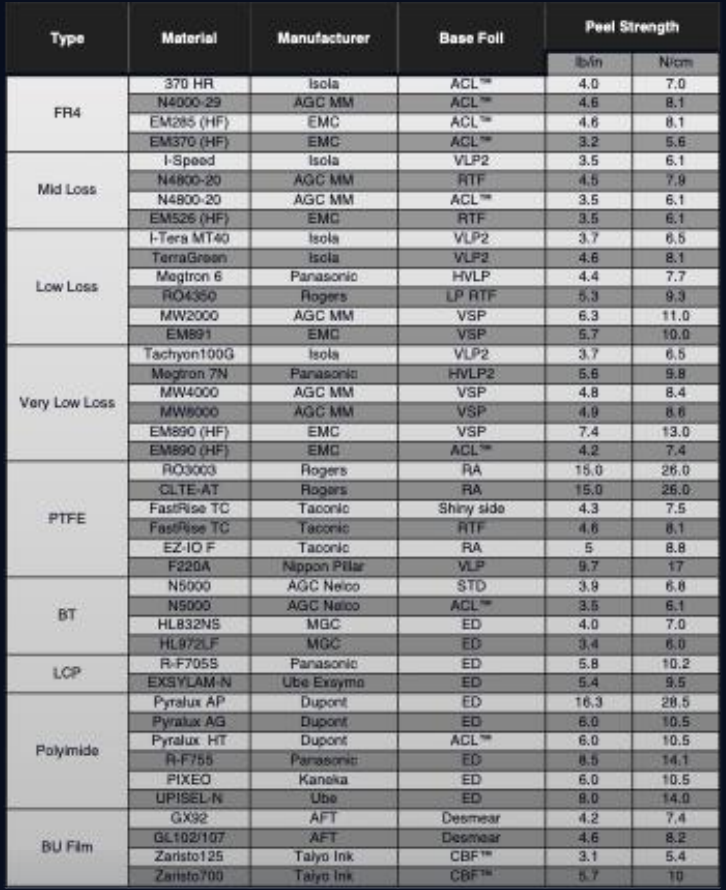
Standard US PCB Products:
75/75um Circuits

Ultra High-Density Interconnect (UHDI):
25/25um Circuits

LQDX LMI$_{x}^{®}$
1/1um Circuits

Enabling Superior Adhesion on All Advanced Substrates

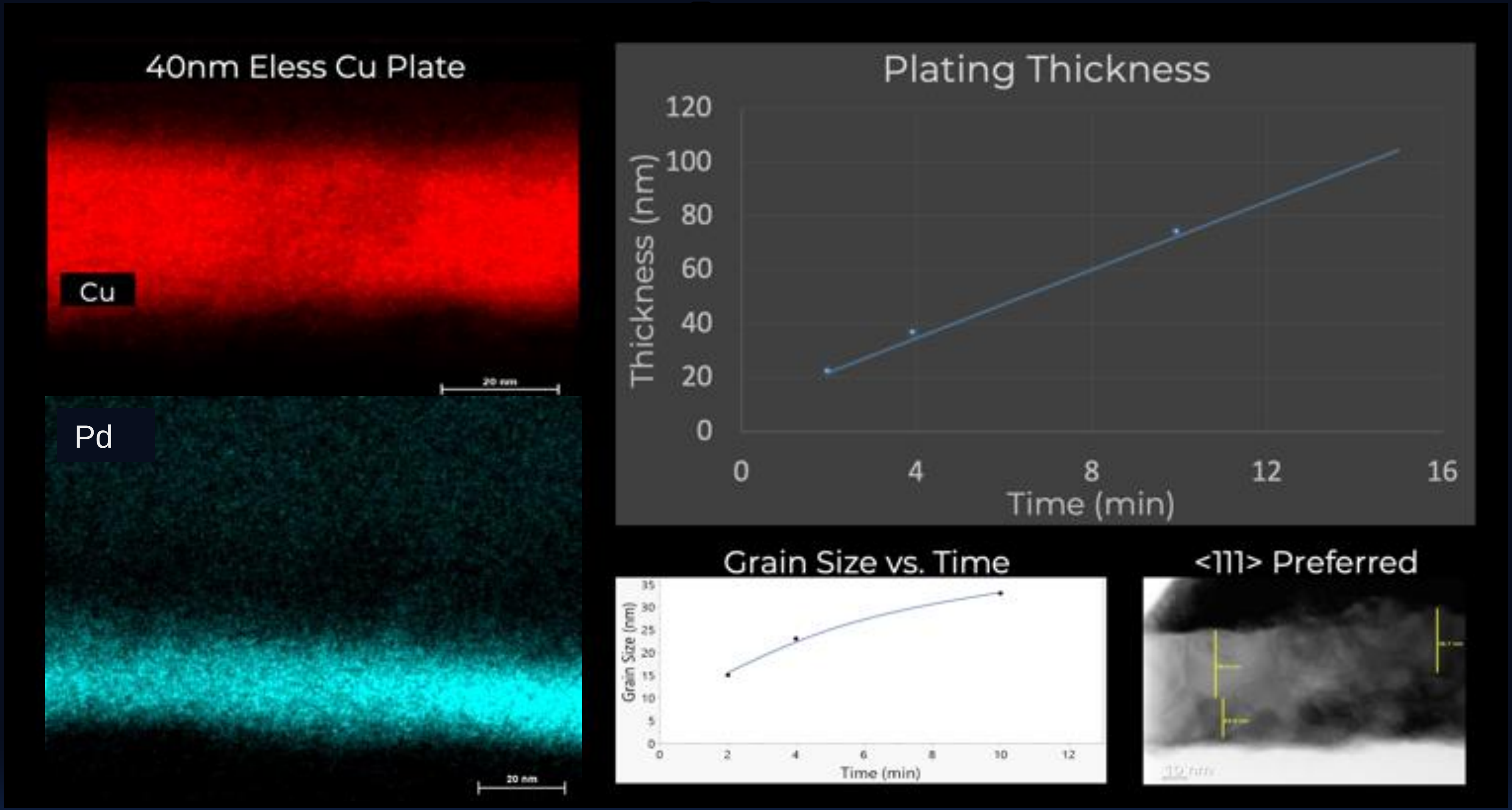




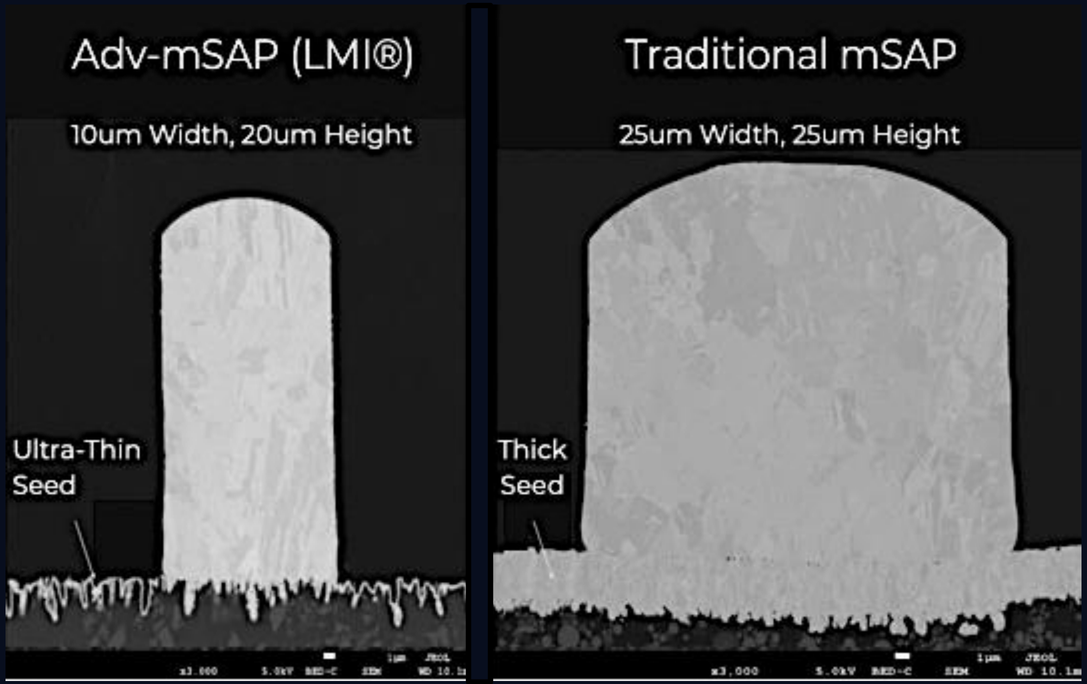
Type	Material	Manufacturer	Base Foil	Peel Strength	
				lb/in	N/cm
FR4	370 HR	Isola	ACL™	4.0	7.0
	N4000-29	AGC MM	ACL™	4.6	8.1
	EM285 (HF)	EMC	ACL™	4.6	8.1
	EM370 (HF)	EMC	ACL™	3.2	5.6
Mid Loss	I-Speed	Isola	VLP2	3.5	6.1
	N4800-20	AGC MM	RTF	4.5	7.9
	N4800-20	AGC MM	ACL™	3.5	6.1
	EM526 (HF)	EMC	RTF	3.5	6.1
Low Loss	I-Tera MT40	Isola	VLP2	3.7	6.5
	TerraGreen	Isola	VLP2	4.6	8.1
	Megtron 6	Panasonic	HVLP	4.4	7.7
	RO4350	Rogers	LP RTF	5.3	9.3
	MW2000	AGC MM	VSP	6.3	11.0
	EM891	EMC	VSP	5.7	10.0
Very Low Loss	Tachyon100G	Isola	VLP2	3.7	6.5
	Megtron 7N	Panasonic	HVLP2	5.6	9.8
	MW4000	AGC MM	VSP	4.8	8.4
	MW8000	AGC MM	VSP	4.9	8.6
	EM890 (HF)	EMC	VSP	7.4	13.0
	EM890 (HF)	EMC	ACL™	4.2	7.4
PTFE	RO3003	Rogers	RA	15.0	26.0
	CLTE-AT	Rogers	RA	15.0	26.0
	FastRise TC	Taconic	Shiny side	4.3	7.5
	FastRise TC	Taconic	RTF	4.6	8.1
	EZ-IO F	Taconic	RA	5	8.8
	F220A	Nippon Pillar	VLP	9.7	17
BT	N5000	AGC Nelco	STD	3.9	6.8
	N5000	AGC Nelco	ACL™	3.5	6.1
	HL832NS	MGC	ED	4.0	7.0
	HL972LF	MGC	ED	3.4	6.0
LCP	R-F705S	Panasonic	ED	5.8	10.2
	EXSYLAM-N	Ube Exsymo	ED	5.4	9.5
Polyimide	Pyralux AP	Dupont	ED	16.3	28.5
	Pyralux AG	Dupont	ED	6.0	10.5
	Pyralux HT	Dupont	ACL™	6.0	10.5
	R-F755	Panasonic	ED	8.5	14.1
	PIXEO	Kaneka	ED	6.0	10.5
	UPISEL-N	Ube	ED	8.0	14.0
BU Film	GX92	AFT	Desmear	4.2	7.4
	GL102/107	AFT	Desmear	4.6	8.2
	Zaristo125	Taiyo Ink	CBF™	3.1	5.4
	Zaristo700	Taiyo Ink	CBF™	5.7	10

Enabling Ultra-Dense Lines/Spaces on the Most Advanced IC-Substrates

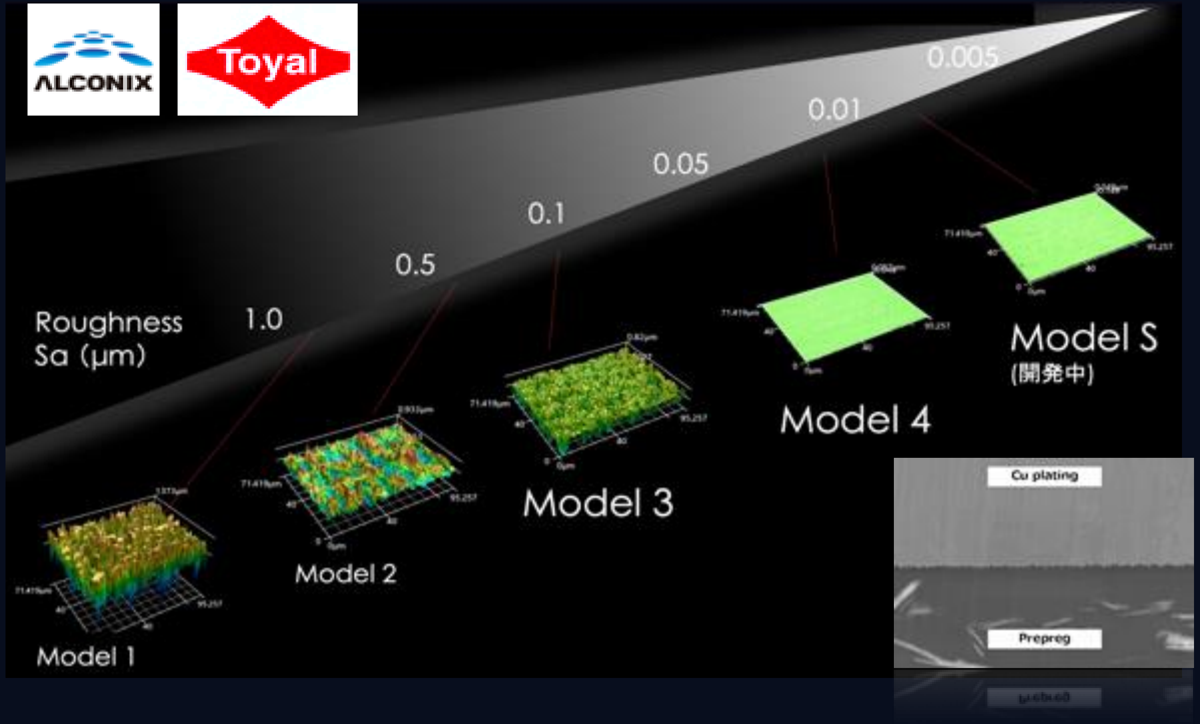
Ultra-Thin Electroless Copper (40nm) + Ultra-Fine Lines/Spaces (1/1um) with Preferred Grain Size & Structure: ACL™ & LMI$_x$®



Enabling Superior Signal Integrity with Aluminum Clad Laminates (ACL^{TM})

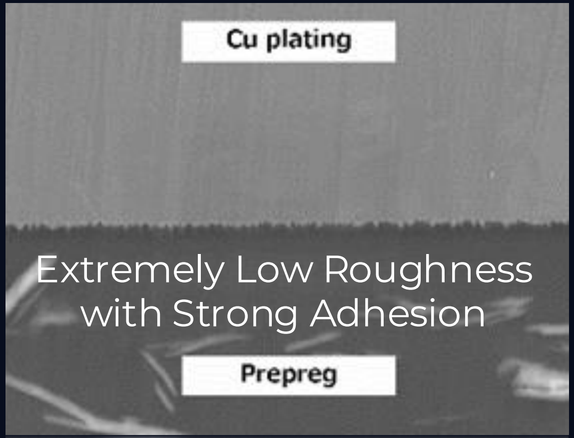


Extremely Thin Seed Layers =
Extremely Straight Side Walls

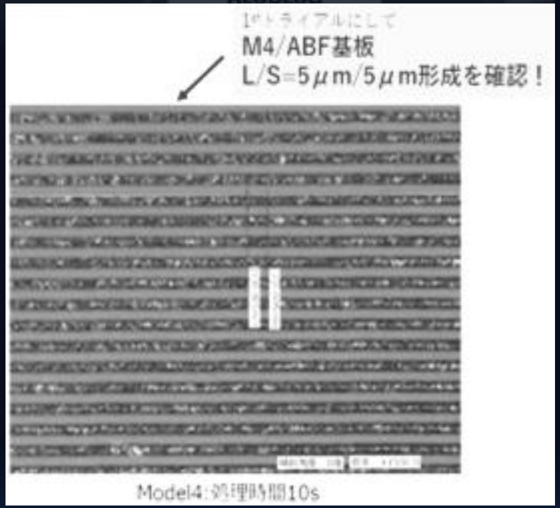


Extremely Low Aluminum Roughness =
Extremely Fine Lines w/ Strong Adhesion

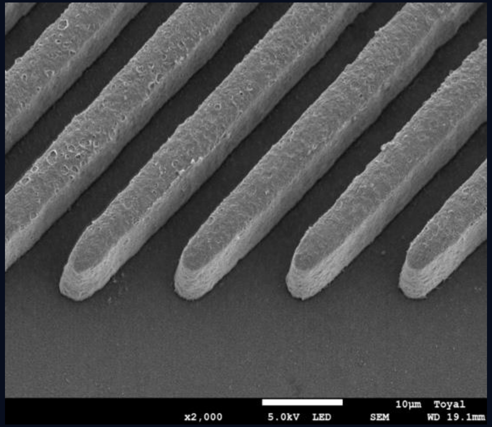
Enabling Superior High-Frequency Interconnect Performance

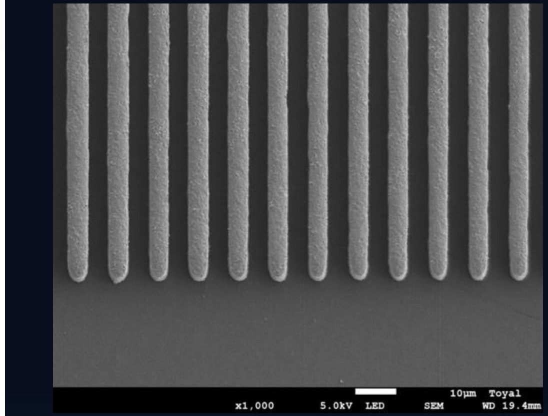


Extremely Low Roughness with Strong Adhesion



Extremely Thin Seed Layers = Extremely Straight Side Walls



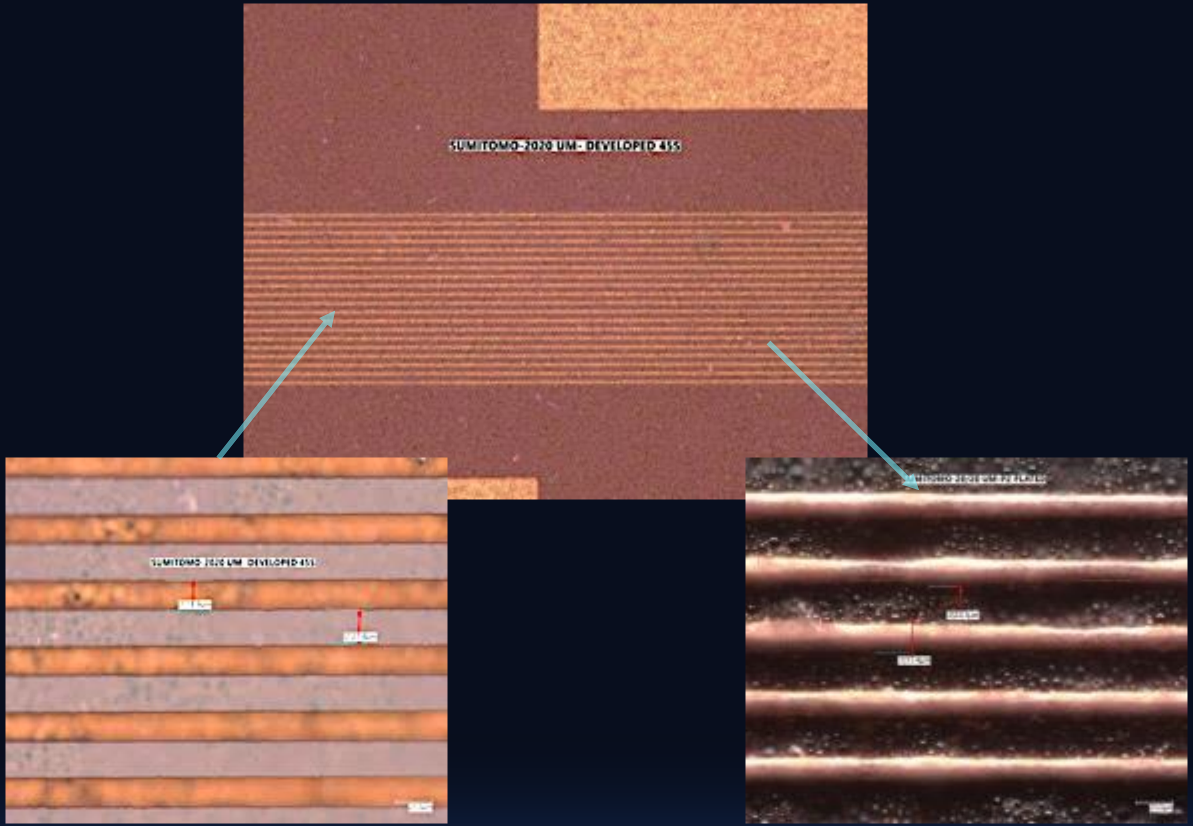


and Extremely Fine Features.

Enabling Next Gen Packaging: E.g. Low-Cost Ink Metallization of FOWLP

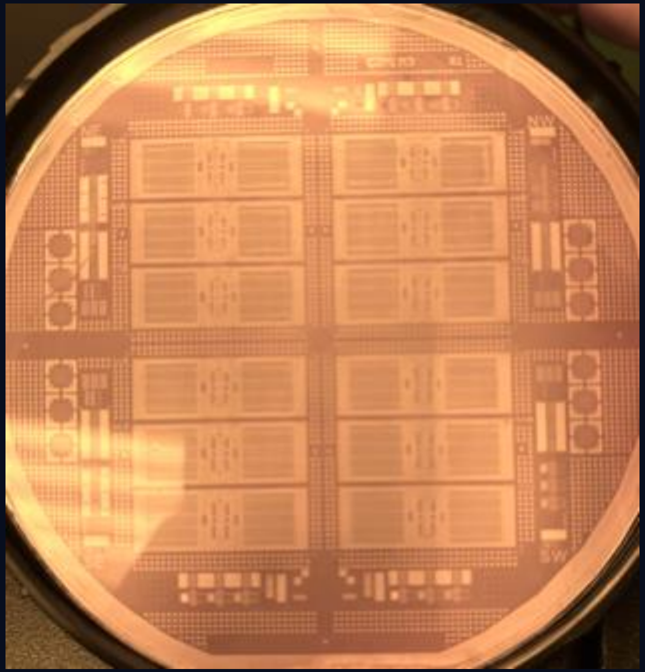
- SUMITOMO: PROPRIETARY EMC
- LQDX: LMI$_x$®
- ATOTECH: E-less Cu MV TP2
- BREWER SCIENCE: Photo Resist + Imaging
- MARCH: Pre-Plasma: O2/CF4
- ATOTECH: ECD + PR Removal/Flash Etch

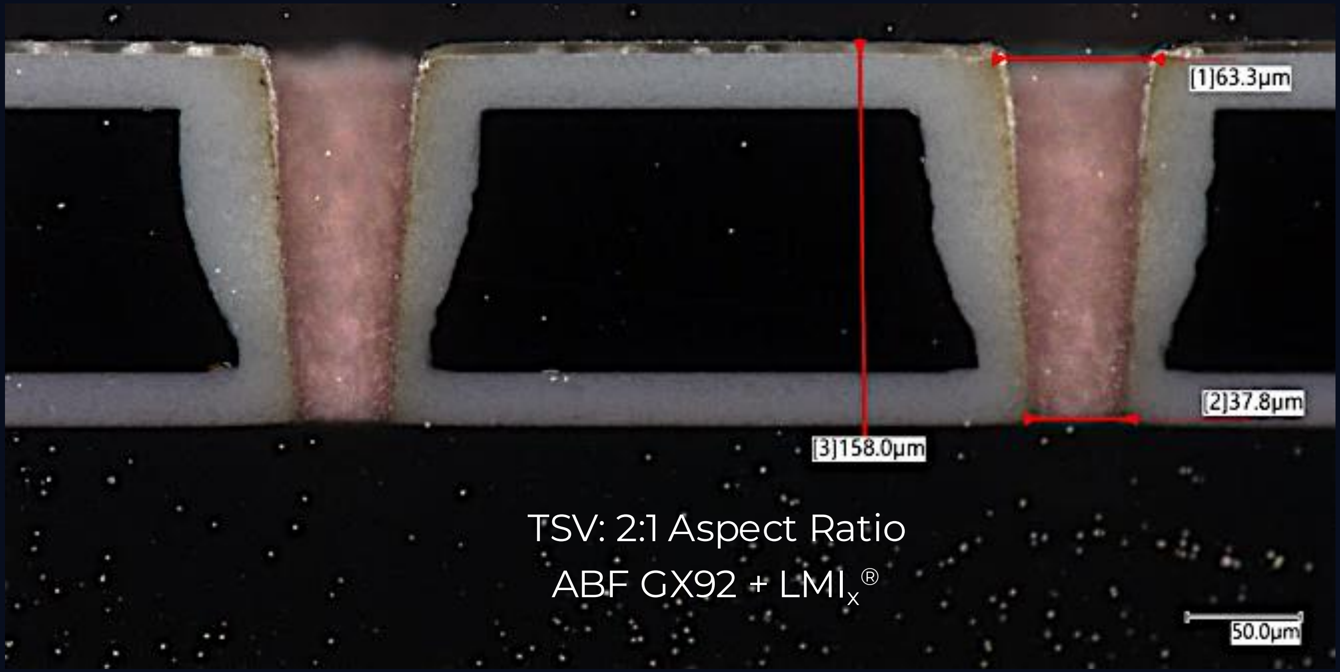
LQDX-Alconix-Brewer Science Design/Mask (7um, 15um, 20um features). Max Temp 170C.



Enabling Next Gen Semiconductor Packaging: E.g. Silicon Substates w/ TSV

Substrate on Wafer Test Vehicle (Designed by AMAT):

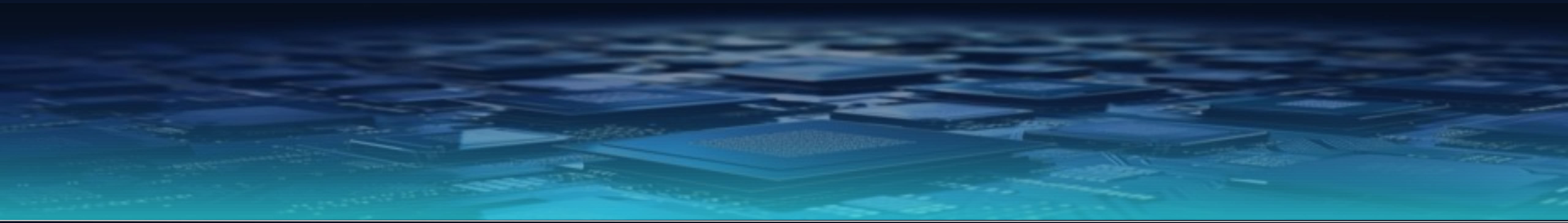




TSV: 2:1 Aspect Ratio
ABF GX92 + $\text{LMI}_x^{®}$

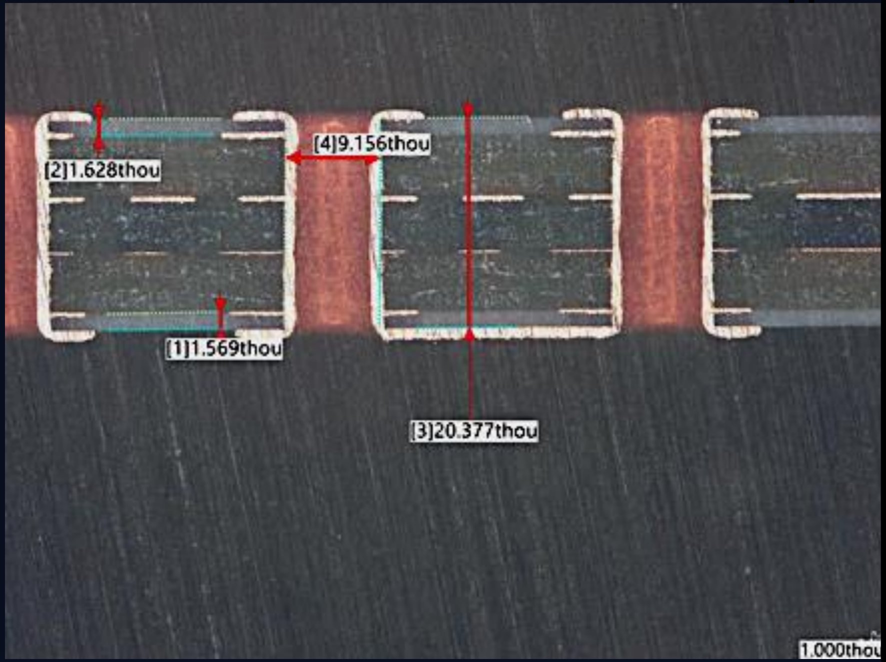
Shared Courtesy of Applied Materials Inc.

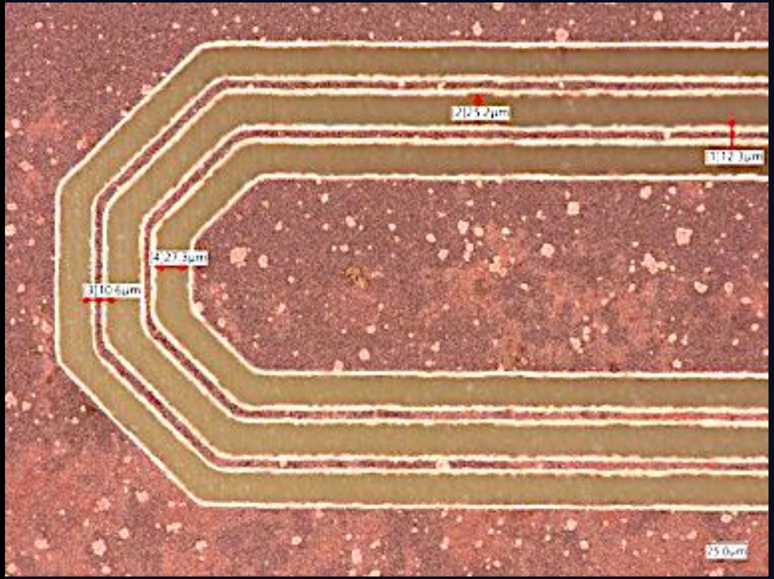
2. Metallization of Ultra UHDI Organic Substrates

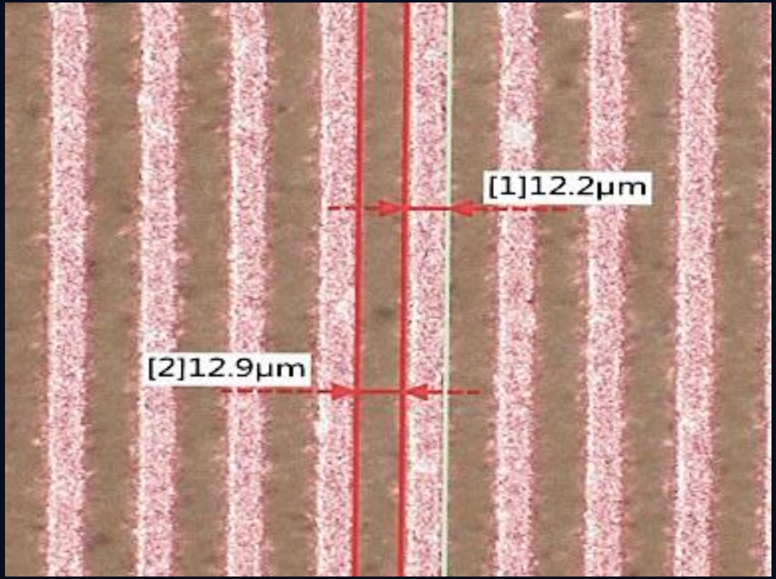


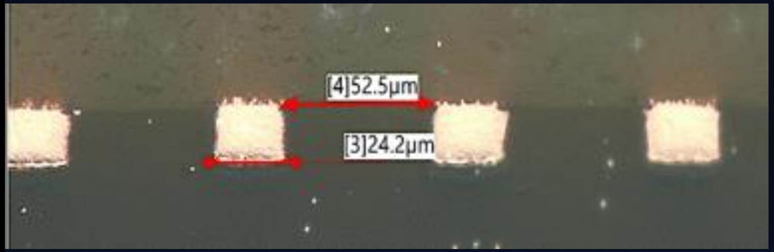
Enabling Advanced UHDI PCBs Using 100% USA Supply Chain

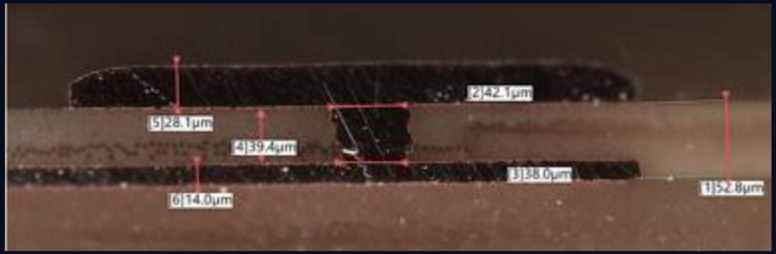
½ mil (12um) patterns on 6-Layer UHDI RF circuit boards using 100% USA material set including LQDX ACL™ & LMI_x®
(Designed and built by NSWC Crane)





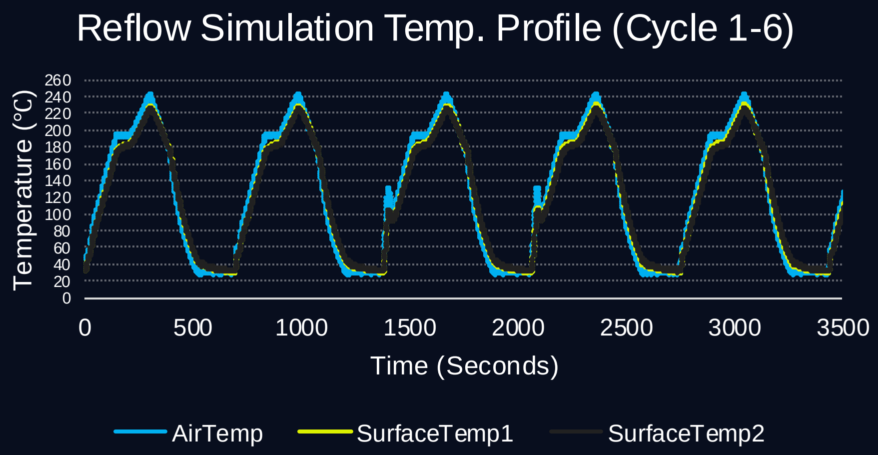


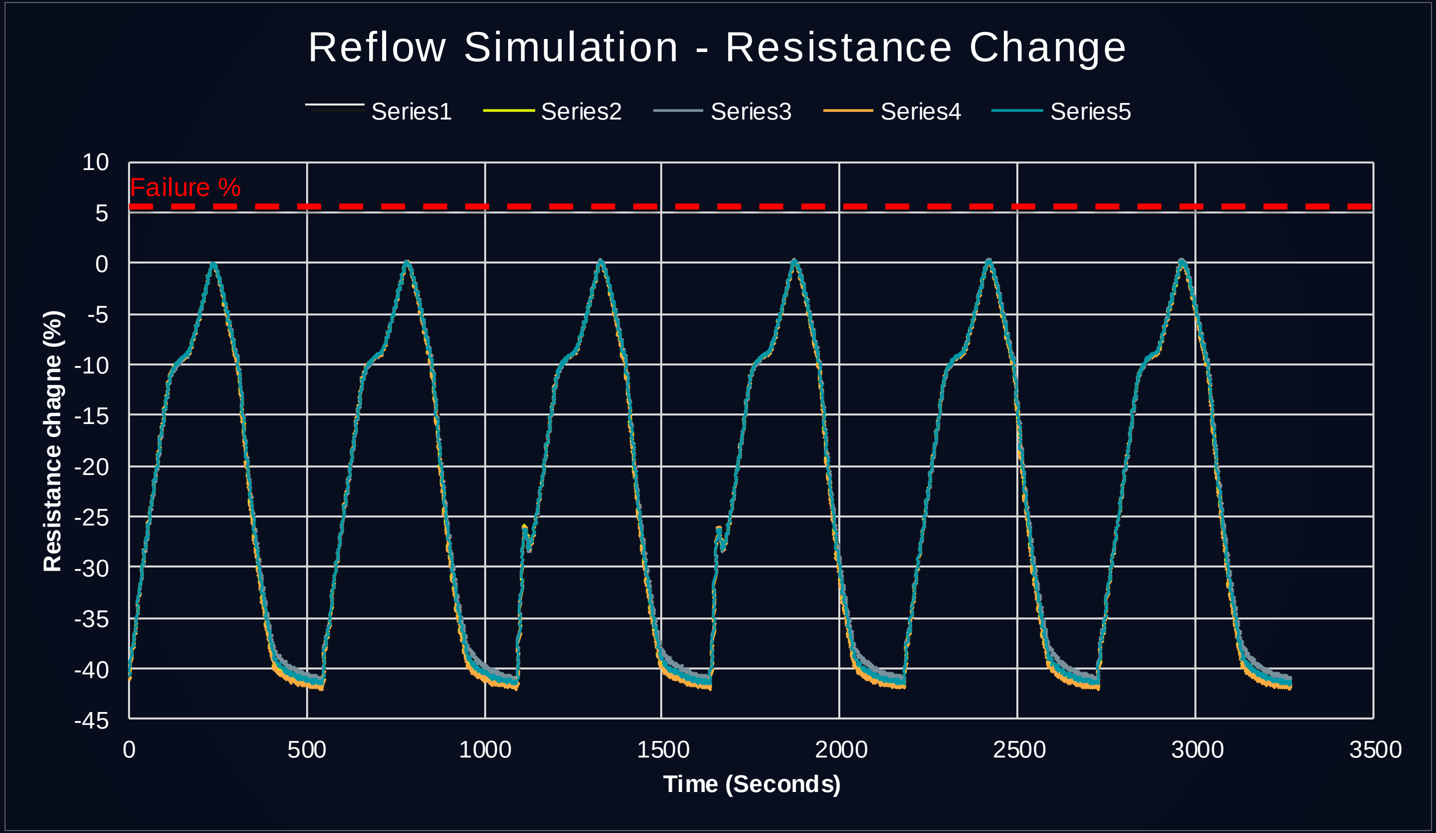




Reliability Data - Thermal Stress, Convection Reflow Simulation

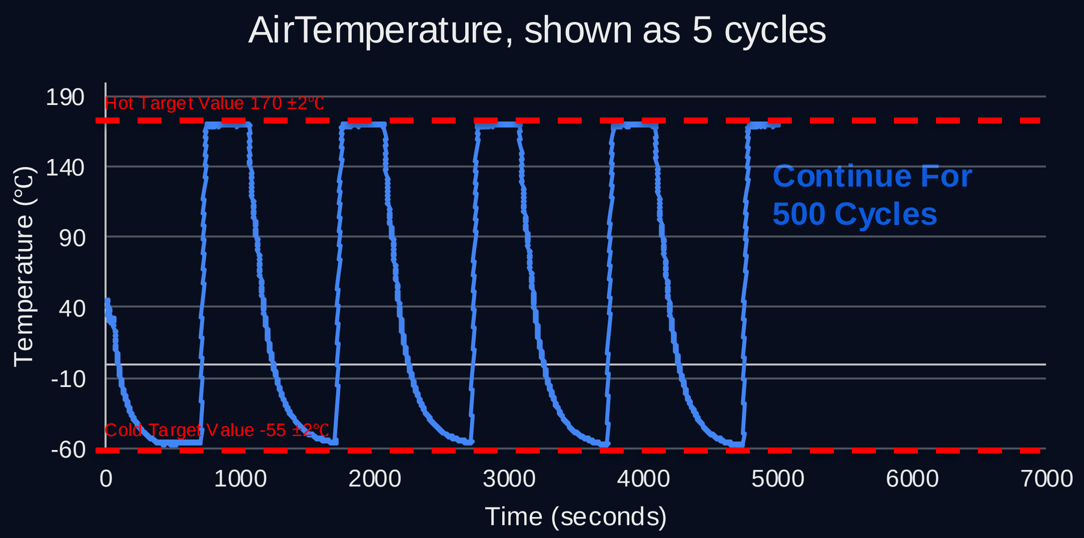
- Test Method: IPC-TM-650 Method 2.6.27B, Table 5-2 (230℃)
- Reflow Profile: 230 ℃
- Quantity of Cycles: 6
- Number of Nets per Coupon: 2
- Failure Percentage (%): 5



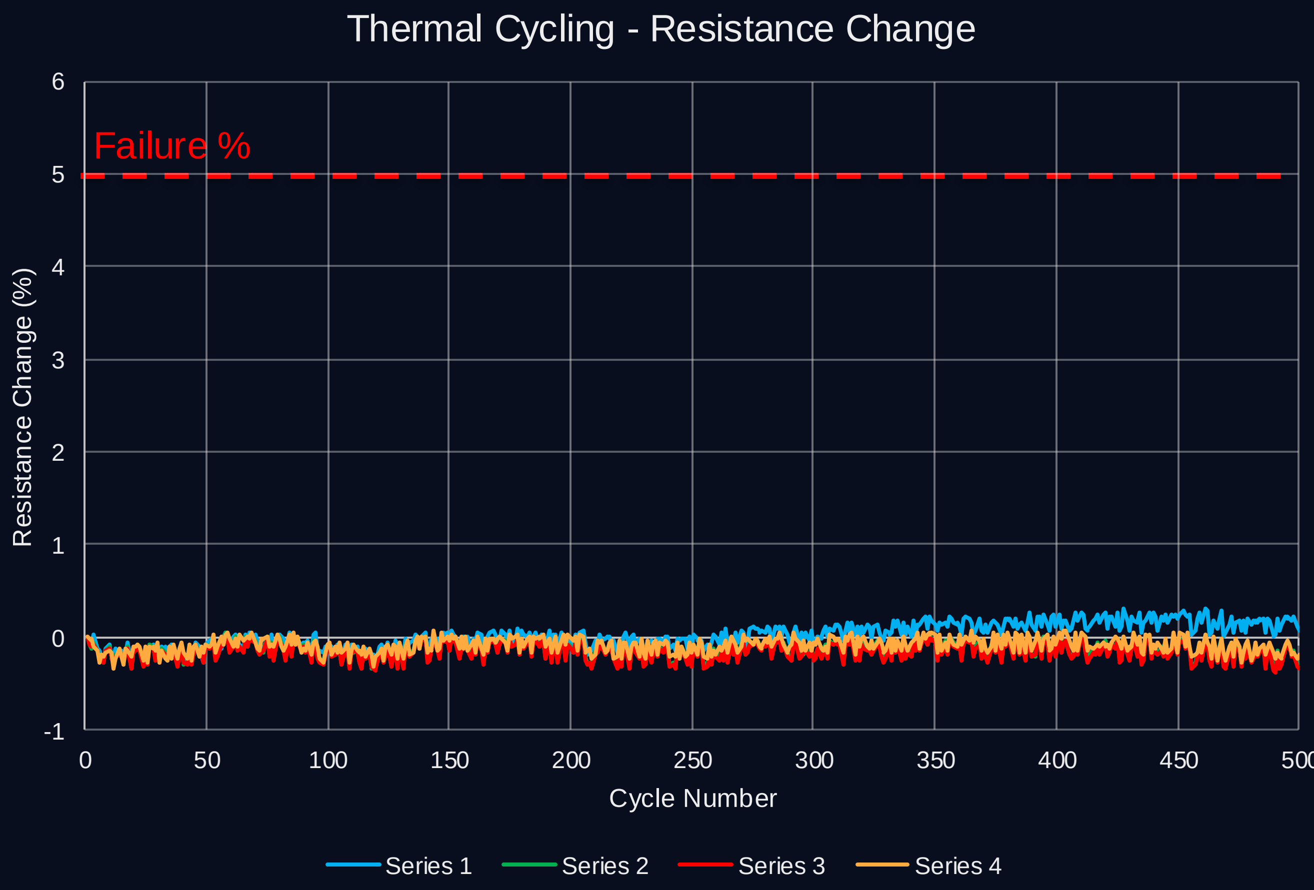


Reliability Data - Thermal Shock

- **Test Method:** IPC-TM-650 Method 2.6.7.2C, Continuity
- **Cycle Range:** -55℃ - 170 ℃
- **Quantity of Cycles:** 500
- **Number of Nets per Coupon:** 2
- **Failure Percentage (%):** 5



Continue For 500 Cycles

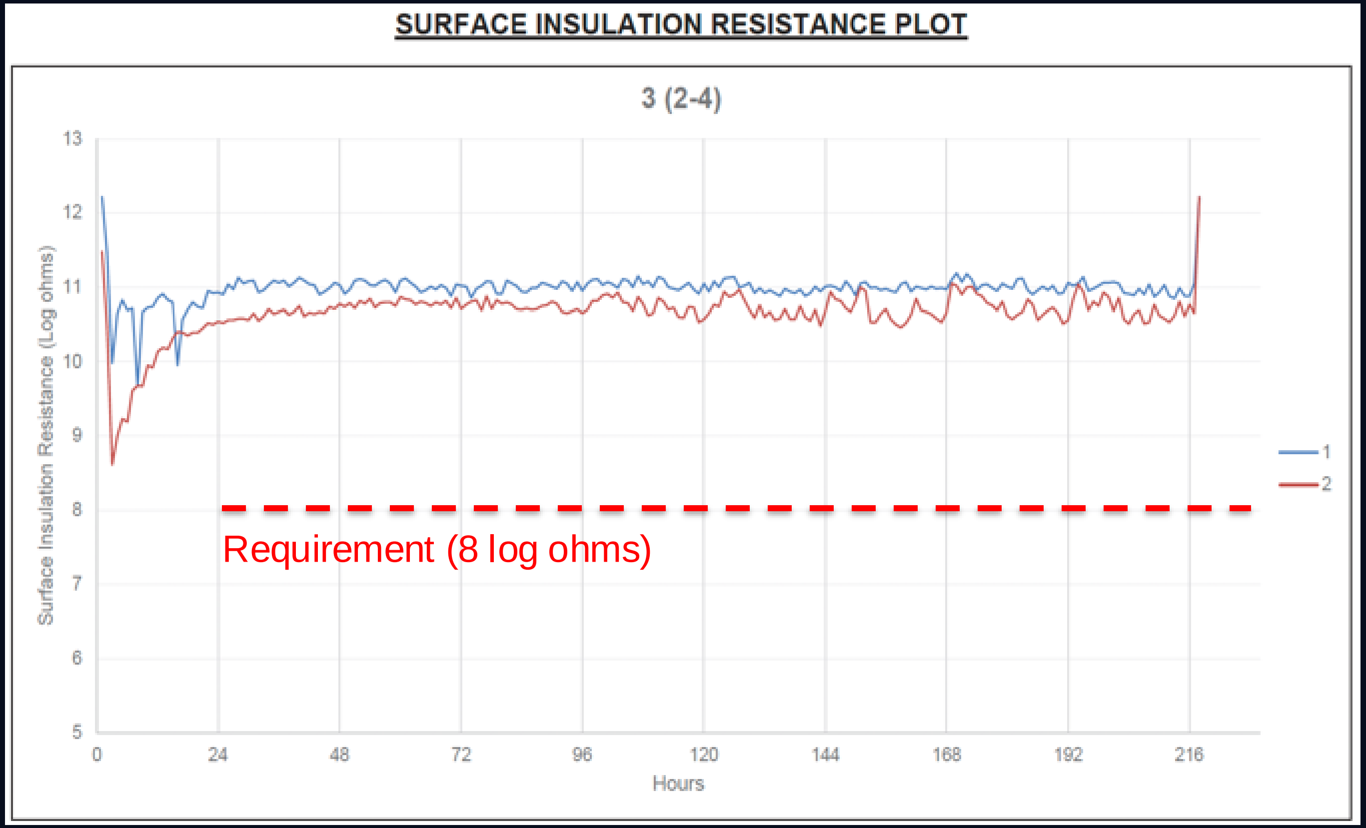


Reliability Data - Surface Insulation Resistance

- Test Method: IPC-TM-650 Method 2.6.3.7
- Test Conditions: 40 ℃ / 90 %RH
- Duration: 72 hours
- Bias Voltage: 5 volts DC
- Measurement Voltage : 5 volts DC

Requirement:

All SIR test patterns shall show a minimum resistance of 100 megohms (>108 ohms), beginning 24 hours after the chamber has stabilized at the elevated test condition



SURFACE INSULATION RESISTANCE PLOT

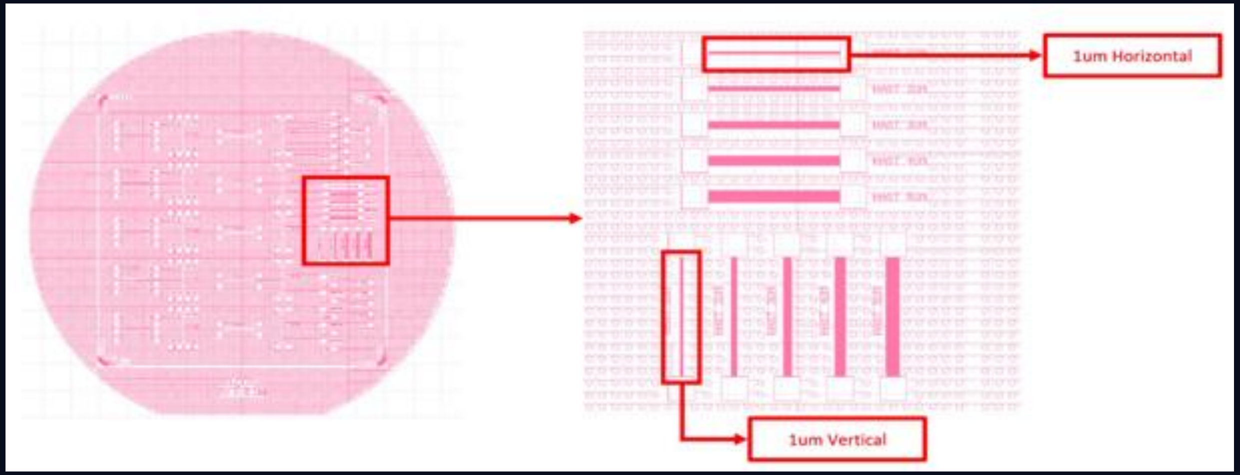
Requirement (8 log ohms)

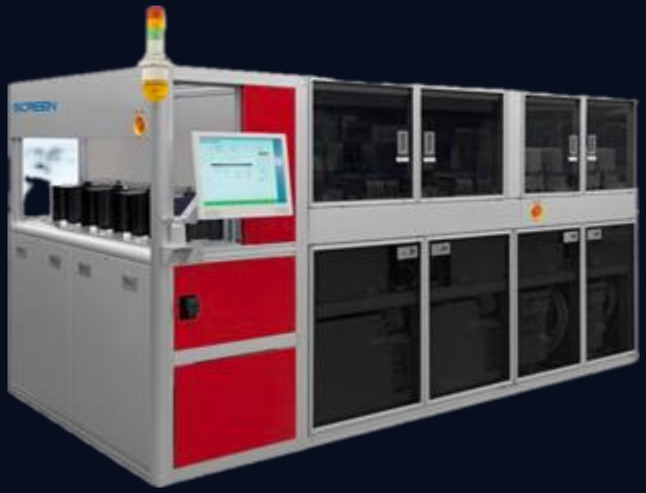
LQDX + ASU

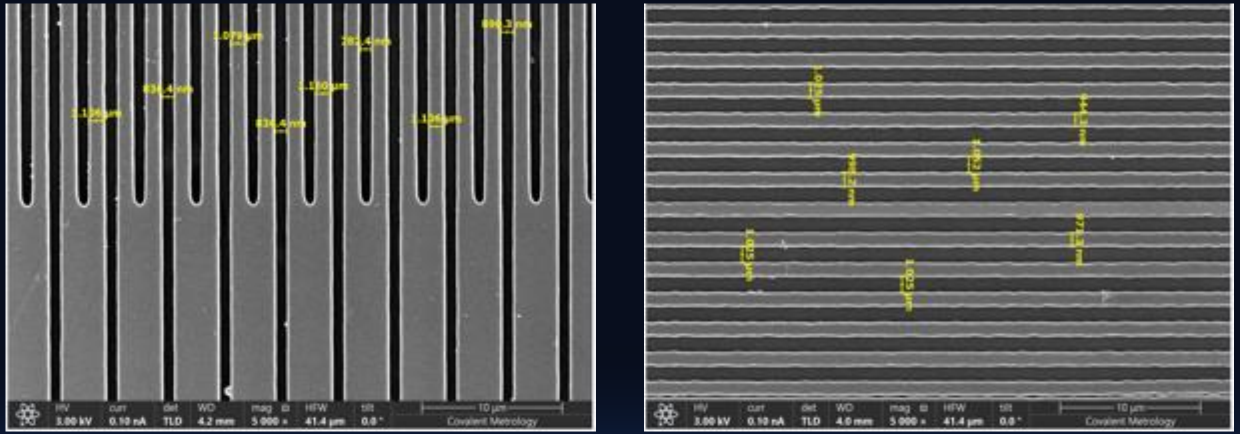
3. Patterning of Sub-Micron Features & Vias

1um Trace/Space Test Vehicle (LQDX + Japan Partnerships)

Consortia Test Vehicle: 1um Feature Pattern (Designed by AT&S)





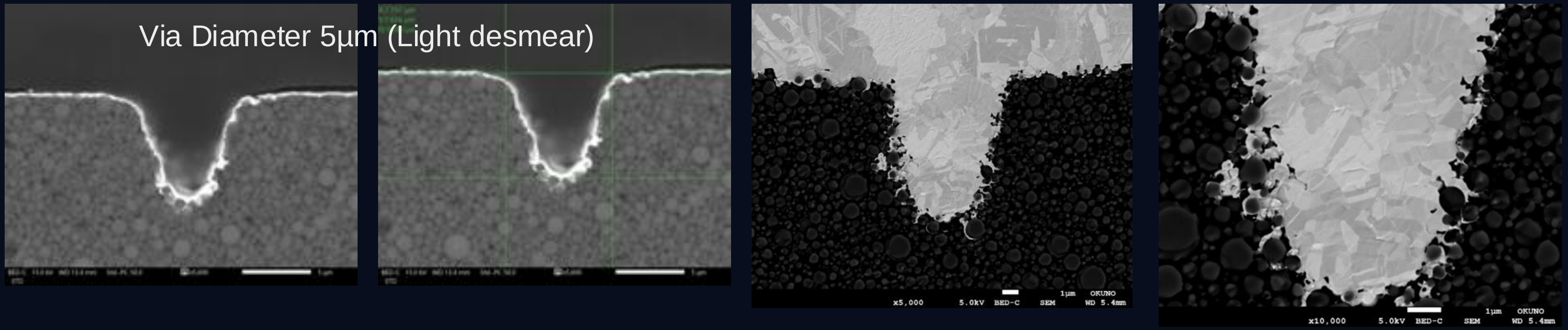


1um L/S

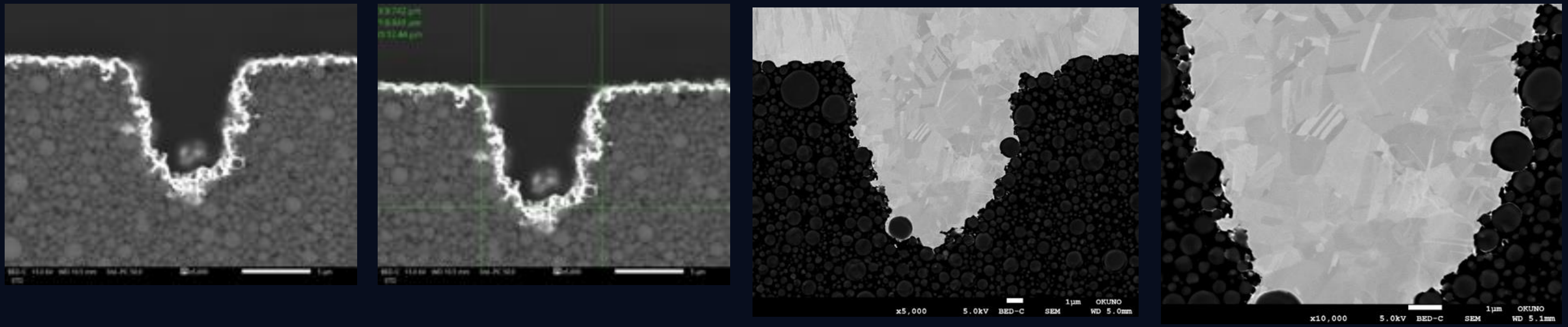
- AT&S: Design
- AJINIMOTO: ABF GL-102
- LQDX: LMI$_x$®
- UYEMURA: E-less Cu
- JSR: Liquid Photo Resist
- SCREEN: Direct Imaging
- OKUNO: ECD + PR Removal/Etch

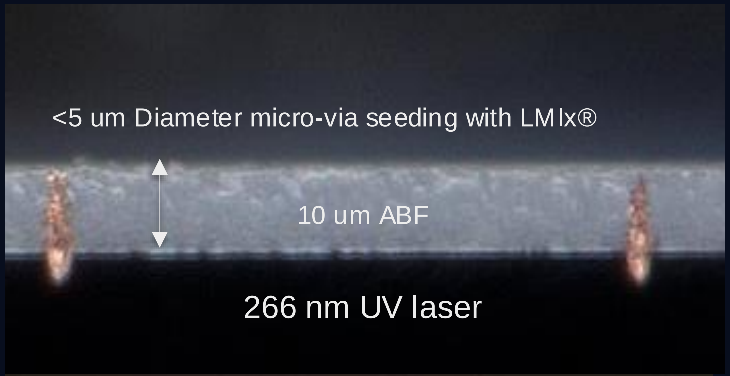
5um Micro-Vias (2:1 AR) on ABF® GL Materials

Via Diameter 5µm (Light desmear)



Via Diameter 5µm (Regular Desmear)





<5 um Diameter micro-via seeding with LMIx®

266 nm UV laser

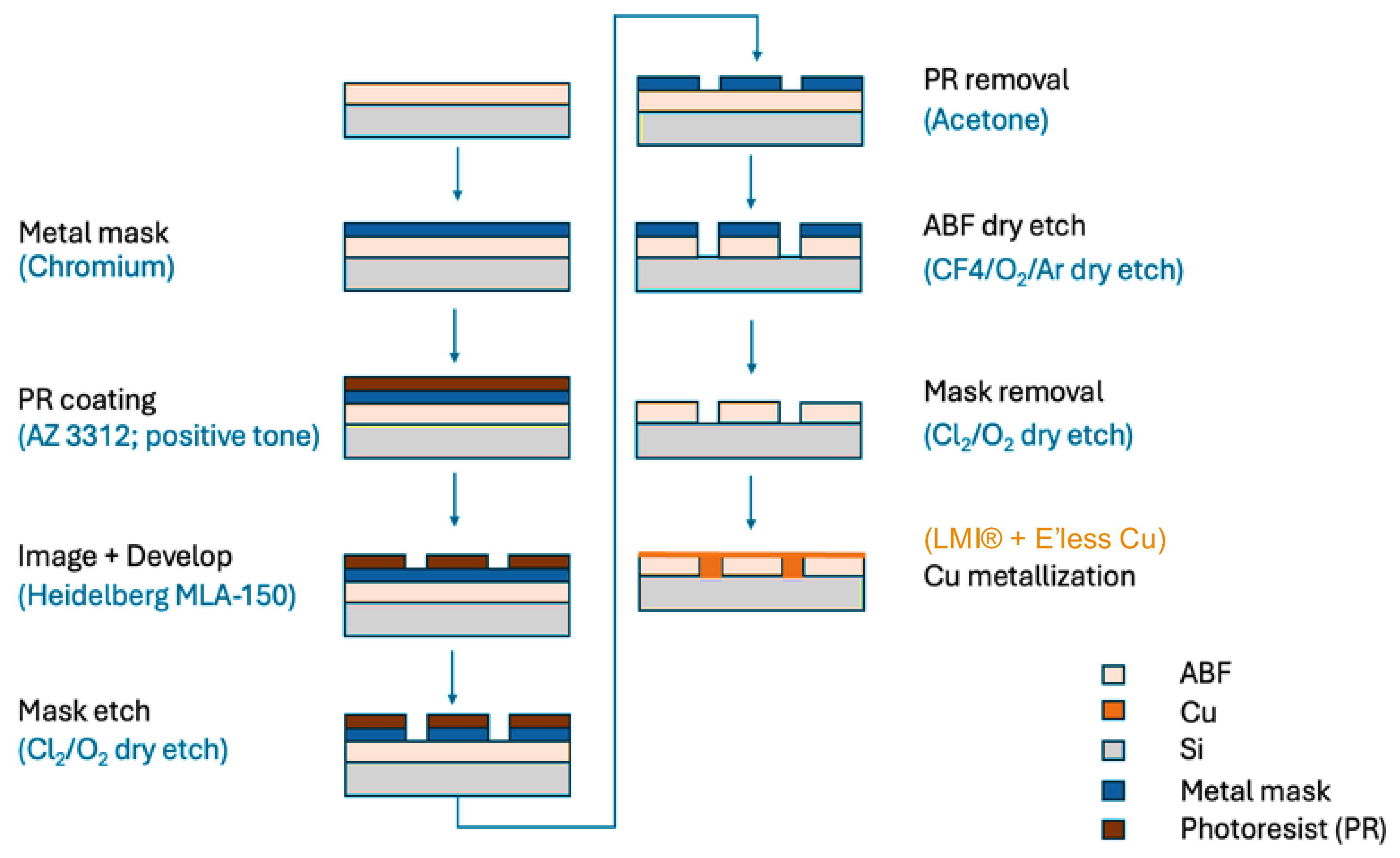
A comprehensive DOE was completed to assess the impact of: (1) ABF material type, (2) laser type [excimer vs. UV], (3) laser process conditions, (4) pre-clean and chemical de-smear parameters, (5) plasma pre-treatment, (6) compatibility of commercial e-less copper chemistries, and (7) cure/annealing variables.

CONCLUSIONS: Optimal performance on GL materials = $\mathrm{LMI}_{\mathrm{ABF}}$, DI water rinse, minimal de-smear, 170C cure, with optimized laser parameters and process chemistry compatibility variables available with permission.

Sub-Micron Features & Deep Vias in ABF with Dry Etch Processing

Highly efficient solution for high density panel level packaging: DRIE + LMI®

DRIE Process Flow



Metal mask
(Chromium)

PR coating
(AZ 3312; positive tone)

Image + Develop
(Heidelberg MLA-150)

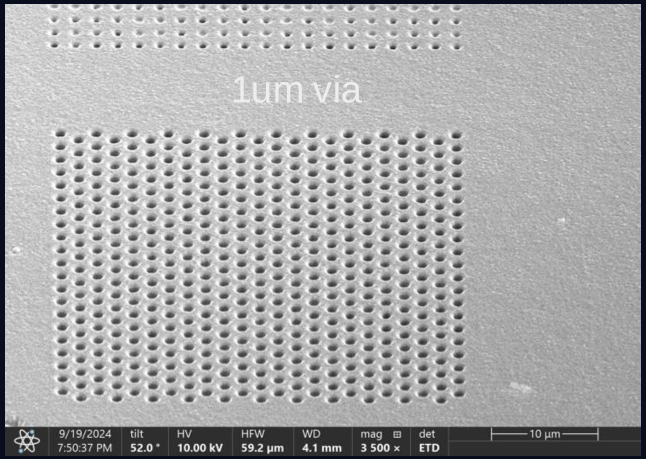
Mask etch
(Cl$_2$/O$_2$ dry etch)

PR removal
(Acetone)

ABF dry etch
(CF4/O$_2$/Ar dry etch)

Mask removal
(Cl$_2$/O$_2$ dry etch)

(LMI® + E'less Cu)
Cu metallization

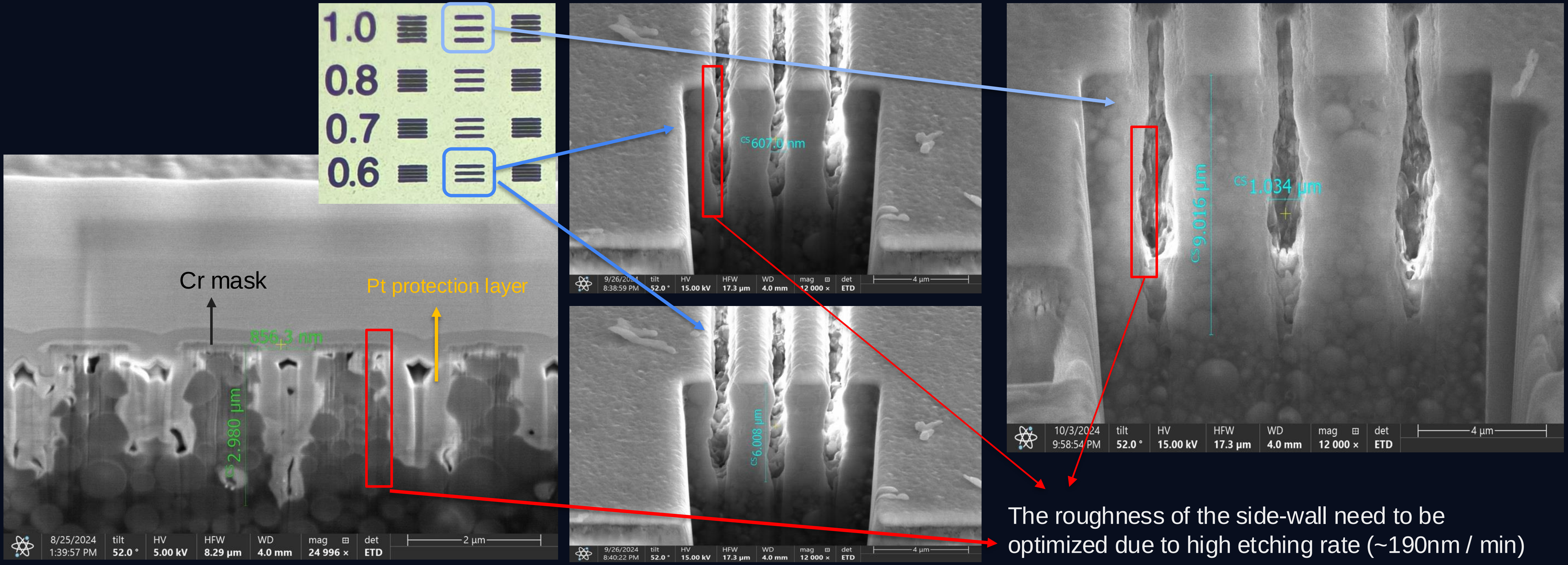


Dry etch recipe for 1um vias

RF power	350 W
Pressure	70 mT
CF4:O2	9:1
Etch time	120 mins
CF4 rate (sccm)	36
O2 rate (sccm)	4
Ar rate (sccm)	25

Sub-Micron Features & Deep Vias in ABF with Dry Etch Processing

Achieving 10:1 AR by DRIE, design for AI and 6G applications



Trench Width: 0.6 um
Trench Depth: 6 um

Trench width: 1 um
Trench depth: 9 um

The roughness of the side-wall need to be optimized due to high etching rate (~190nm / min)

Sub-Micron Features & Deep Vias in ABF with Dry Etch Processing

Improving side-wall roughness to enhance data/signal transmission efficiency

Roughness vs Etching rate DOE

Etching Time (min)	RF Power (W)	Pressure (mT)	$CF_4:O_2$	Etching Depth (nm)	Etching Speed (nm/min)	Roughness (nm)
15	250	100	8:2	2850	190	500
			9:1	2250	150	300
			10:0	1300	87	100

Adding O_2 increases the etching rate, but it also leads to a rougher surface

Roughness vs Pressure DOE

Etching Time (min)	RF Power (W)	$CF_4:O_2$	Pressure (mT)	Etching Depth (nm)	Etching Speed (nm/min)	Roughness (nm)
15	250	9:1	100	2250	150	300
			900	900	60	300
		10:0	50	1150	77	100
			100	1300	87	100

Lowering pressure also increases the etching rate, but it has no impact on the roughness

Sub-Micron Features & Deep Vias in ABF with Dry Etch Processing

A 3-step process for 5um in diameter and 25 um in depth via with no resin or silica residual in the via

Step 1: Etching Silica filler Smooth side-wall	
RF power	350 W
Pressure	70 mT
CF4:O2	9:1
CF4 rate (sccm)	36
O2 rate (sccm)	4
Ar rate (sccm)	25

➡

Step 2: Etching resin Good resolution	
RF power	350 W
Pressure	100 mT
CF4:O2	8:2
CF4 rate (sccm)	32
O2 rate (sccm)	8
Ar rate (sccm)	25

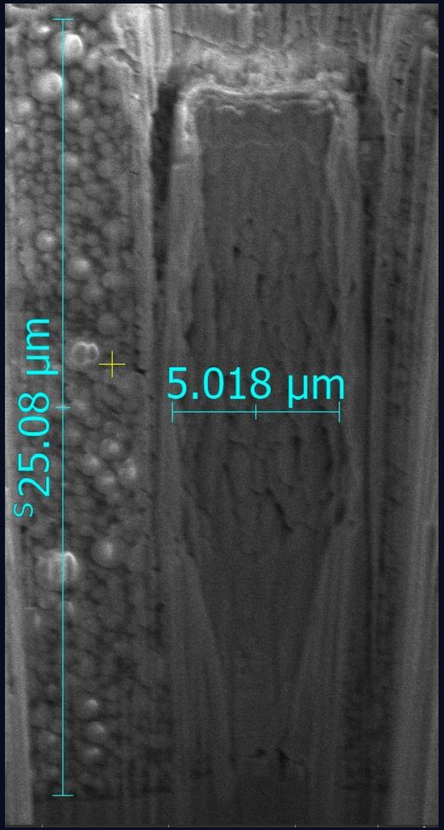
➡

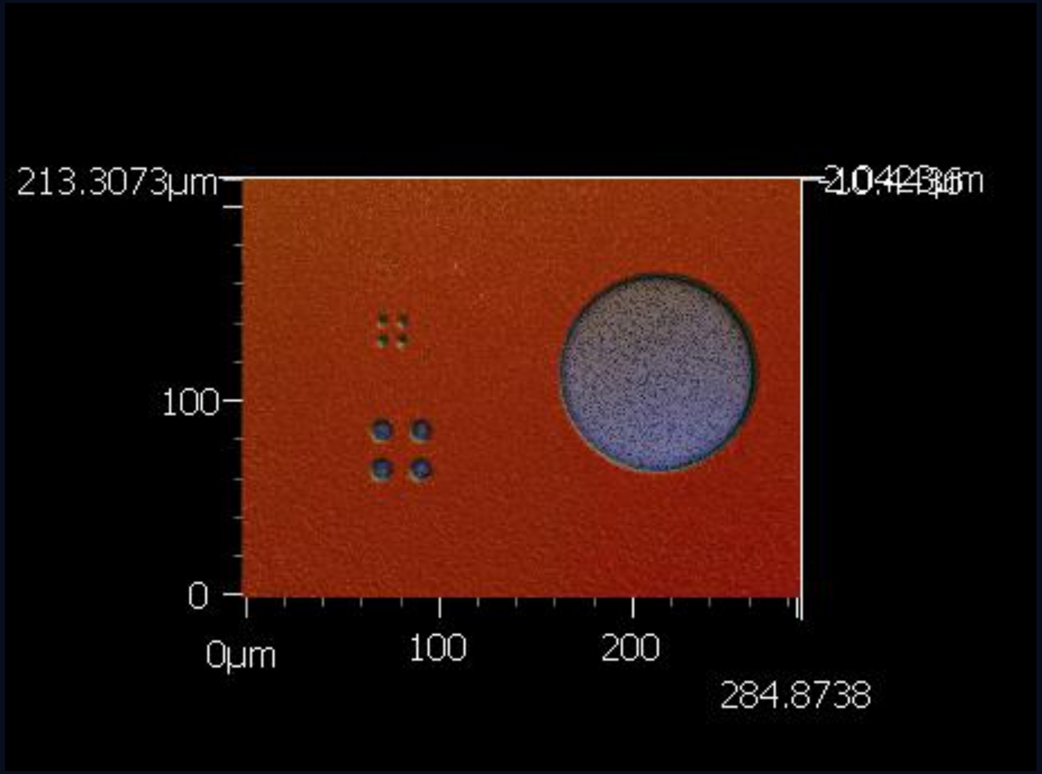
Step 3: Clean-up Silica filler Accurate dimension	
RF power	350 W
Pressure	70 mT
CF4:O2	9:1
CF4 rate (sccm)	36
O2 rate (sccm)	4
Ar rate (sccm)	25

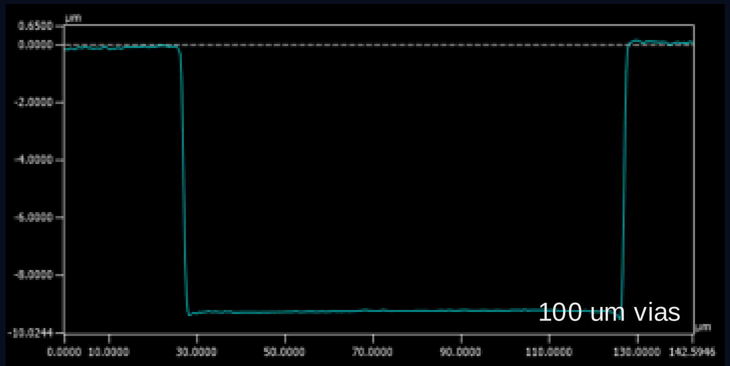
Sub-Micron Features & Deep Vias in ABF with Dry Etch Processing

High signal communication efficiency, zero debris residual, high aspect ratio and less taper-angle for high density via process

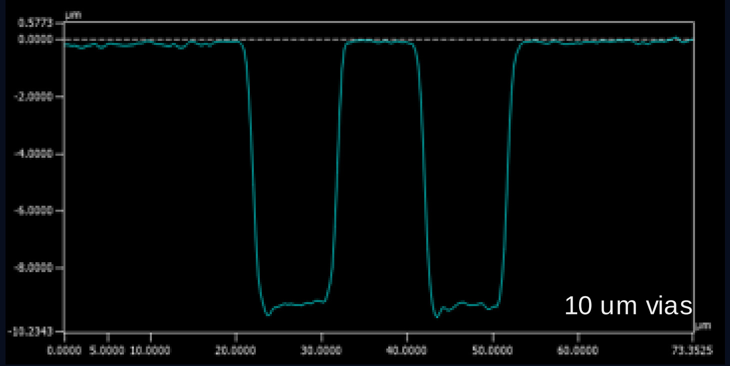
Diameter: 5um
Depth: 25 um



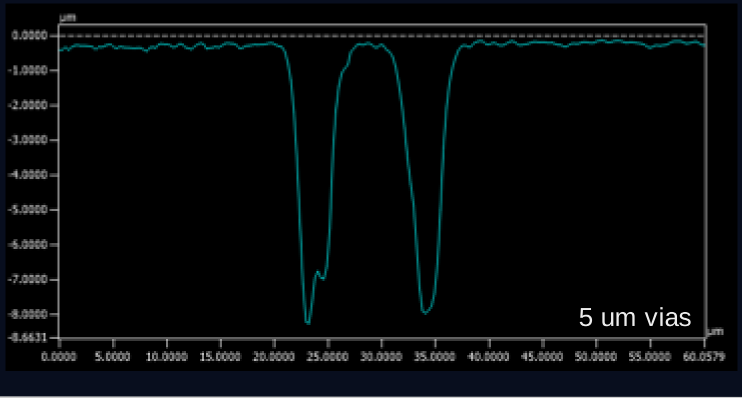




100 um vias



10 um vias



5 um vias

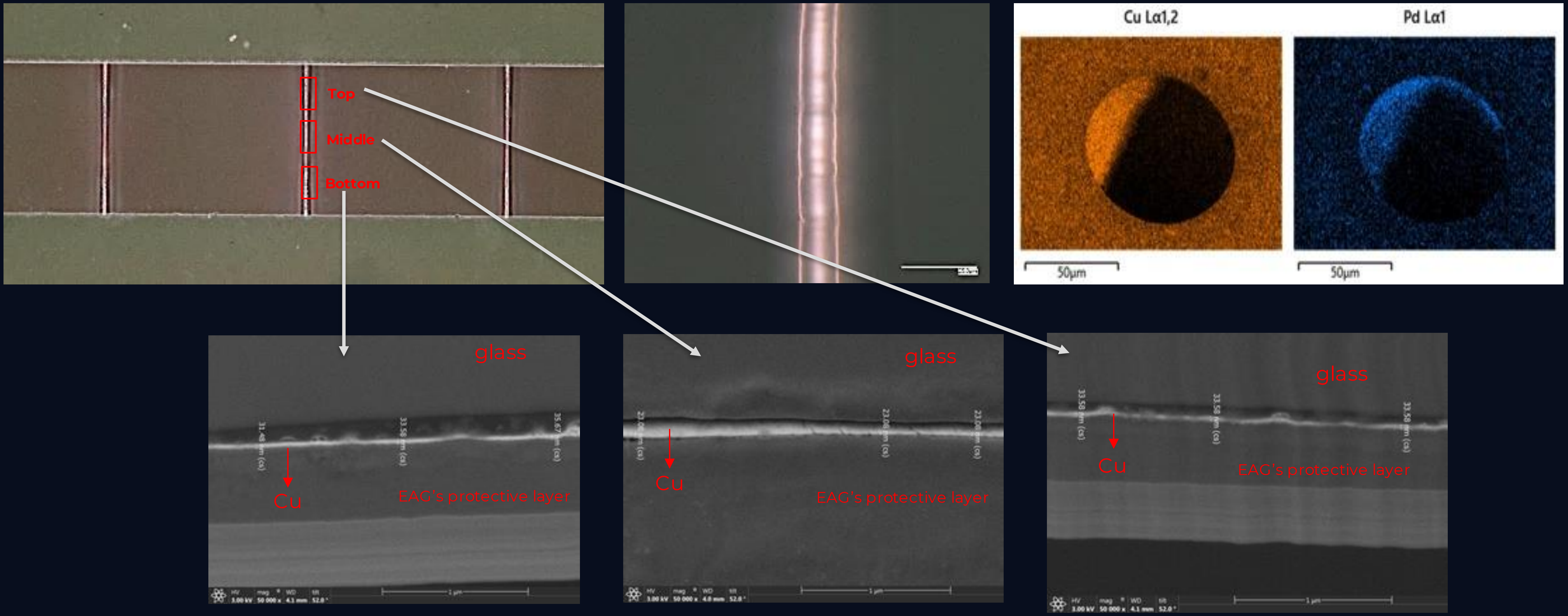
4. Metallization of Glass Substrates & TGV

Applying LMI$_X$® to Glass Core Substrates with High-AR TGVs

Glass Core Substrates			
Benefits	**Challenges**	**Current State of Art**	**Advantage of LMI®**
Superior dimensional stability	Poor adhesion	Surface roughening prep: E.g. Kr-F excimer laser	Low cost processing (dip, spray, spin coat)
Low CTE (matched to silicon)	Difficult to form and plate TGV	Adding adhesion prometers via complex surface treatments	Low temperature (180C max)
Exceptional thermal stability	Brittle & difficult to handle	High temp. processing: E.g. M-Ox	100% E'less step coverage in high-AR TGV
Low moisture absorption	Expensive processing	Expensive, processing and equipment needs	Excellent TGV adhesion and anchoring
Electical performance (low Dk & Df)			Demostrated on both Corning and Schott glass panels

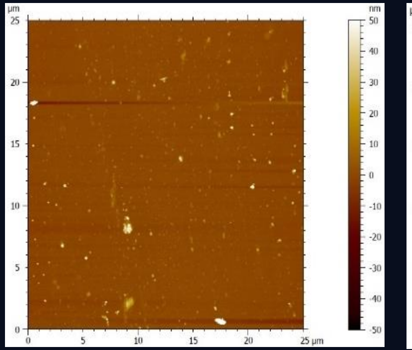
Glass Substrate & Through Glass Via Low-Temp Metallization

Schott Borofloat-33 Glass 650um Thickness, 50um Via,
13:1 AR TGV with LMI_x® and Electroless Copper

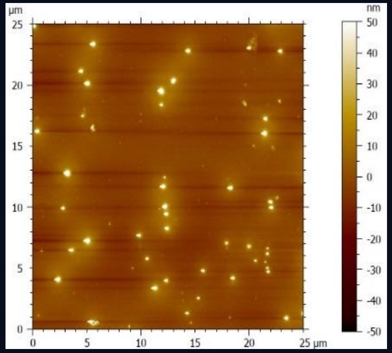


Enabling Glass Substrate & Through Glass Via Low-Temp Metallization

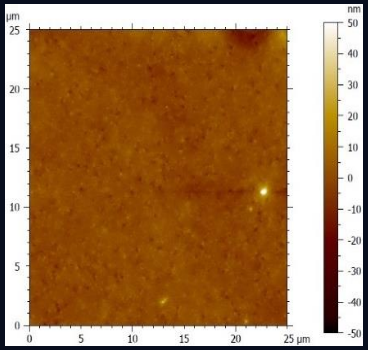
Bare Borofloat-33 Glass
Scan size=25x25um
Sa=1.312nm



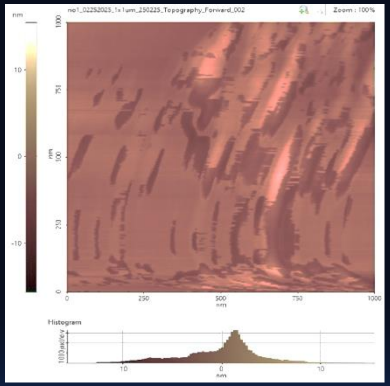
Adh. Promoter
Scan size=25x25um
Sa=3.855nm



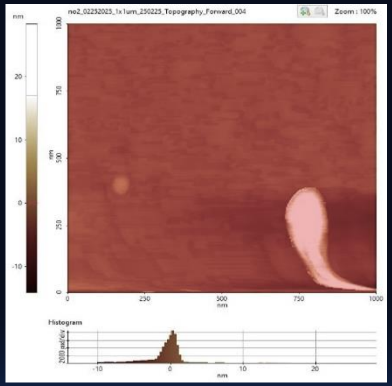
After LMI$_x$® + E-less Cu
Scan size=25x25um
Sa=2.061nm



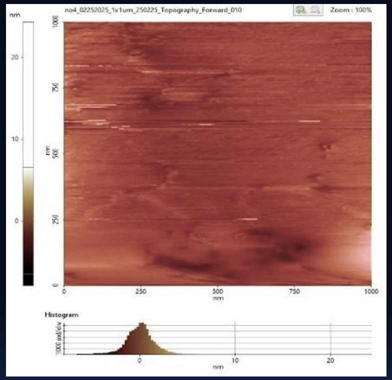
Scan size=1x1um
Sa=3nm



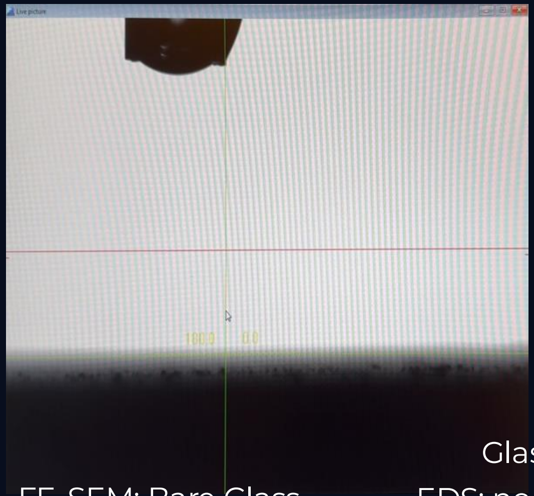
Scan size=1x1um
Sa=2nm



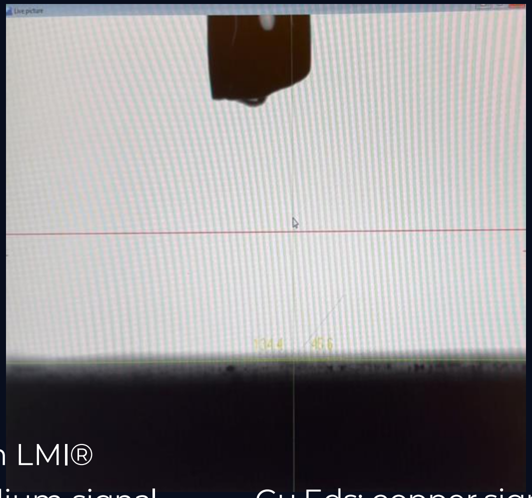
Scan size=1x1um
Sa=1.2nm



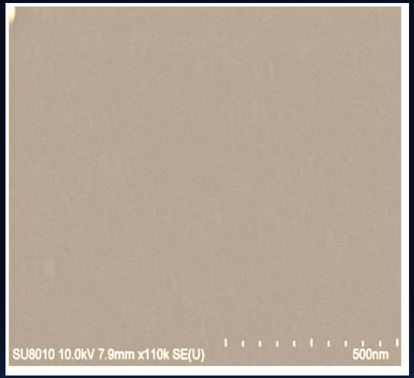
Aqueous solution
Borofloat-33 Glass with via



LMI$_x$® drop on Borofloat-33 Glass with via
¼ playback speed

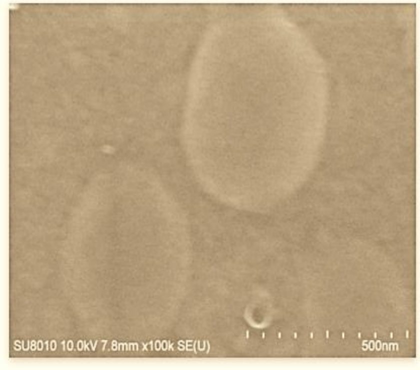


FE-SEM: Bare Glass



Glass with LMI®
EDS: no palladium signal

Cu Eds: copper signal



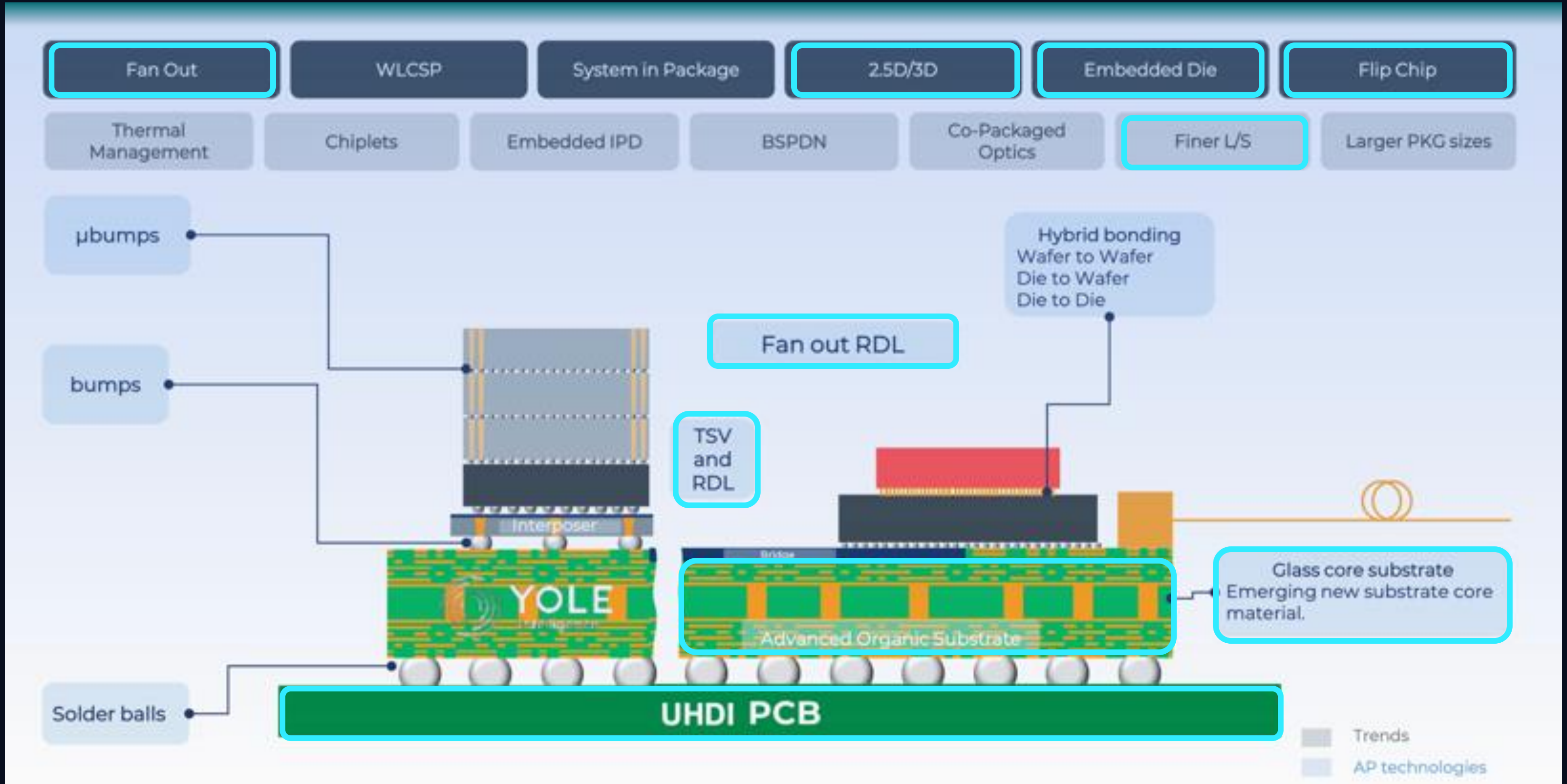
Glass Substrate & Through Glass Via Scorecard

Performance		
Specification	**Value**	**Characterization Method/ Partner**
E'less Cu Thickness	30-50 nm	X-SEM/ EAG
Cu sheet resistance	3.1 ohm/ square (high due to oxide formation)	4-point probe sheet resistance / in-house
Cu Roughness	< 5 nm	AFM / Covalent & SJSU
**Nano-scratch on E'less Cu*	16.5 ± 1.4 mN by 5 µm sphero-conical indenter	Nano-scratch / Covalent
Cu Adhesion	Class 5B	Cross-hatch test (ASTM D3359) / in-house
Conformality / Continuity	100% Continuous with Good Conformality	SEM / EAG EDX / Covalent

*** The critical load at delamination was measured as 16.5 ± 1.4 mN across five scratches. The corresponding depth profile shows a residual depth of ~ 40 nm at the delamination point, confirming that the copper layer has been penetrated.**

Enabling Glass Substrate & Through Glass Via Low-Temp Metallization

Yole's 2025 Overview of High-Performance Computing Architecture



Areas Addressed by $LMI_x^{®}$

Thank You

LQDX

www.LQDX.com

IMAPS DPC March-04-2025, Arizona USA