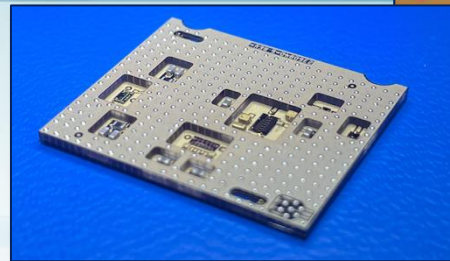
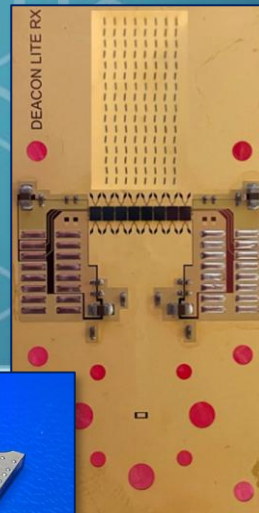
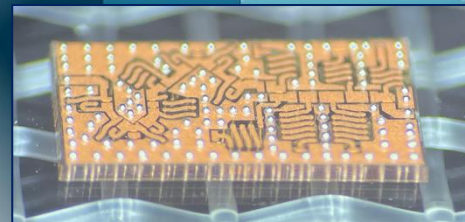




3D Heterogeneous Integrated RF Systems-in-Package using Glass Packaging

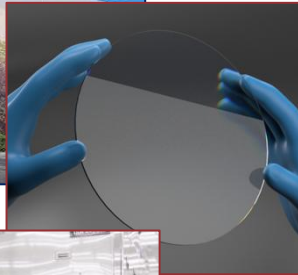
Jeb H. Flemming
CTO/Founder of 3D Glass Solutions





About 3D Glass Solutions

What do we do and why is it different?



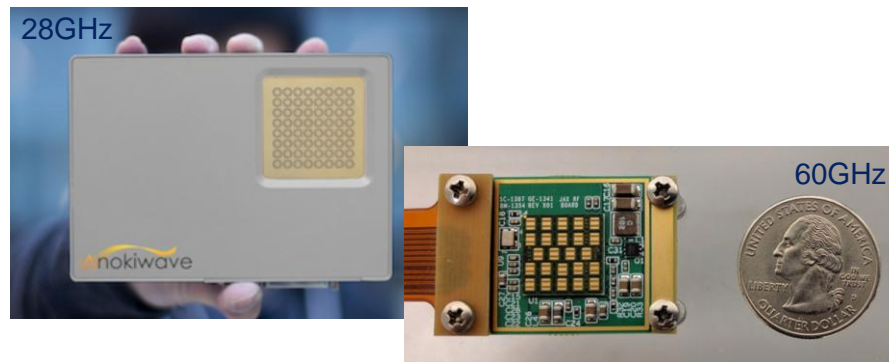
- A provider of advanced electronic packages with substantial Size, Weight, and Power reductions (SWAP) to enable a new generation of electronic devices using glassy materials
- Full turnkey manufacturing: Design → Wafer Fab → Assembly → Test
- Enabling major advancements in:
 - Millimeter wave applications
 - High performance antenna, electronic warfare, counter-electronics
 - High performance computing, silicon photonics and DoD special programs.
- Headquarters and **40,000 Sq. Ft. of advanced manufacturing space** in north Albuquerque, USA.
- Lockheed Martin & In-Q-Tel as major investors and board member
- **Flight legacy on F-35 and IC Satellites**
- ITAR Compliant, ISO:AS9100 qualified, 100% US manufacturing
- Foundational IP, with market leading customer base, and product/results to support world class performance claims

Key drivers: substantially reduced SWAP, RAD hard, high temperature, 3D Heterogeneous Integrated systems-in-package

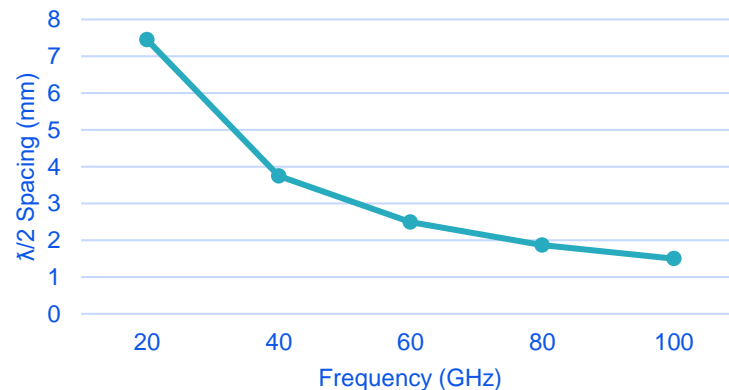
Challenges in SiP Systems for Phased Arrays

- ▶ Higher frequencies enable:
 - Higher communication throughput
 - Higher resolution radar
- ▶ Higher frequencies require:
 - Tighter antenna spacing
 - More complex SiPs
- ▶ RFFEs becoming more complicated
- ▶ Beam forming ICs are too expensive and take too long to develop
- ▶ 3DHI solves fundamental RFFE development cost problems while meeting demanding size constraints

Leverage the Z-Dimension to package more functionality in a fixed footprint



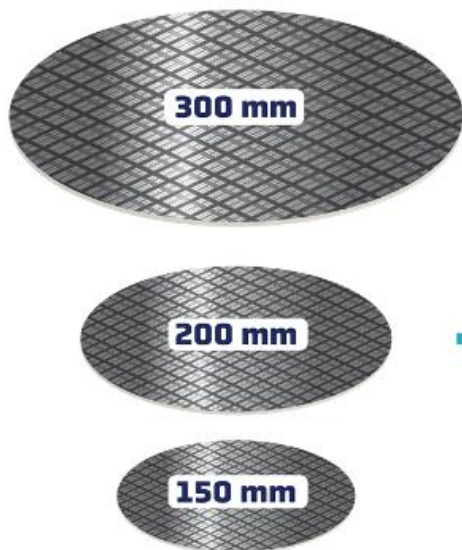
Frequency vs. Antenna Spacing



3D Heterogeneous Integration

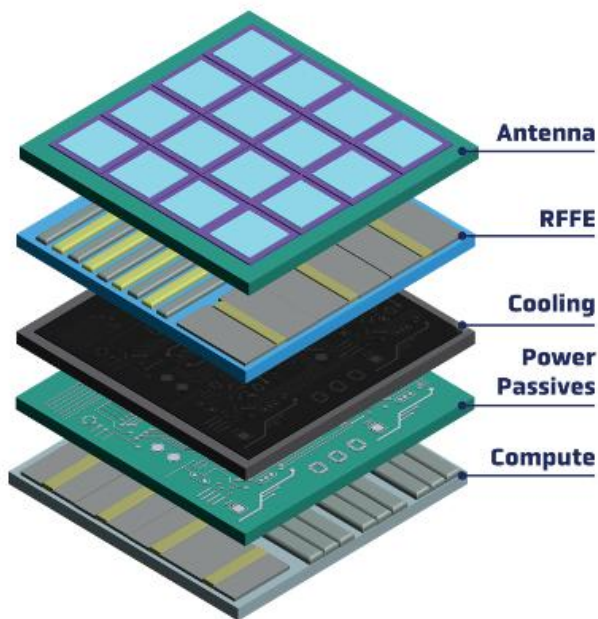
3DHI components

Wafer Fab



3DHI layers

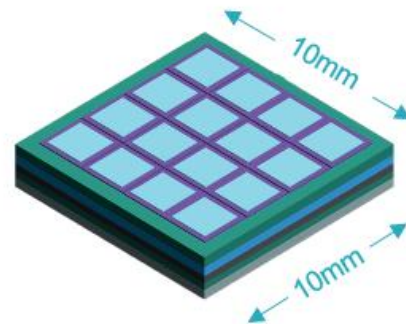
Glass Packaged Layers



3DHI microsystems

System-in-Package (SiP)

>90% Reduction in Size
>90% Reduction in Weight
Lower Power Consumption

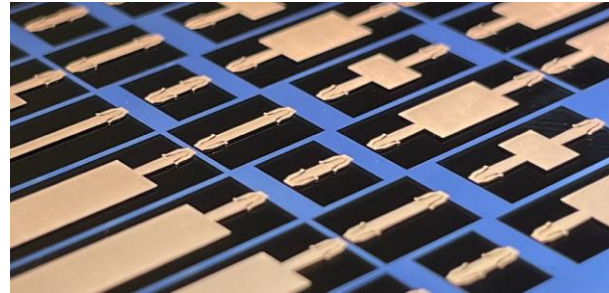


Why Glass?

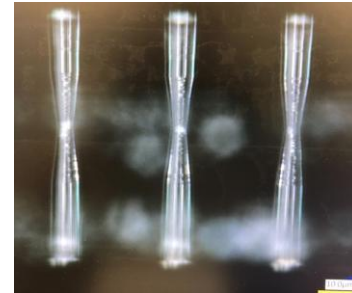
- ▶ Chemistry
 - Benign, rad-hard, high temp stable
 - Great for shock and vibe (compression)
- ▶ Hundreds of compositions to choose from
 - More glass types than PCB types
 - Signal conditioning (Digital & RF)
 - CTE
 - Index of refraction
- ▶ Performance gaps do exist with glass
 - Limited to TGVs only
 - Trend towards lower CTE
 - Bow, low copper content, reliability
 - Cannot integrate deep cavities and conductor undercuts
 - Low coefficient of thermal transfer
- ▶ Photo-sensitive glass fills this gap

	Glass Name	CTE	DK	Df	Frequency
1	PSG	8.53	6.4	0.014	10 GHz
2	HPFS	0.52	3.8	0.00002	10 GHz
3	EXG	3.17	5.3	0.003	1 KHz
4	7070 Glass	3.20	4.1	0.0033	50 GHz
5	Pyrex/Borofloat	3.30	4.5	0.0065	10 GHz
6	Low-Loss Coring	3.26	4.6	0.0037	10 GHz
7	Low-Loss Schott	3.29	4.0	0.0021	10 GHz
8	EA-N1	3.80	5.5	-	10 GHz

HPFS Fab at 3DGS for mmWave



EXG at 3DGS for HPC



3DGS has a complete manufacturing line
for standard glassy material fabrication

Photosensitive Glass (PSG) Ceramic

▶ Low loss

- Variable (1.5 - 6.4) dielectric constant
- Smooth surface: enables low-loss, multi-layer copper RDL interconnect with minimal surface resistance on both sides

▶ 8.5ppm/°C CTE

Closer to copper's CTE (16.7ppm/°C CTE) than silicon (2.6 ppm/°C) and fused silica (0.6 ppm/°C)

▶ Use of an inexpensive wet etch process for 3D glass structuring:

- Dense arrays of through glass vias (TGVs)
- Empty substrate integrated waveguides (eSIWs) and high gain antennas

▶ Ultra-low electrical and thermal resistance and parasitics (short path lengths) resulting from:

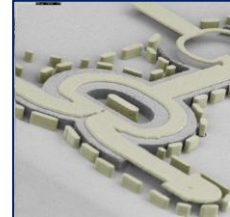
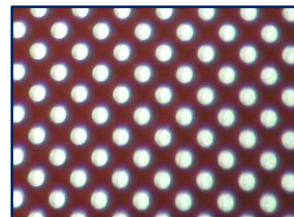
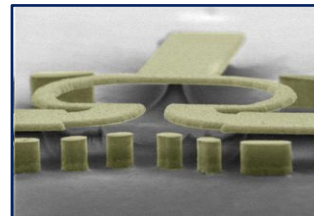
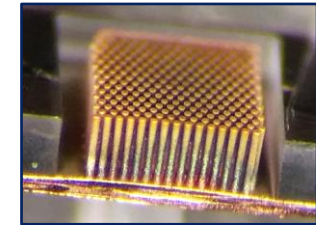
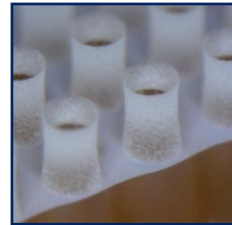
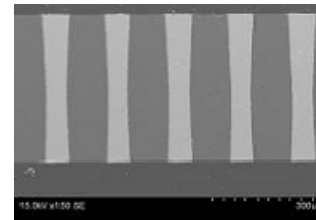
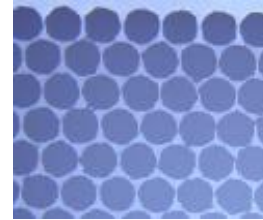
- Dense TGVs
- Multi-level RDL interconnects

▶ Glass between the TGVs provides excellent electrical and thermal insulating properties

Minimize crosstalk

▶ Ideal material for harsh environments

- Radiation hardened and capable of withstanding high temperatures (>600C)



3DHI Layer Process Flows Descriptions

- ▶ Individual 3DHI layers may be treated individually as a stand-alone device layer
- ▶ Mix and match 3DHI layers to build desired 3DHI microsystems

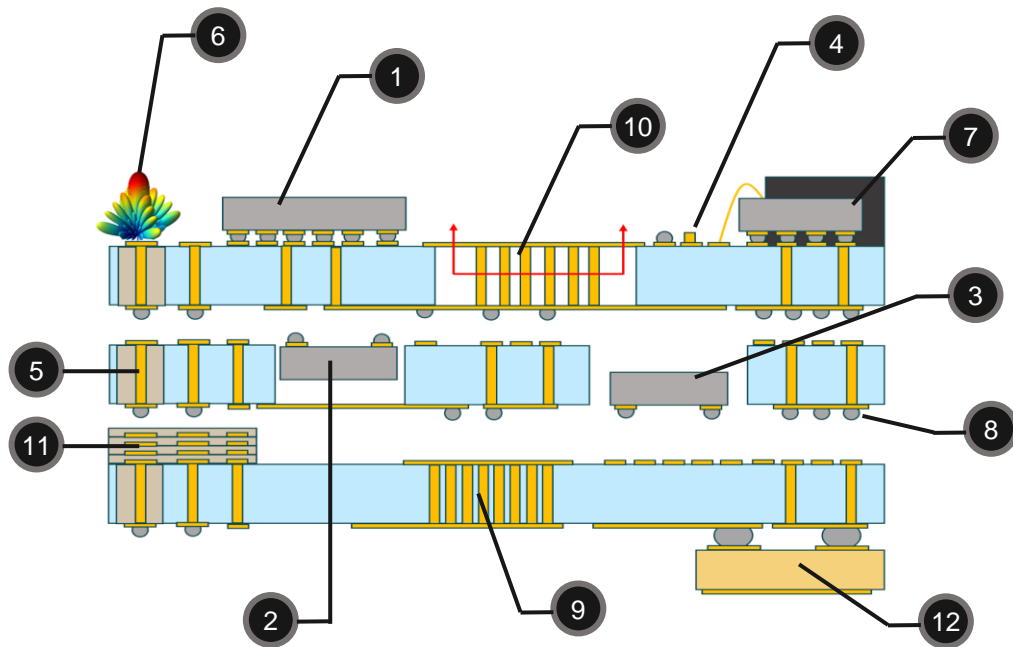
#	3DGS 3DHI Layers	Existing PDK	Description
1	Interposer + Cavity	Yes	• High gain antenna, EW
2	RF-Integrated Passive Device (IPD)	Yes	• Switched filter matrix (DARPA WARP), RFFE, EW, RF signal conditioning
3	RF/Digital Interposer		• High Performance Compute • Interposer, mmWave RFFE, mmWave RFIC interposer
4	Substrate Integrated Waveguide (SIW)	Yes	• Antenna in package, directed energy, high gain antenna, EW
5	RF Interposer + Cavity	Yes	• Broadband RF signal conditioning

3DHI Layer Assembly



6-12GHz Half-Duplex Tx/Rx
 4 3DHI Glass Layers
 Layer IDs: PCB, 2, 1, 2, 1

1. Silicon and III/V integration – GaAs, InP, etc.
2. “Picture frame” fully shielded embedded die
3. “Window frame” fully shielded embedded die
4. Pillars, bumps, wire bonds, TCB, etc.
5. Vertical coaxial transitions
6. On-package antennas
7. Underfill and Overmold
8. Low-loss metallic interconnects
9. Thermal vias (80W/mK)
10. Embedded microfluidics for advanced cooling
11. Multi-layer redistribution layers
12. PCB integration

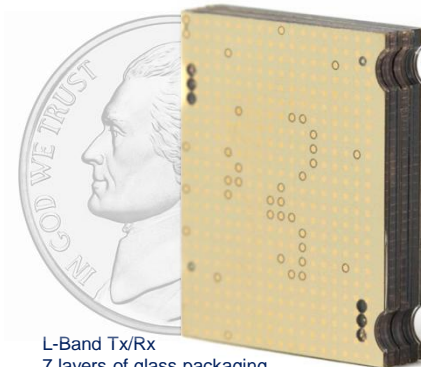
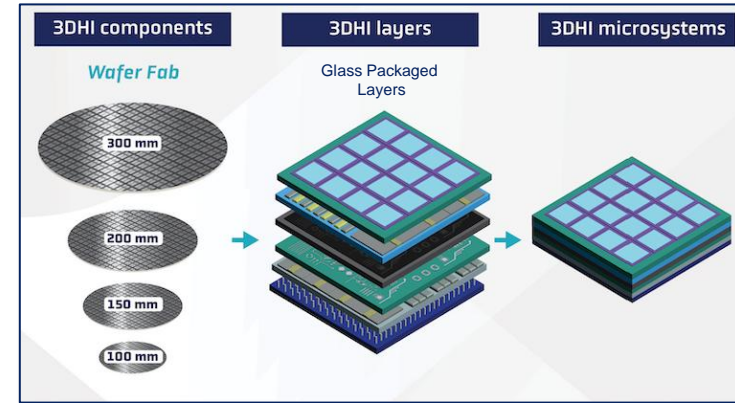




What is New in our Approach?

The World's First 3D Heterogeneous Integrated System-in-Package Technology

- ▶ **True 3D**
 - Reduce system size by stacking multiple glass substrate layers in the Z-dimension
- ▶ **True heterogeneous integration**
 - Integrate CMOS, GaAs, GaN, SiC, Si, SiGe, SMT capacitors, packaged die, and others into a single system-in-package (SiP)
- ▶ **Integration friendly**
 - Wire bonding, flip chip, SMT solder, and other approaches proven
- ▶ **Substantially reduce Size, Weight, and Power (SWAP)**
 - 60-98% reduction in size
 - 50-80% reduction in weight
 - >20% less power consumption
- ▶ RAD Hard, temperature stable up to 600C
- ▶ Fully RF shielded system-in-package
- ▶ BGA or LGA assembly directly to a PCB



L-Band Tx/Rx
 7 layers of glass packaging
 19mm x 22mm x 3.3mm (thick)
 >30 SMT, wire bonded, & flip chip parts inside
 US Nickel for size perspective

Electronic Warfare

- Tunable Filters: 3DHI assemblies enable substantial SWAP-C reduction by utilizing 3DGS high-Q inductors and RF switch integration with varactors

RF Front Ends

- Large system (BOM) aggregation from antennas to bits (compute). High density and low loss interconnects improve performance and reduce size. Embedded cavities mitigate interference concerns

Beam Forming Tiles

- Use modular scalable beamforming tiles for large scale phased arrays. Tight $\lambda/2$ spacing at high frequency requires 3DHI. Integrate PA + LNA in glass tile under antenna

High Performance Compute for ML/AI

- Integrate multi-layer 3DHI for compute & power passive integration in a true 3DHI package

#	3DGS 3DHI Layers	Existing PDK	Description
1	Interposer + Cavity	Yes	• High gain antenna, EW
2	RF-Integrated Passive Device (IPD)	Yes	• Switched filter matrix (DARPA WARP), RFFE, EW, RF signal conditioning
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3DHI Layer Assembly



6-12GHz Half-Duplex Tx/Rx
 4 3DHI Glass Layers
 Layer IDs: PCB, 2, 1, 2, 1

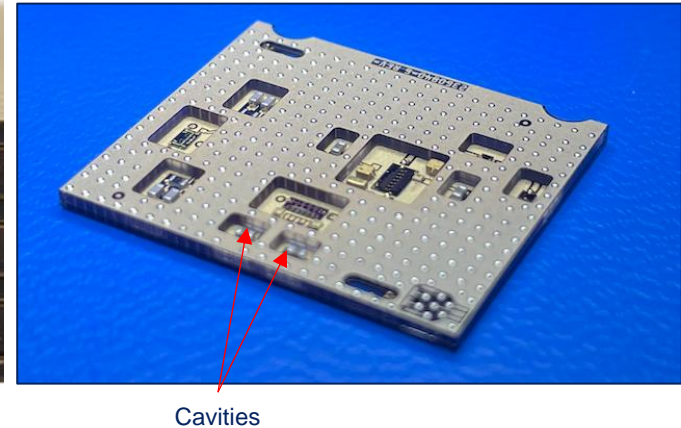
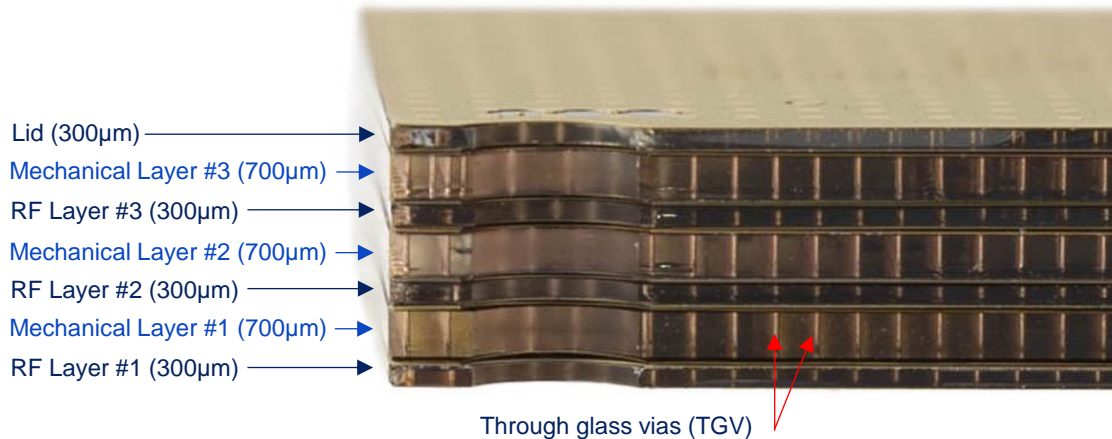


Glass Stacking Overview

Moving in the Vertical Dimension

3DGS has developed assembly processes for multi-layer glass assemblies

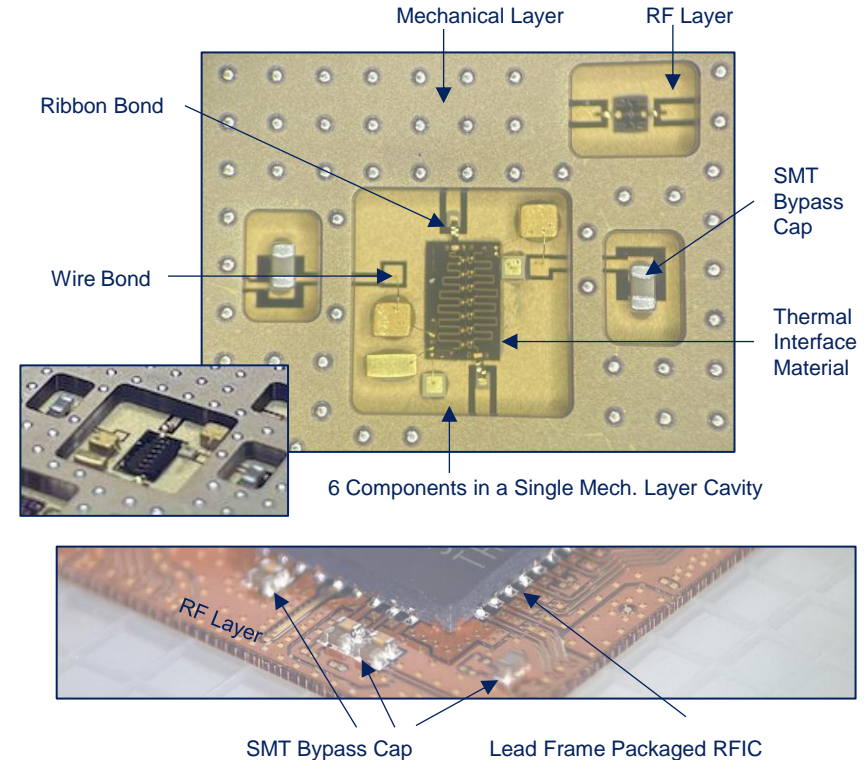
- ▶ **RF Layers:** Main electrical layer used for routing and to assemble active and passive die. Mix and match die from different processes to achieve desired performance and density.
- ▶ **Mechanical Layers:** Create room for assembled die (including wire bonds) by using cavities. Create controlled impedance traces including vertical transitions (digital, ground, and 50Ω).
- ▶ **Glass to Glass Bonding:** Vertical connections accomplished using low loss metal interconnects.



Component Integration Capabilities

Proven, Reliable, and Scalable

- ▶ 3D integration reduces interconnect lengths improving insertion loss, latency, and power efficiency.
- ▶ All thick copper redistribution layers use ENEPIG surface finish to enable a broad array of assembly techniques
 - SMT onto glass
 - LGA/BGA packaged die onto glass
 - Wire/Ribbon bond
 - Flip Chip
 - Conductive epoxy
- ▶ Integrate with multiple types of assembly thermal profiles
 - AuSn → SAC305 → Sn63 → Indium → Sn93 → conductive epoxy
- ▶ While system level reliability is heavily dependent upon actual design and layout, individual assembly techniques have been proven reliable by 3DGS and our customers.





The Power of Cavities

Mini-Faraday Cages

Cavities perform several important functions

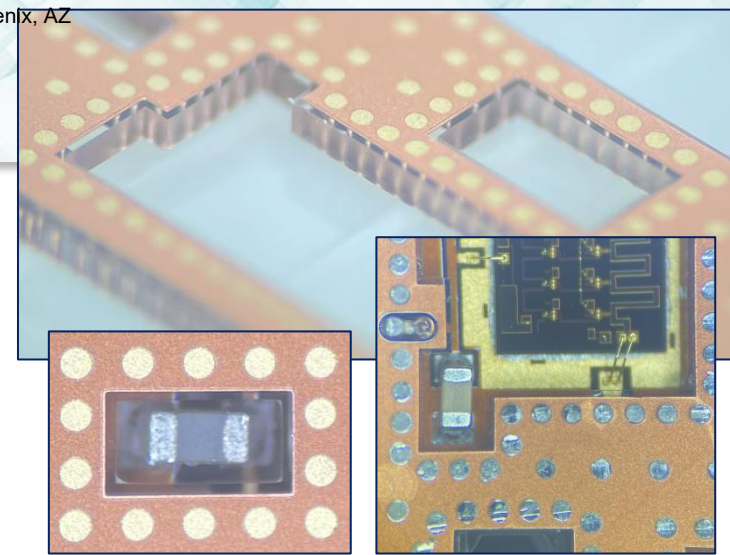
► Embedding ICs

- Cavities provide space for embedded die and their electrical connections (e.g. wire bonds) to exist between layers
- Complex shapes and outlines are easily produced
- Minimum cavity size = $200\mu\text{m} \times 400\mu\text{m}$ enables the isolation of even the smallest SMT parts

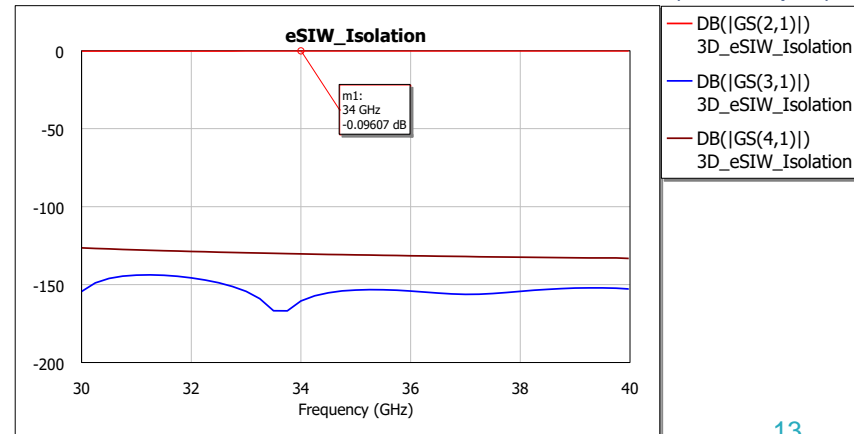
► High isolation

- They provide 6-sided isolation to adjacent chips with TGV ground fence along edge of cavities to form micro-Faraday cages.
- Achieve up to 60dB of isolation between adjacent cavities spaced only $300\mu\text{m}$ apart

- Metal etch stop can also be included on one side of cavity to form a lid, fully enclosing the cavity



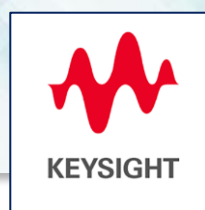
Simulated Isolation with three rows of TGVs (60/120 μm)





Connecting Glass Layers

RF 3DHI – High Frequency Performance



Create low-loss high frequency controlled impedance transitions between glass layers

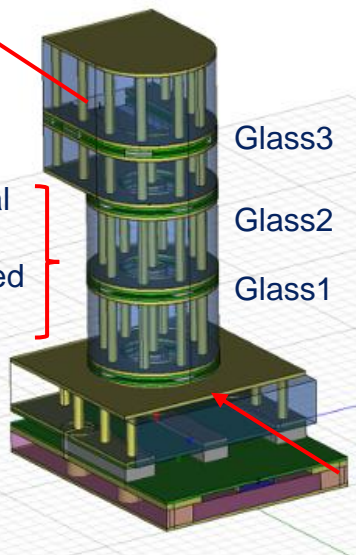
CPWG

- RF trace = 160um
- Space = 67um

Silver

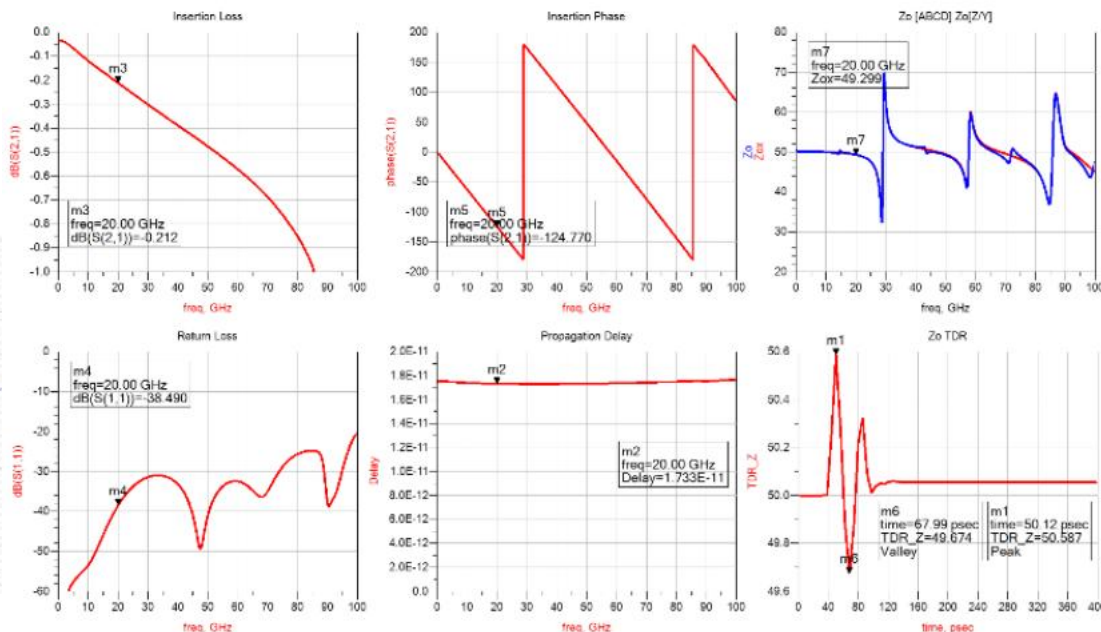
- Diameter = 120um
- Height = 50um

RF_{OUT}: Glass 4



Center signal and ground vias optimized for 50Ω

RF_{IN}: PCB

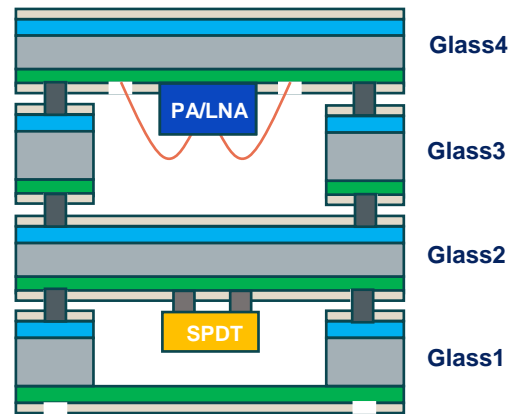
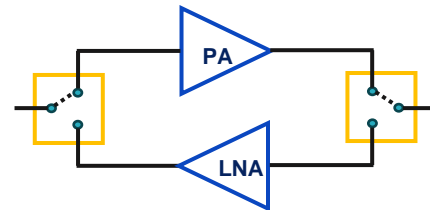
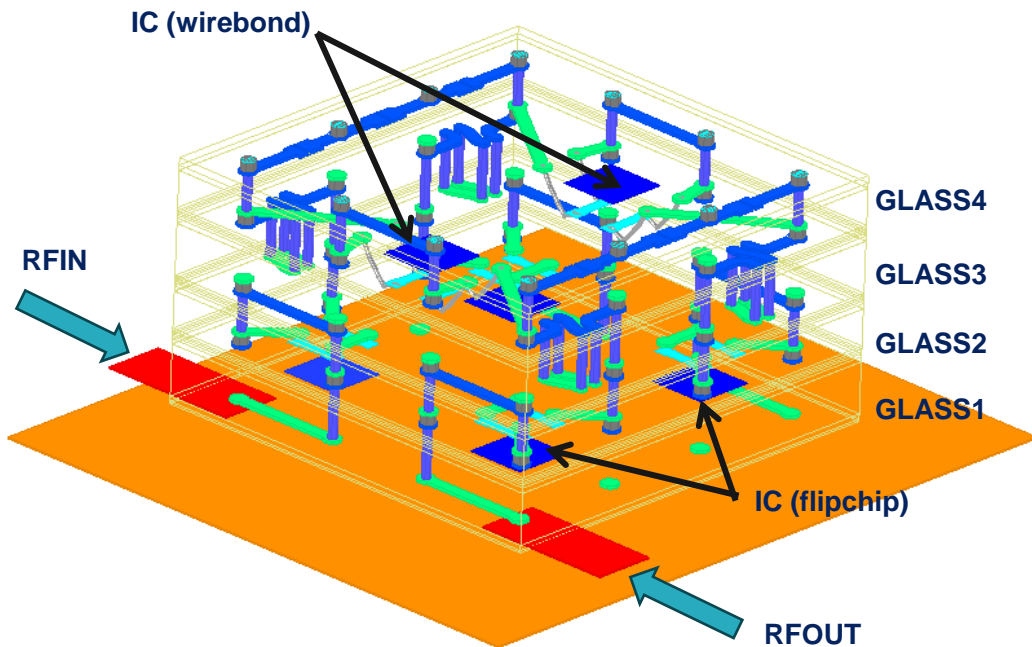




ADS 3DHI Layout of Multiple Glass Layers



- Each glass layer design (4x) and IC (2x) requires its own library before assembly.
- Glass libraries shown use this PDK.
- Assembly occurs in top level PCB library (parent) using smart mount with 6 child libraries added in.
- Cavities created in glass layers 1 and 3 to create room for ICs assembled on glass layers 2 and 4.



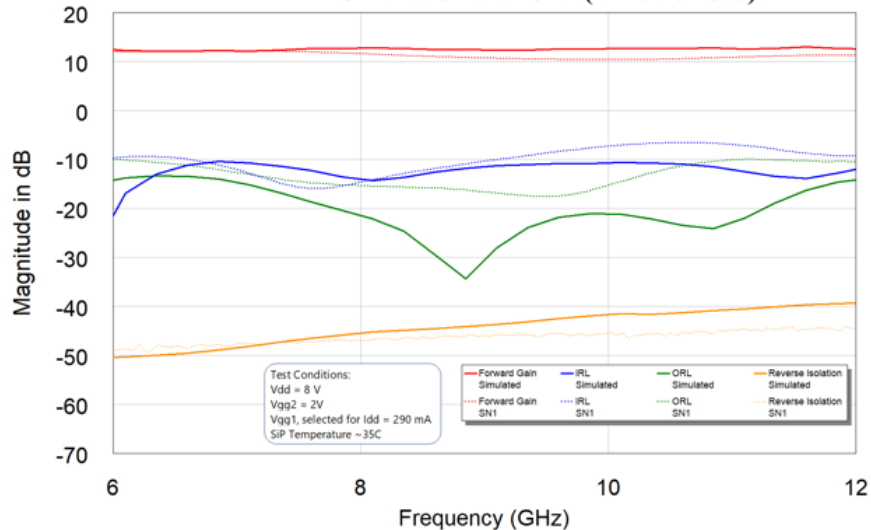


6-12GHz Half Duplex Tx/Rx

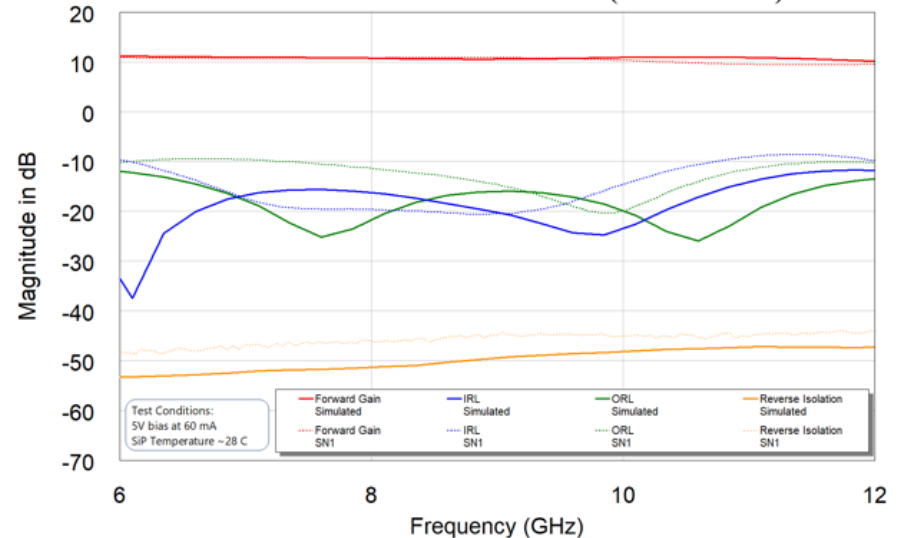
- 14 embedded devices (LNA, PA, switches, caps, etc.)
- 5 watts operation
- 60% reduction in size
- 40% reduction in weight



MFM1 PA Simulation with SN1 (full de-embed)



MFM1 LNA Simulation with SN1 (full de-embed)





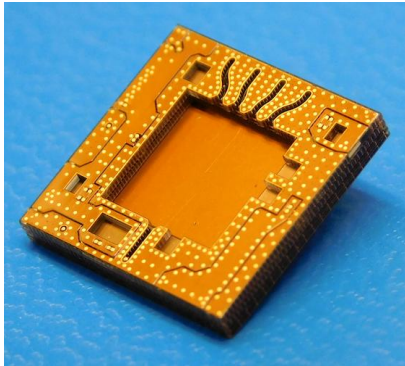
3DHI Thermocycling Reliability Test Data

500 Cycles

Measurements are a bit misaligned due to probe contact issues on solder ball pads

850 Cycles

- 4 Glass Layers
- 6-12GHz Wilkinson Power divider
- JEDEC A104, condition G: Thermocycling -40C to 125C

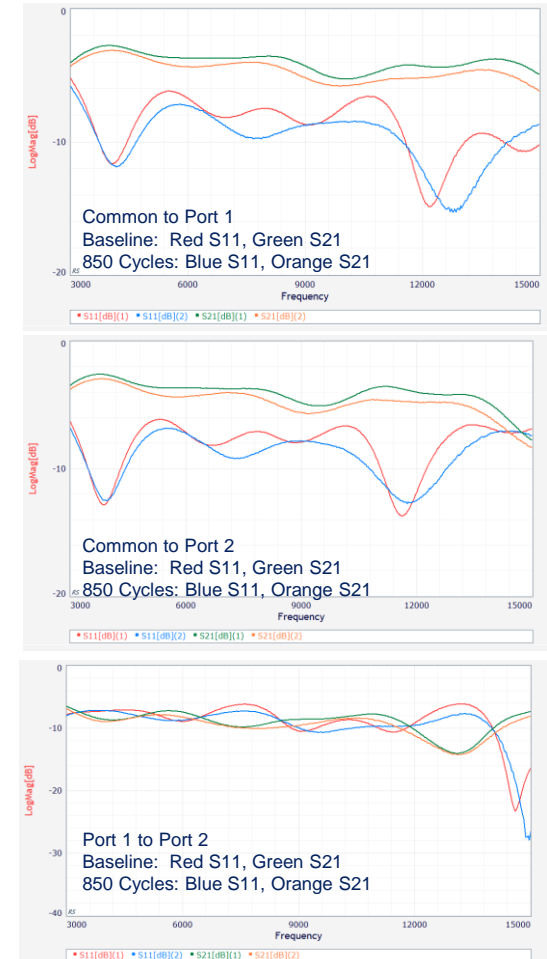
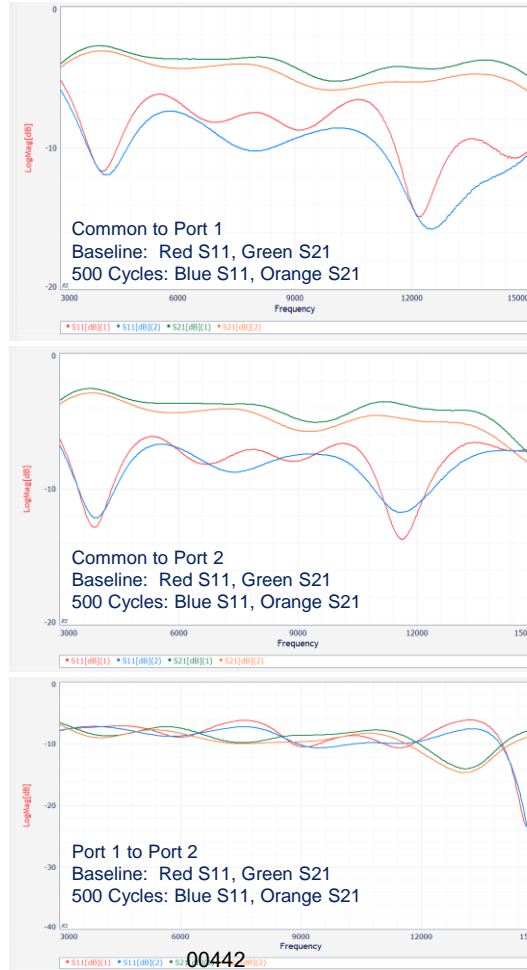


S2P Plot Collected:

- Common to Port 1
- Common to Port 2
- Port 1 to Port 2

Unused ports are not terminated

All probing was done on solder pads



Conclusion

- ▶ Beam forming has a critical need for Z-height maximization
- ▶ Glass offers the necessary first principles success criteria (CTE, strength, etc.)
- ▶ Developed....
 - Full design, production, and assembly ecosystem for glass stacking
- ▶ Validated excellent simulation vs. measured results
- ▶ Reliability testing shows strength and is ongoing



▶ Thank You

