Heterogeneous Integration of Magnetic Spin Wave and CMOS Chips Into a Hybrid Computing System

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Outline

1. Introduction of SWMG
2. Hybrid System Motivation
3. Hybrid System Concept
4. Packaging Results
5. Discussion & Outlook

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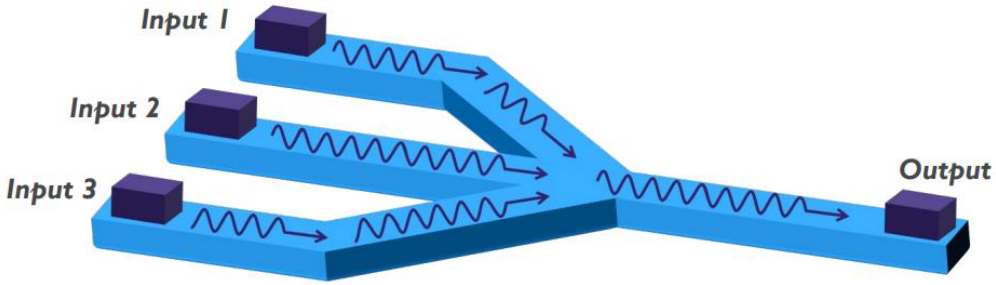
Introduction of SWMG

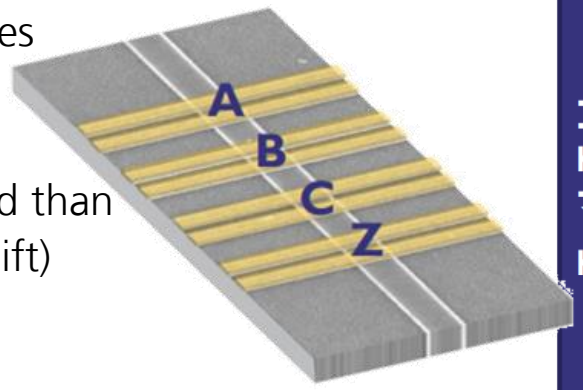
Spin Wave Majority Gate



- Schematic SWMG

What is spin wave majority gate computing?

- Downscaling of CMOS more complex, expensive -> SWMG alternative along other computing alternatives like quantum computing
- Spin wave majority gate: consist of uneven number of inputs, at least 3, superposition principal
- Antenna induces magnetic spin wave in wave guide, Receiver antenna induces current
- Different computational calculations possible (example of AI calculations)
- On Device development and testing, promises results with less energy needed than transistor (electron push over gate needs more energy than magnetic spin shift)
- On device working experimentally confirmed,
  but need to show a computing system actually doing a calculation



- Early test device by imec

Majority gate truth table

Truth Table	A	B	C	Z	
	0	0	0	0	AND
	0	0	1	0	
	0	1	0	0	
	0	1	1	1	
	1	0	0	0	OR
	1	0	1	1	
	1	1	0	1	
	1	1	1	1	

- Truth tabel

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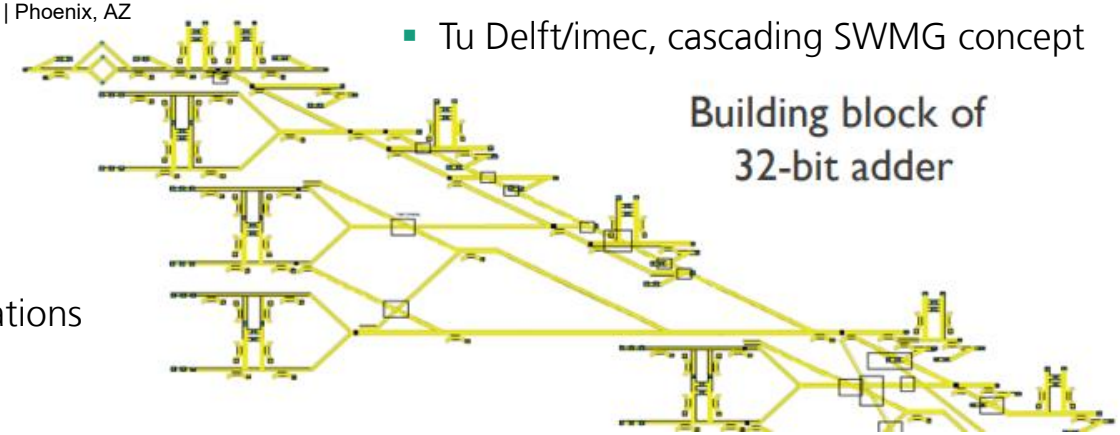
Introduction

Hybrid System Motivation

- Tu Delft/imec, cascading SWMG concept

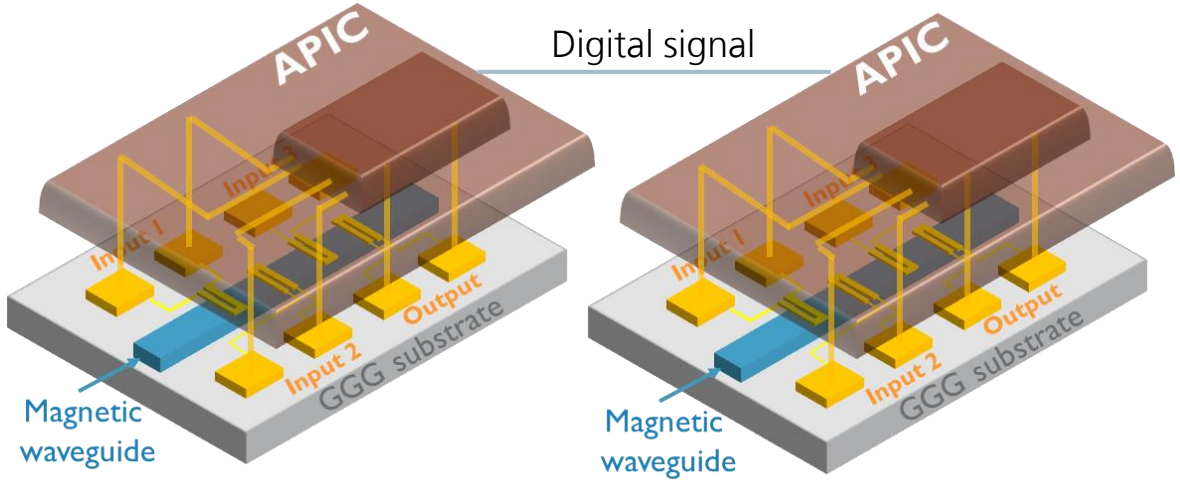


- Easy, known cascading through digital signal
- Low energy shift, different computations possible

Motivation

- Combining both strength of CMOS and SWMG
- First step from device to circuit level
  - First step to cascading (requirement for computing)
  - Circuit need more than just SWMG devices to work
    - Inverters, Couplers, Amplifiers
    - External magnetic field
- Simplification through APIC: Simplify the Spin wave circuitry for proof of concept of cascading (inverter, couplers amps over APIC)
  - Provide a first of a kind system with SWMGs
- APIC CMOS for input signal and output read out
  - Can account for small phase changes
- Combine both chips through an interposer assembly

simplify



SWMG Module 1

SWMG Module 2

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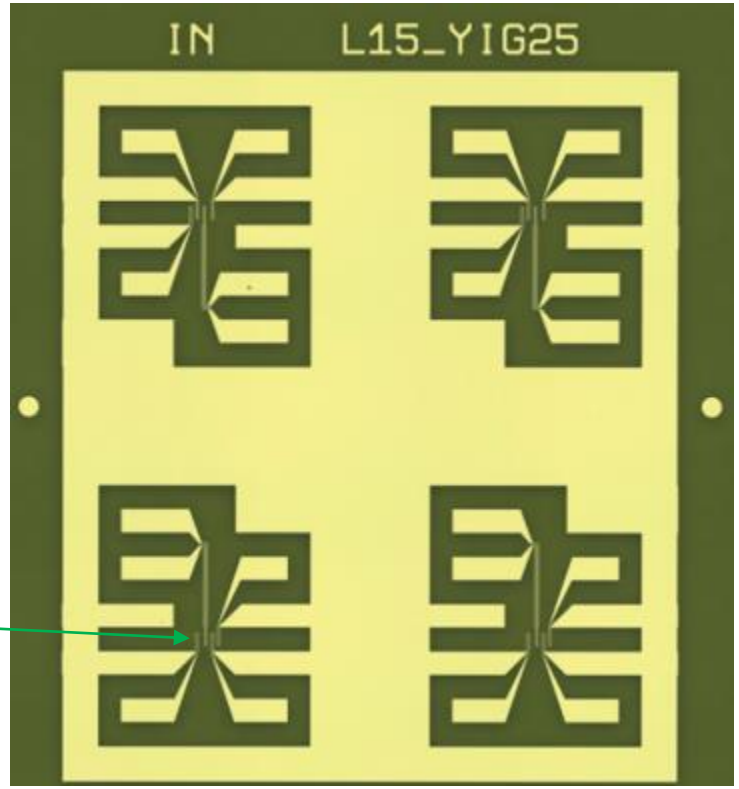
Introduction
Hybrid System Packaging

Challenges

- Novel materials for packaging:
  - $Y_3Fe_5O_{12}$ (Ytrium-Iron-Garnet, YIG) as wave guide
  - CoFeB as wave guide
  - $Gd_3Ga_5O_{12}$ (Gadullinium-Galium-Garnet, GGG) as carrier material
- Influence of packaging materials (ABF) on SWMG devices unknown
- Influence of interposer structure (circuitry, lanes, vias, etc.) on SWMG unknown
- SWMG not fully understood and optimized in detail
  - Need to control Phase shifts, delays, dampening, etc. (spin wave properties)
  - Dedicated APIC Design with many evaluation / measurement subsystems/circuits
- Open questions : APIC design, SWMG design, Interposer Design –> APIC should cover wide range of variations in RF /Spin wave design
- For cascading system many HF interconnects needed (~100) at 8Ghz



- YIG wave guide with gold antennas on GGG wafer: 4x SWMG devices

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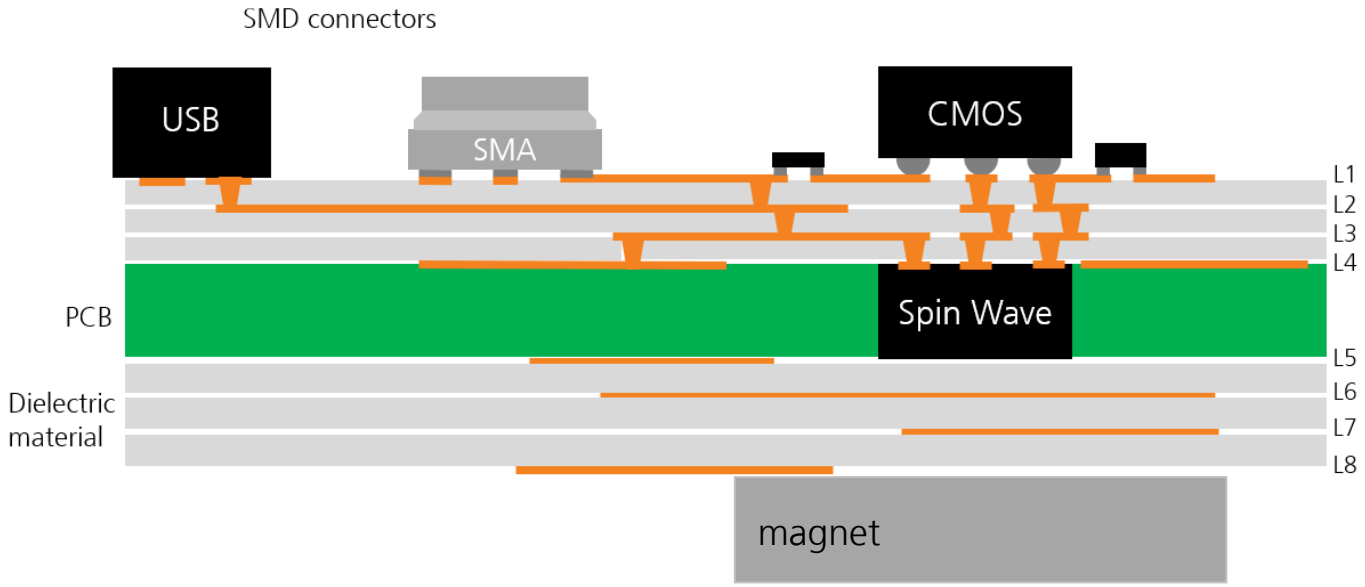
Introduction
Hybrid System Packaging

Concept

- Organic interposer panel technology was chosen, based on Ajinomoto Build Up Films (ABF)
- SAP process chain to structure interposer /RDL layers
- Fine line for fitting stacked SWMG/APIC (given pitch)
  - Fine line material for RF application available
- Advantage:
  - Fast design changes because of mask less LDI lithography
  - Low cost organic Interposer panel technology
- Stacking SWMG vertically with APIC via Interposer
  - Simple design to keep RF traces same length
  - Avoiding phase shifts/differences
- Combining interposer function with packaging function of SWMG by embedding in PCB Core



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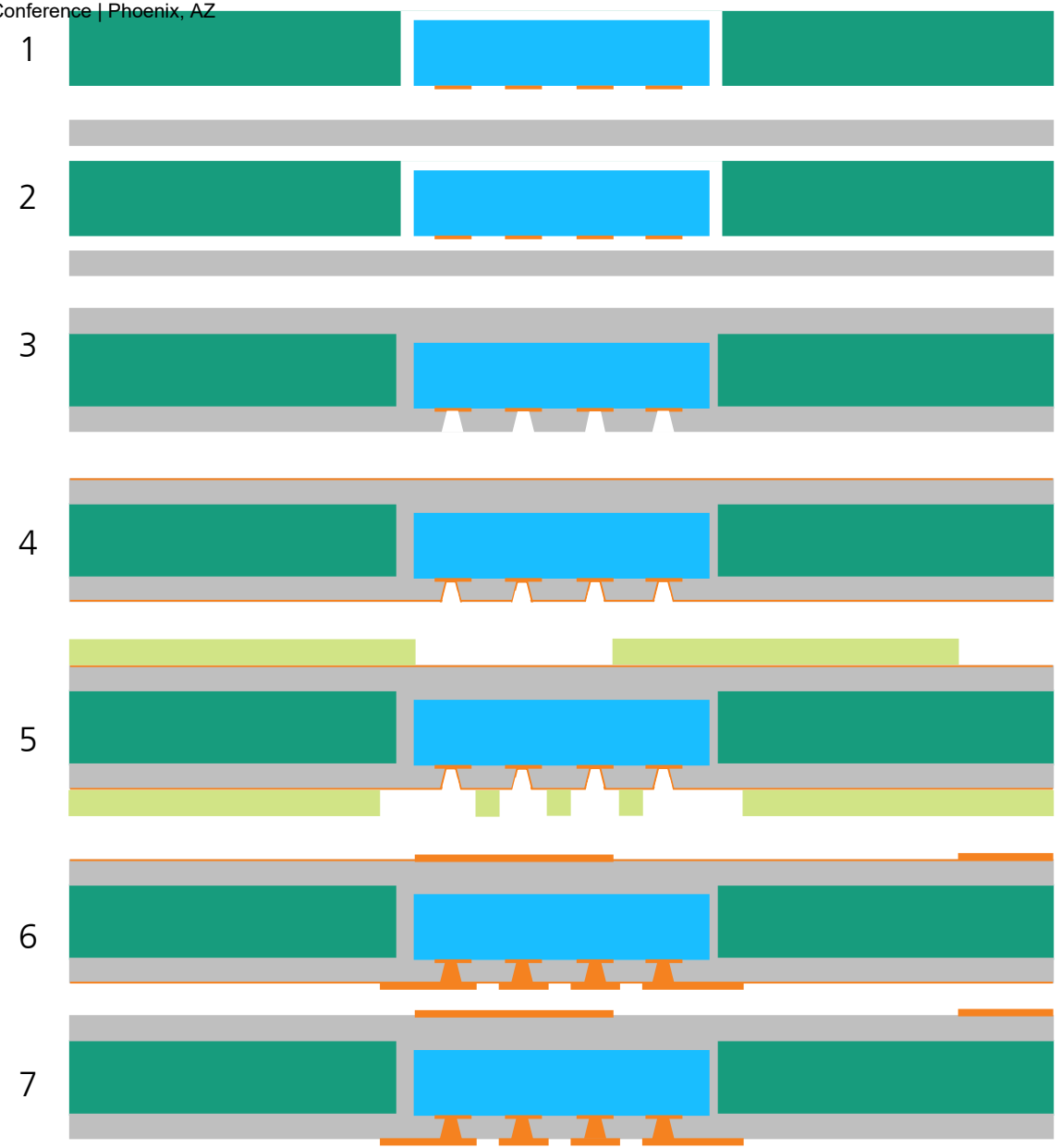
Hybrid System Packaging

Technology Approach

Concept Exkurs: Embedding and SAP

- Core with cavity – SW chip placed in cavity
- Lamination Step1: ABF from both sides, cavity need to be filled around SW chip
- Laser drilling to Chip pads: copper pads required with certain thickness for laser stop range, adaptive
- Sputtering of Cu seed layer for structures and Via fill
- Dry resist lithography
- Cu-plating of lines and Via fill
- Seed layer removal with plasma etch, alternatively wet etching
- Next build up layer starting from step 2



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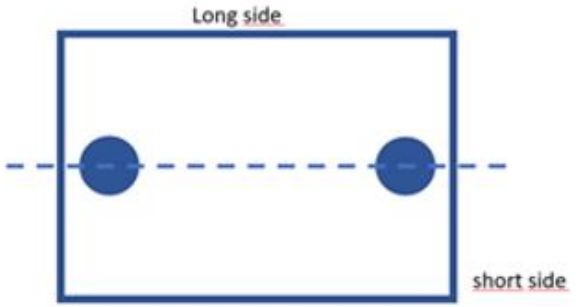
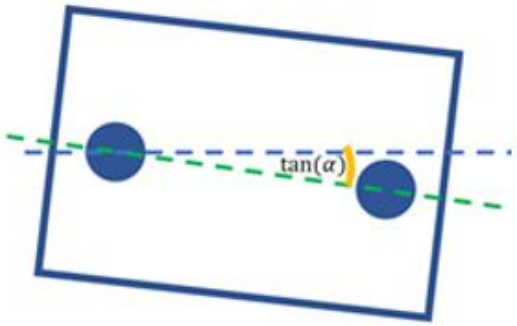
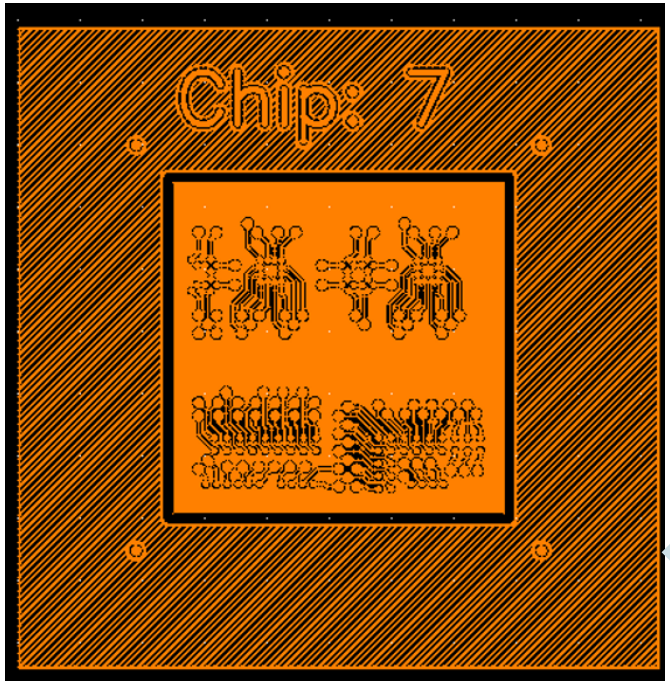
Hybrid System Packaging
Technology Approach

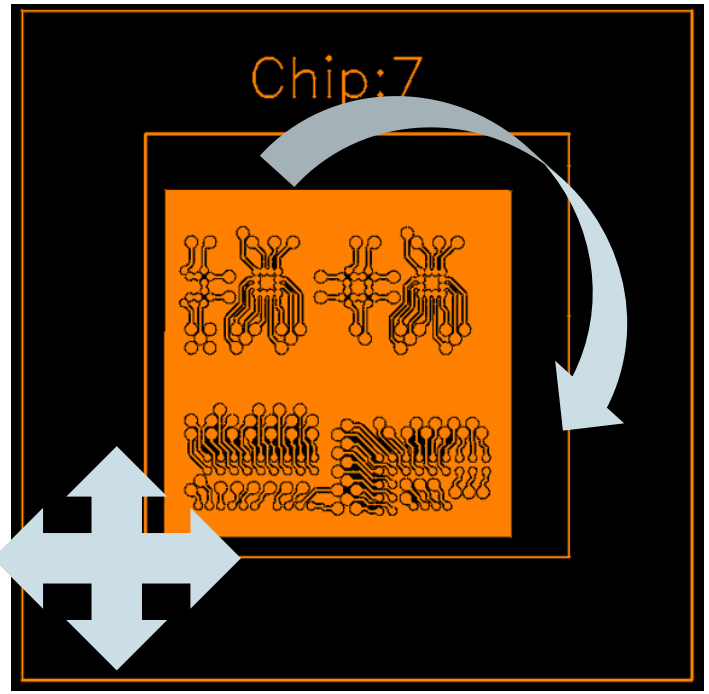




Concept Exkurs: Adaptive Layout

- After embedding adaptive layout required
  - Fitting design to exact position of chip
  - Accounting for x-y movement and rotation in embedding process
  - Allows for fine pitch vertical interconnections
- Adaptation for each chip, automatization possible





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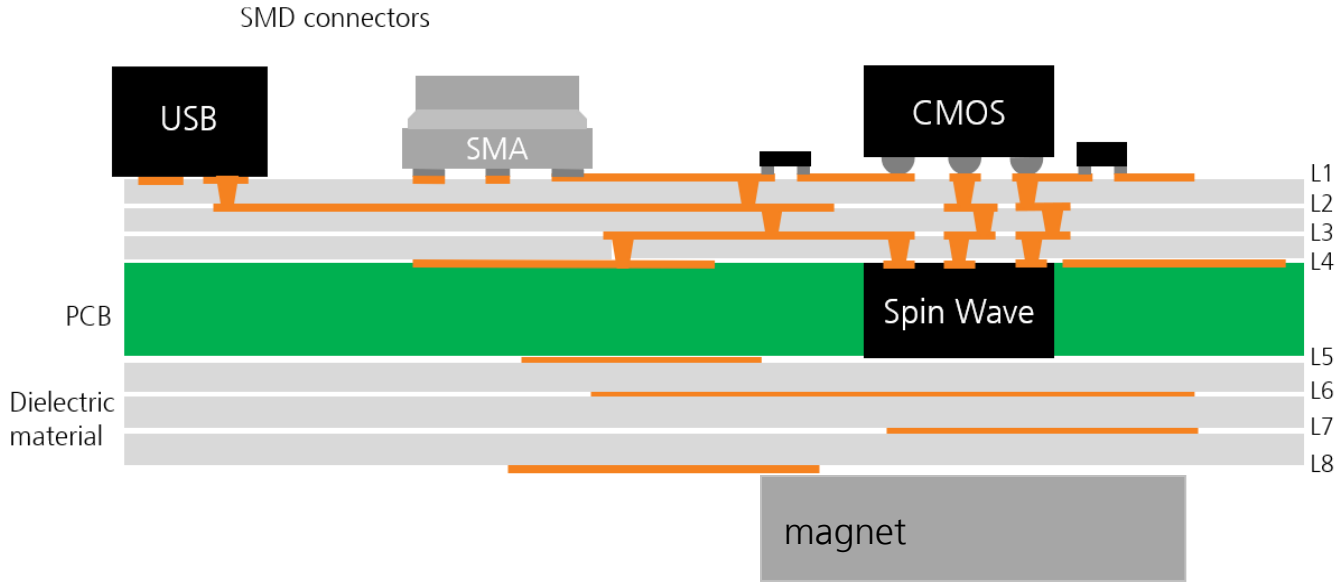
Hybrid System Packaging

SPIDER concept

Concept

- External magnetic field required for SWMG functionality
  - Can be provided with magnet laminated to backside
- Multiple variations of the design as evaluation boards to investigate each component of the hybrid system:
  - Interposer (e.g. RF losses, impedance, transitions)
  - APIC (digital to analog converters, phase shifts/ alterations)
  - SWMG (Antenna design, wave guide design, packaging influence)
- Evaluation boards serve as reference to full hybrid build



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Hybrid System Packaging

Framework conditions

Hybrid System framework conditions

- Signal Frequency set to around 8 Ghz because of YIG propagation properties
- YIG on GGG as SWMG device
- APIC is 65 nm CMOS technology with 80 µm pad /160 µm pitch, design by Partner Akronic
- Organic Interposer Technology on Panel
  - ABF GXT62 Material -> good Dk Df for RF, fine line /HDI viable
  - SAP process chain for Interposer layer
  - 3 layer of ABF for routing/fan out
- SMD viable top layer for connectors / auxiliary circuitry

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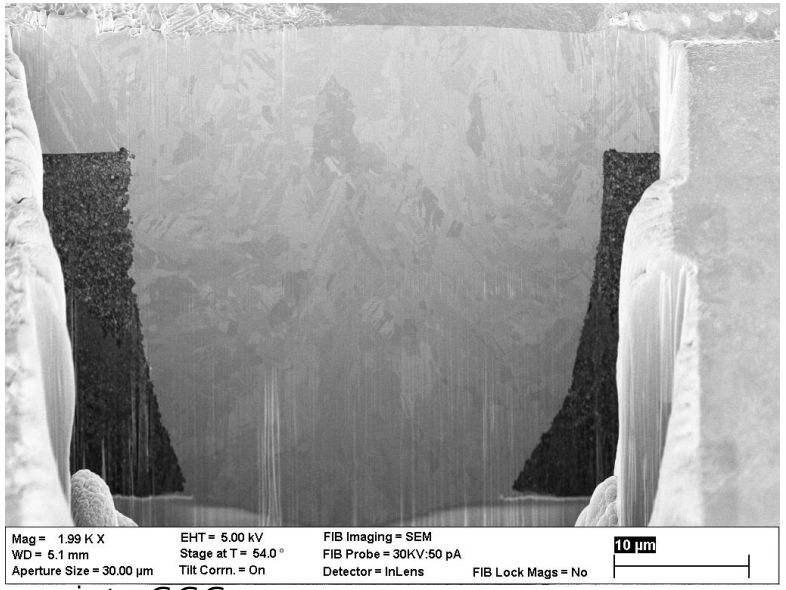
Hybrid System Packaging

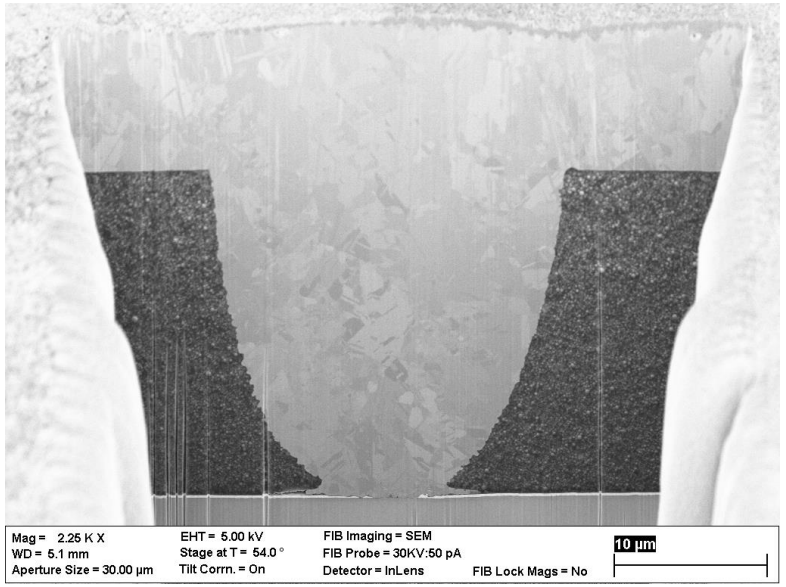
Results

Contacting SWMG

- Since GGG is an isolator and Gold pads are thin, idea to laser through pads and connect the pad ring
  - Safe process time/steps as well as costs for thick gold pads
  - GGG only carrier material, no functions/no circuitry
- Laser parameters were established with absorption/Transmission of GGG /ABF
- UV Laser process validated
  - Thikness of ABF need to be constant
- To keep yield high with variances → more power laser process



More power, deeper into GGG



Less power, narrow bottom via

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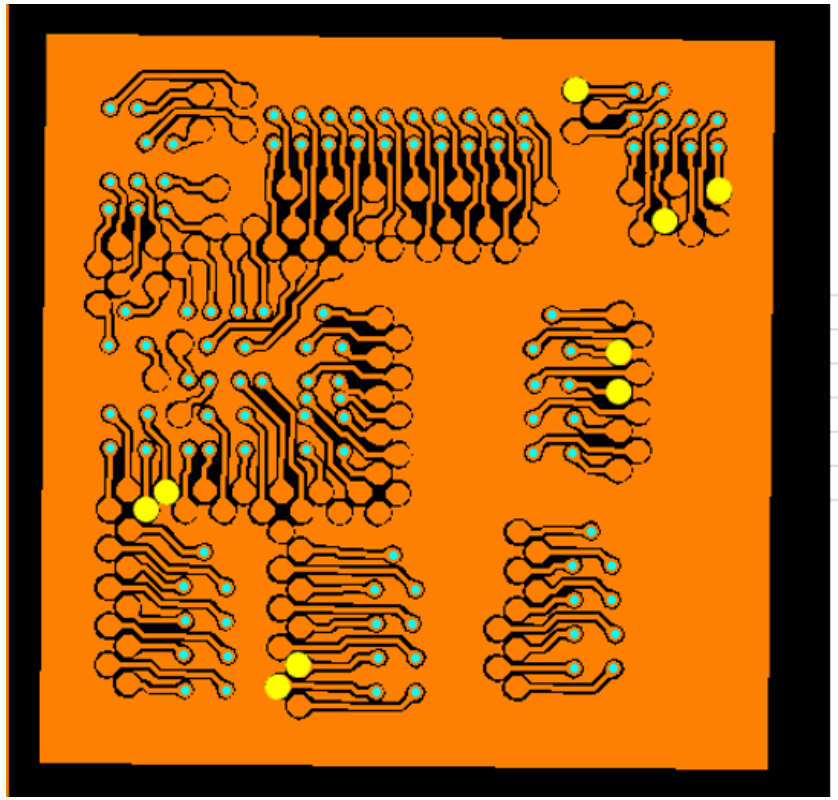
Hybrid System Packaging

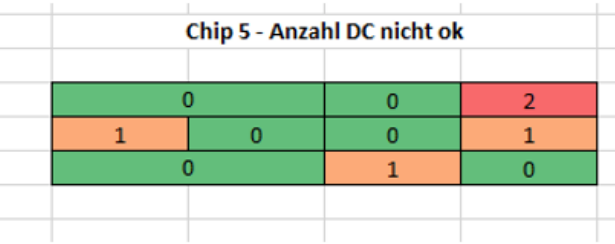
Results

Contacting SWMG

- Validation with Daisy chain layout and FIB cut
  - Around 90% yield
- Even with some alignment issues laser drill to LDI exposure still remaining
- Daisy chain layout: Cu pad → Cu Via → Gold pad SWMG and back up again



- Daisychain layout on 1st gen SWMG



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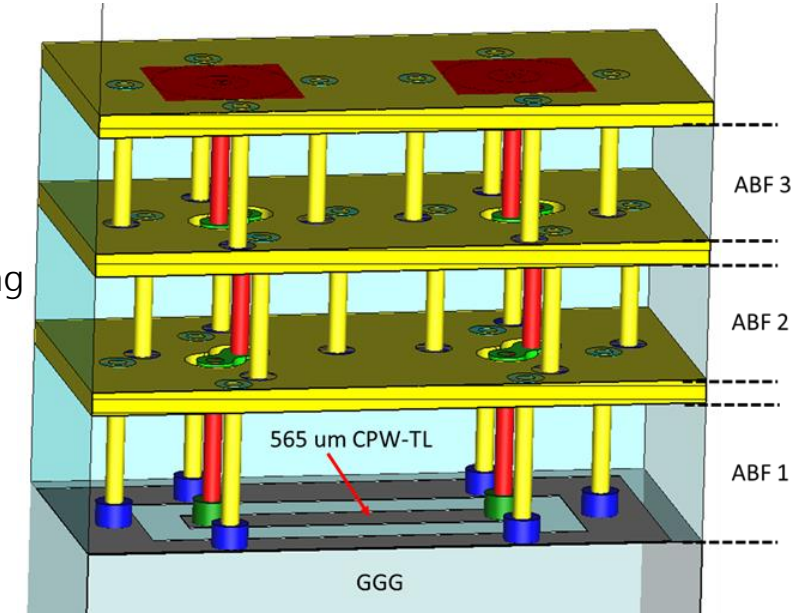
Packaging Results
Coplanar Waveguides

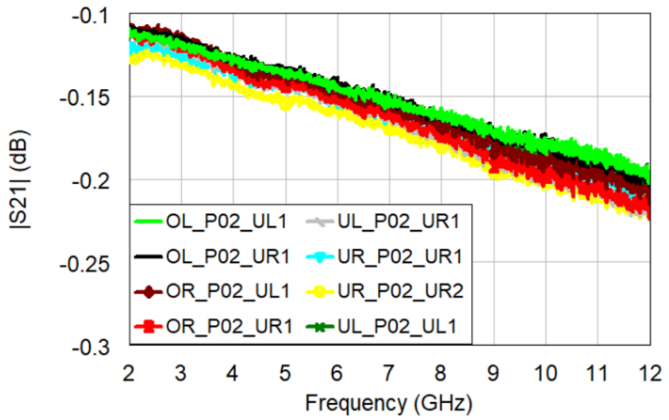
Evaluation Board: Coplanar Waveguide

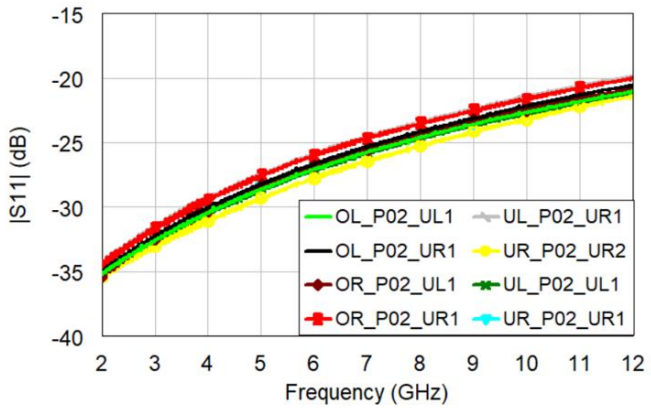
- Evaluation of transition losses through interposer, understand impact of Interposer and RF pathing on signals
- Start with simulations and comparison to measurments
- Confirmed in measurements
- Simulation and experiment are close together
  - Measured 0.17dB loss (S21)
  - Simulated 0.18dB loss (S21)
- Low loss transmission from interposer structure: good

- red= HF line
- yellow = grounding



- 3d Model of Design





- Each line = one path

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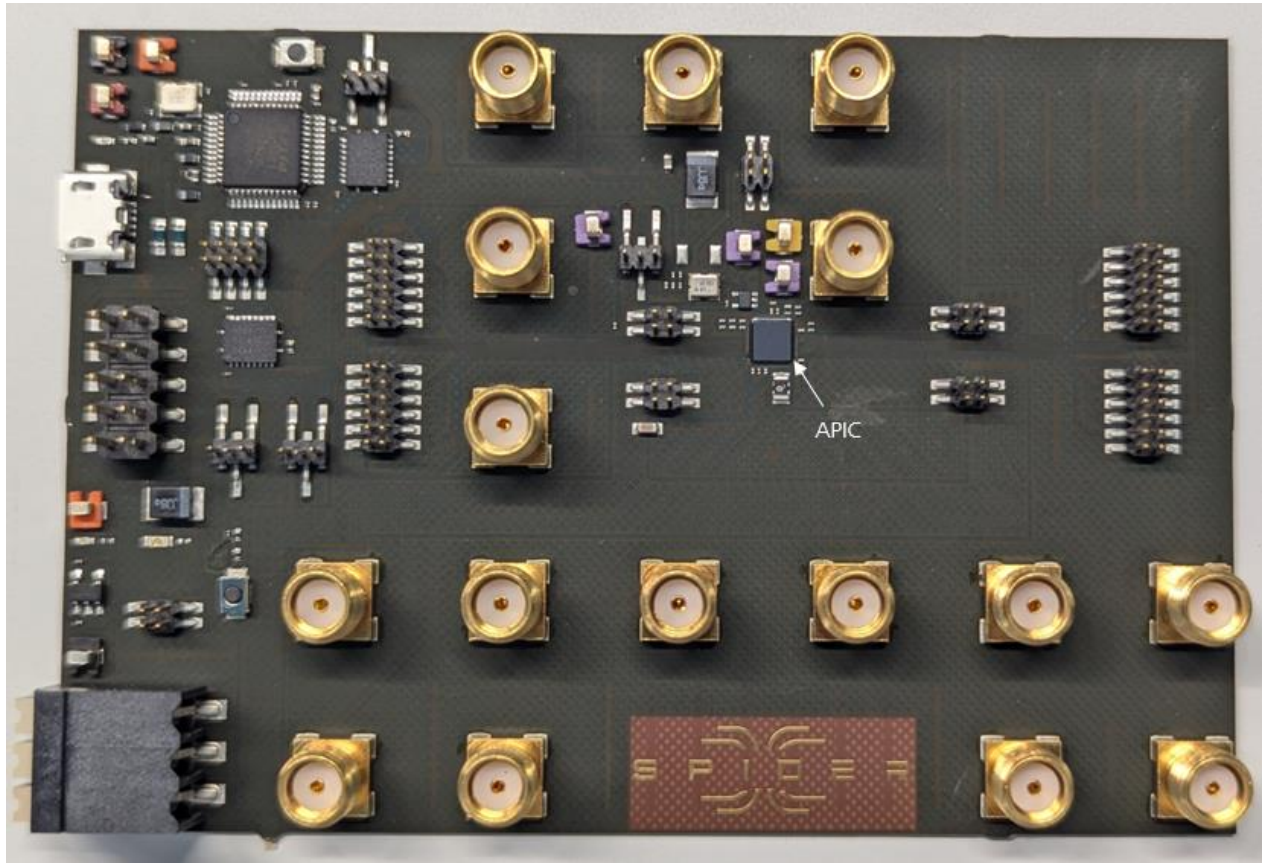
Packaging Results

APIC Evaluation Board

Evaluation Board: APIC Evaluation Board

- Test of the APIC functions and also RF path lines to analysis devices (SMA connectors)
  - Digital to analog converter
  - Analog to digital
  - PLL
  - Phase shifter
  - Internal Clock
- Issue with grounding beneath SMA connector → Design changes needed for 2nd iteration
- Weak adhesion between ABF and Cu: difficult handling with SMA connectors (delamination) found
- But overall, all APIC functions working as intended



designed by Akronic

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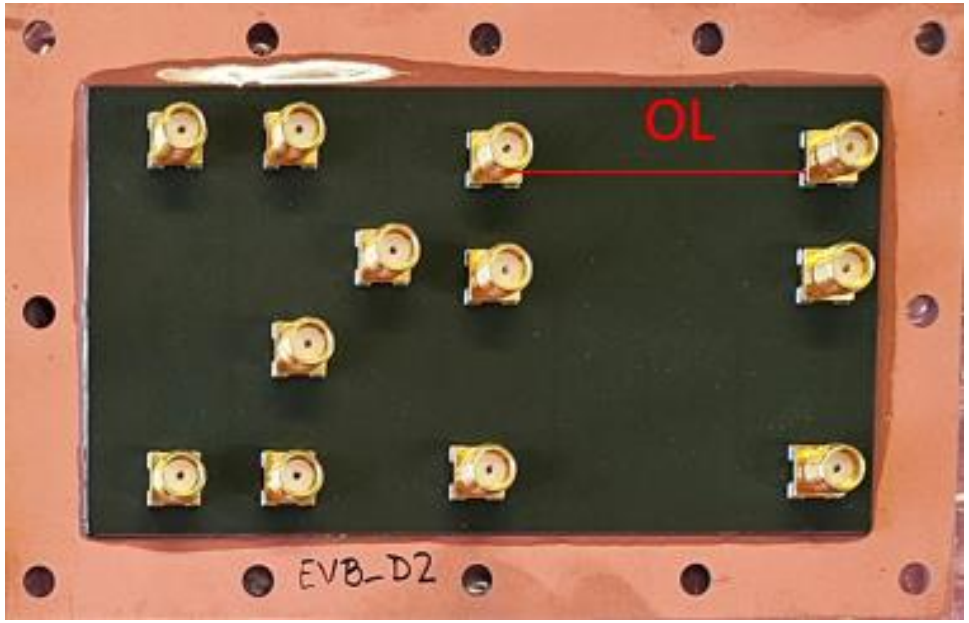
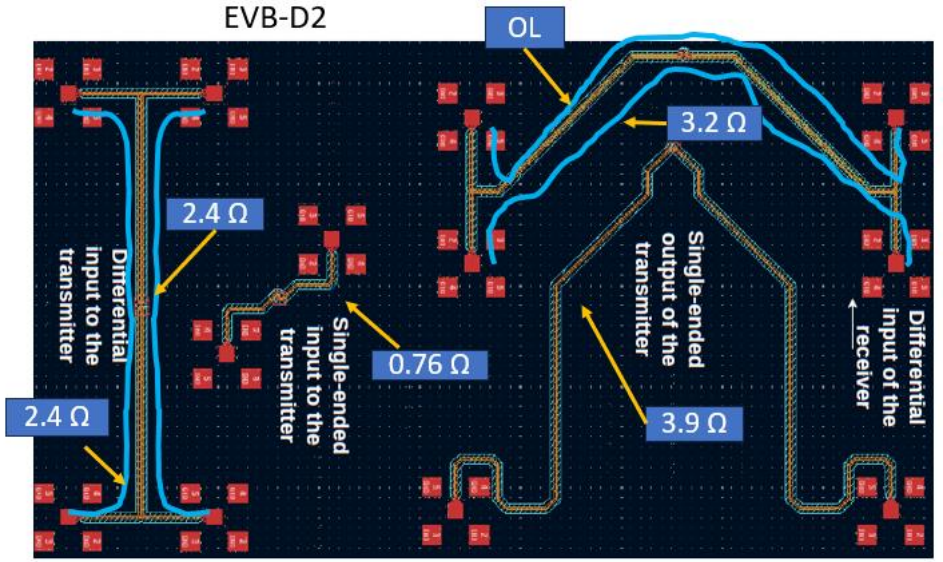
Packaging Results

De-Embedded Evaluation Board

Evaluation Board: De-Embedded Evaluation Boards

- Reference to measure RF trace resistance against APIC Evaluation Board
- Alignment issues between different SAP tools cause bad connection in most RF traces
  - Each individual tool calibrated regularly
  - Problem of different master panel provided by each manufacturer
  - Solution: master panel to calibrate each tool in the SAP process line
- Alignment issues in other Evaluation Boards less obvious because mostly redundant vias instead of only 1 per trace De-Embedded Evaluation Boards





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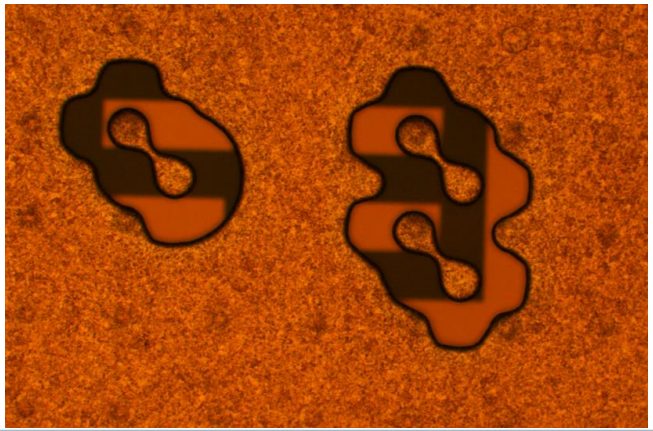
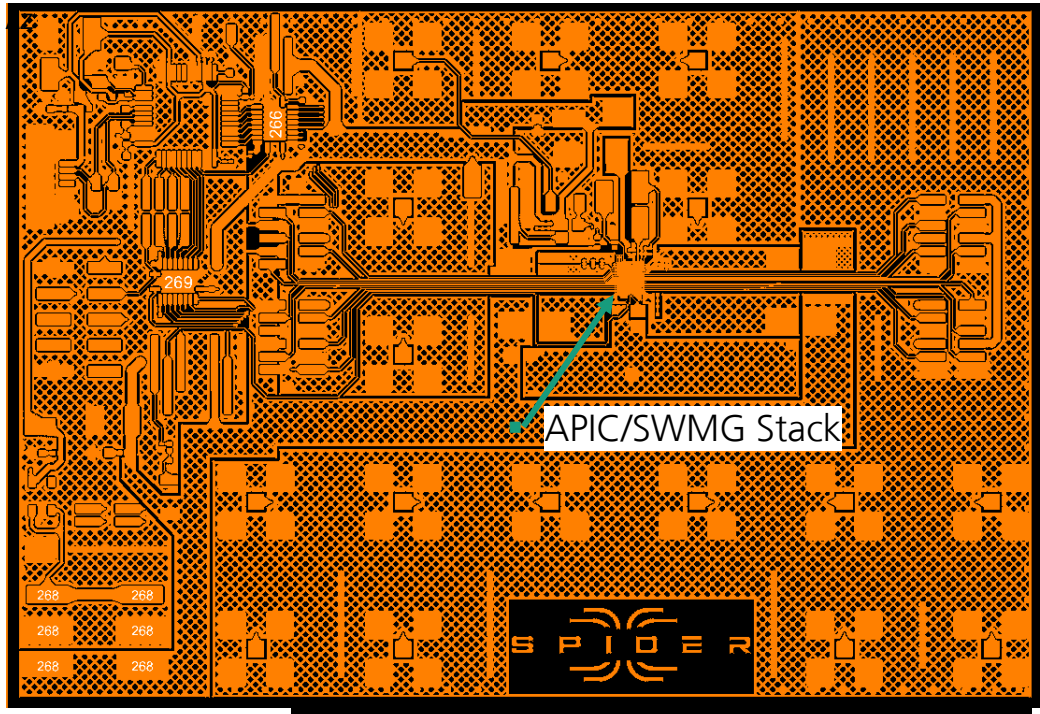
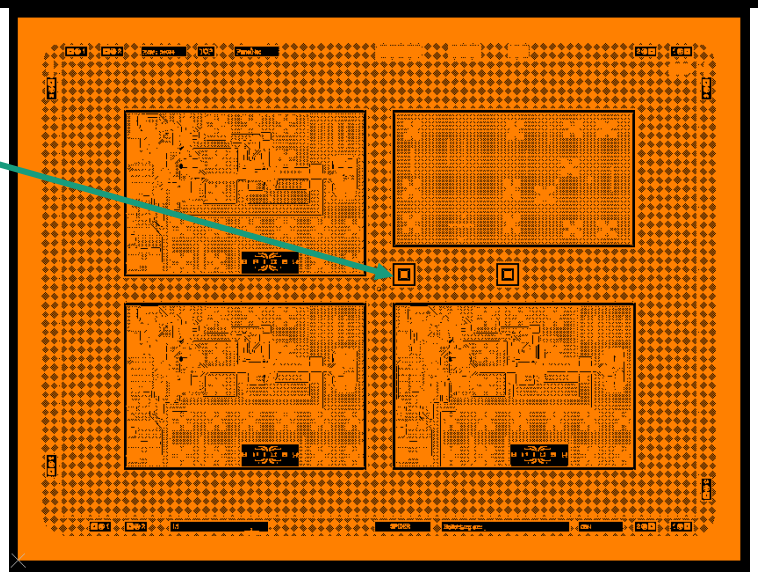
Packaging Results
Hybrid System

Hybrid System: Production started

- Most of the Board is for evaluation /analysis of hybrid system
- If working, small modules could be used to cascade (some initial test modules on panel) + magnetic probe
- + additional de-embedded Board to validate RF trace resistance







- Finished L3 with SWMG structure beneath
- Visible small plating dimple from via filling
- RF traces with dogbone structure
- 60 pad, 35 via

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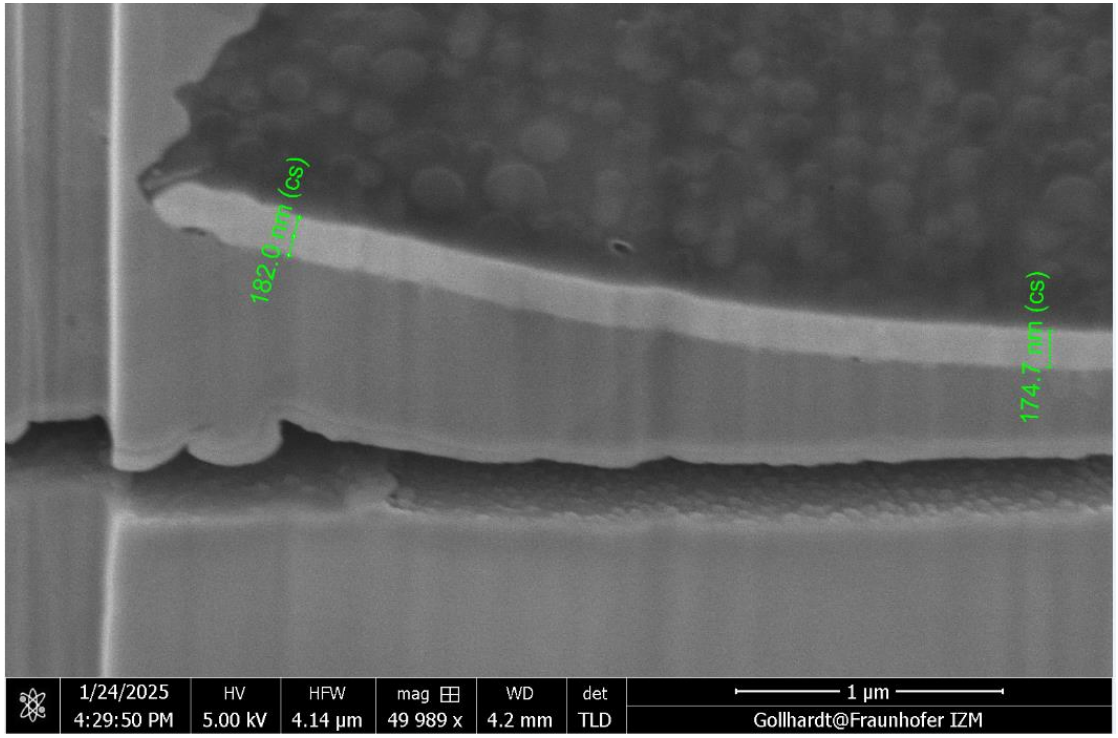
Packaging Results
Discussion

Discussion

- Handling and processing with SWMG (YIG+GGG) similar to normal chips, no special requirements noticed
- Withstand lamination process (pressure/heat) and laser drills in GGG
- Adhesion of Au pads on GGG seems weak.
- Delamination of gold pads on GGG occurred by handling thermo release tape
- Delamination of ABF/Copper Via could be seen in FIB cuts sometimes
- Impact of the delamination on yield or function of systems not investigated yet



- Double delamination: gold from GGG -> underfilled Copper, Copper from GGG

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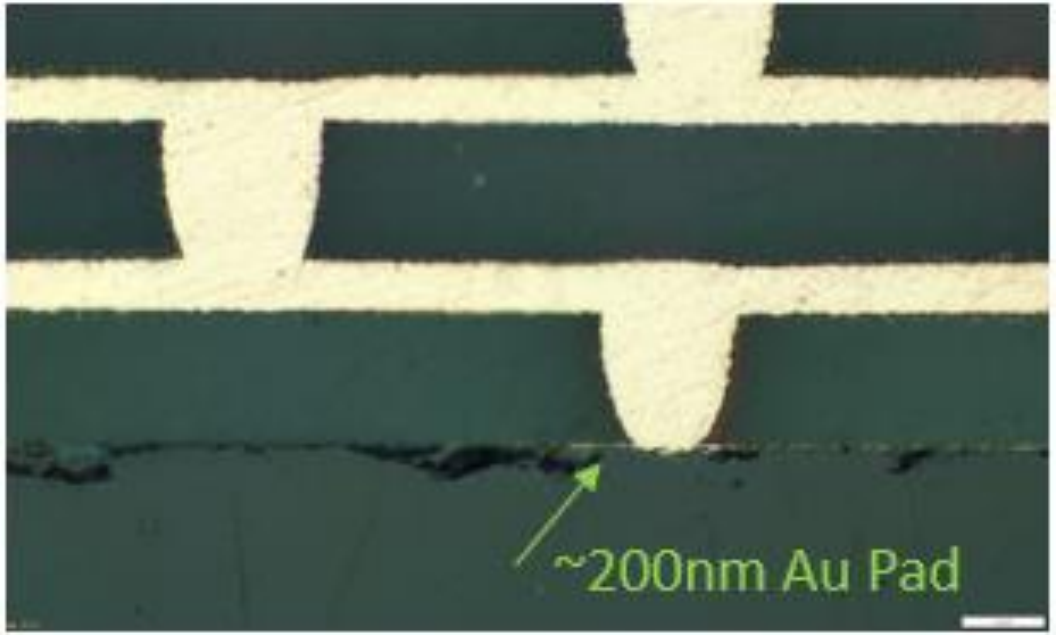
Packaging Results
Discussion

Discussion

- Each Evaluation Board provides valuable information
- Interposer:
  - Confirmed: interposer influence on RF: low
  - Need to be confirmed: influence on YIG
- APIC Evaluation Board: organic interposer technology based on SAP with HDI structures is viable, flexible platform to evaluate the Hybrid system
- Packaging concept is working for this hybrid system approach
- Complete packaging concept for Hybrid System established and shown partly in each evaluation board
- Missing: combined hybrid system evaluation board



- Cross section Interposer structure over GGG/SWMG

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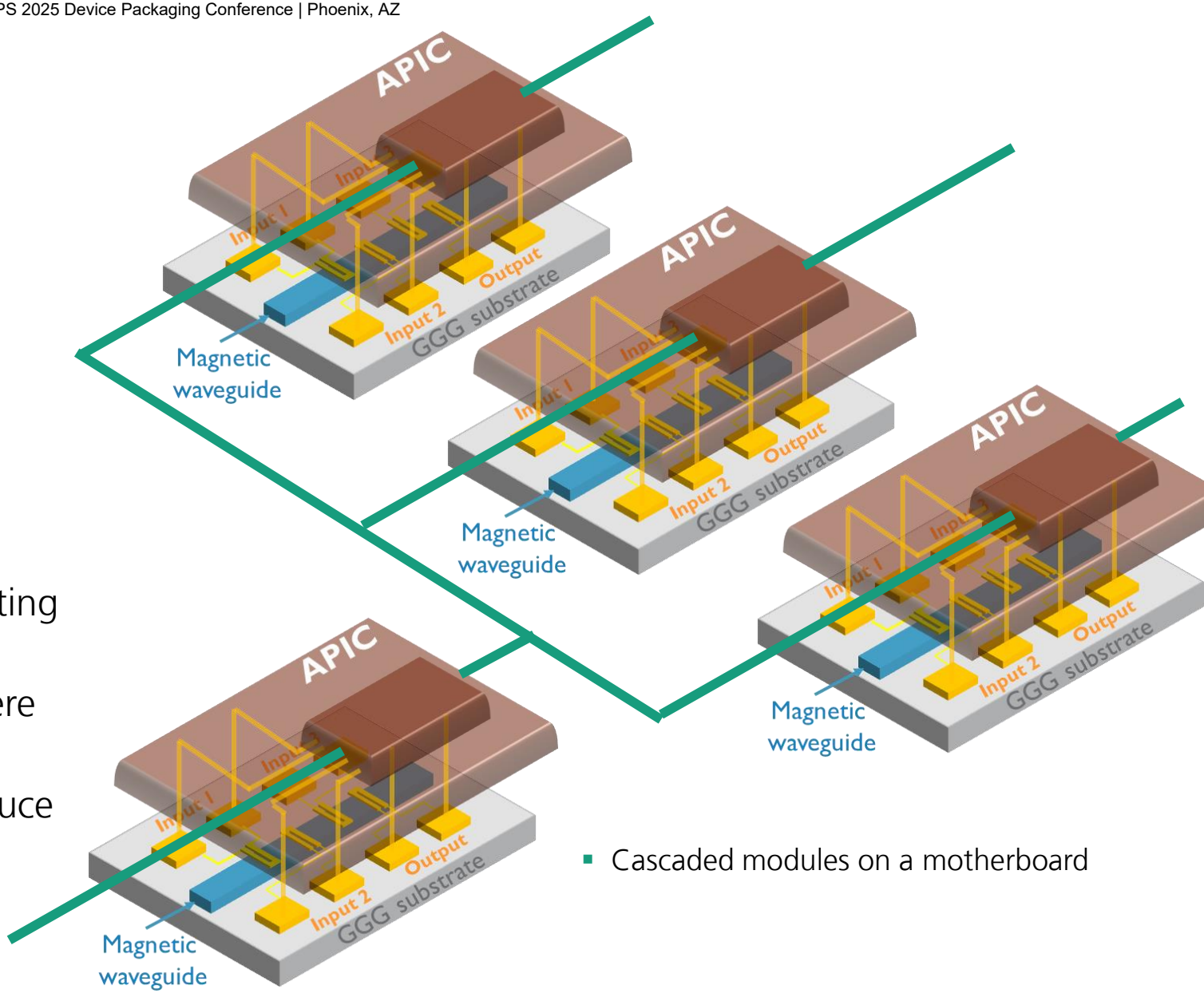
Outlook

Outlook

- Finish Hybrid System Evaluation board + characterization
- Design and Production of modules (SWMG+APIC) and their cascading on a motherboard as proof of concept for computing hybrid system
- Roadmap to cascading in the spin wave sphere and requirements for future packaging (e.g. addressing adhesion problems) goal is to reduce size and energy cost
  - Cascading system: 8 bit adder in this project
  - Show case: flexibility of organic interposer



- Cascaded modules on a motherboard

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