Yield and Cost Analysis of a Face-to-Back Chip-on-Wafer 3D Package

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Agenda

- Introduction
- Activity Based Cost Modeling
- Face-to-Back 3D Stack
  - Process Flow
  - Cost Breakdown
  - Yield Analysis
- Summary

Introduction

Introduction

- One form of advanced packaging is 3D stacking; 2 (or more) chips are stacked directly
  - Different from using an interposer, in which chips are placed side-by-side and routing on the interposer connects them
  - In a 3D stack, routing is on/through the chips
- 3D packaging is attractive for many reasons:
  - Improved performance due to shorter interconnect
  - Enhanced power efficiency
  - Reduced area footprint
- On the other hand, it means sticking vias in expensive chips, risking defects
  - Also design constraints (e.g. thermal)
- Goal of this analysis: understand 3D stack cost drivers
  - Once the cost components are understood, chip designers, technology suppliers, and more can make cost-effective advanced packaging decisions

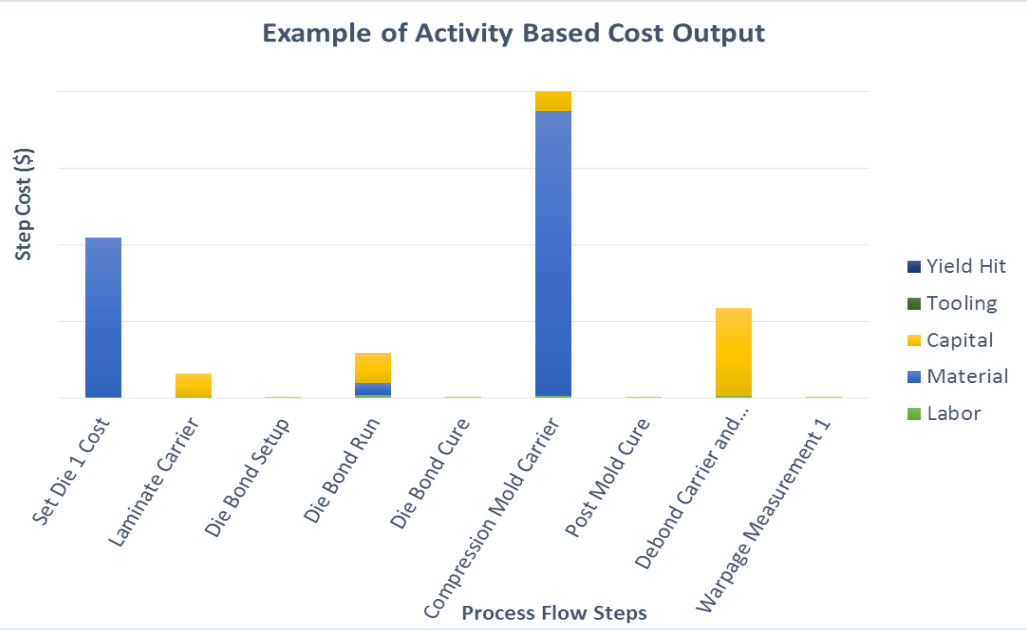
Activity Based Cost Modeling

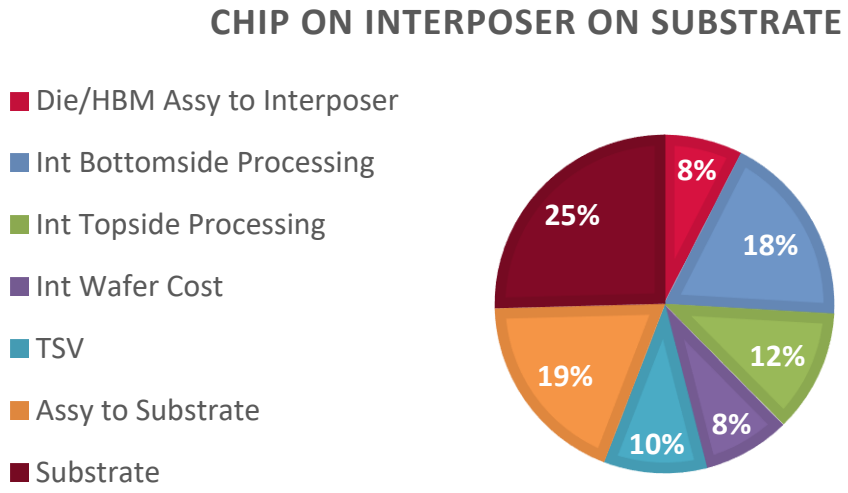
Activity Based Cost Modeling

- Bottom-up approach to cost that accounts for every cost component for every activity
  - Time required to complete the activity
  - Amount of labor dedicated to the activity
  - Cost of material required to perform that activity – both consumable and permanent material
  - Tooling cost
  - Depreciation cost of the equipment required to perform the activity
  - Yield loss
- Factory considerations also included
  - Equipment utilization
  - Load balancing
  - Labor rate
- Detailed output enables results to be seen in detail or rolled up in categories
  - Example output charts on next page

Output Examples

Step Name	Labor Cost/Wafer	Capital Cost/Wafer	Tooling Cost/Wafer	Material Cost/Wafer	Yield Cost
RDL Spin coat	$ 0.08	$ 4.63	$ -	$ 4.38	$ 0.062
RDL Mask Cost	$ -	$ -	$ -	$ 0.21	$ 0.001
RDL Expose	$ 0.02	$ 2.07	$ -	$ -	$ 0.014
RDL Develop	$ 0.03	$ 1.54	$ -	$ 0.55	$ 0.014
RDL Cure	$ 0.08	$ 0.19	$ -	$ -	$ 0.002





Face-to-Back 3D Stack

F2B 3D Stack

- Chips can be stacked in different ways
- For this analysis, analyze a face-to-back (F2B) process
  - Name of process describes the surfaces that touch: the face (top) of the incoming (top) die is in contact with the back of the bottom wafer
  - Though-silicon vias (TSVs) are in the bottom wafer, which also has backside metallization
- Other variations
  - Does not have to be chip-on-wafer
    - If top and bottom die will be the same size after dicing, then this process can be done as a wafer-on-wafer process
  - Multiple bonding methods are available
    - This analysis focuses on hybrid bonding

Process Flow

Top Wafer (Top Die)

- Start with incoming wafer
- Grind to desired thickness

Remaining steps are carried out on face

- Create passivation layer
- Carry out hybrid bonding metallization
- Mount on dicing tape and dice
- Final hybrid bonding preparation

Bottom Wafer

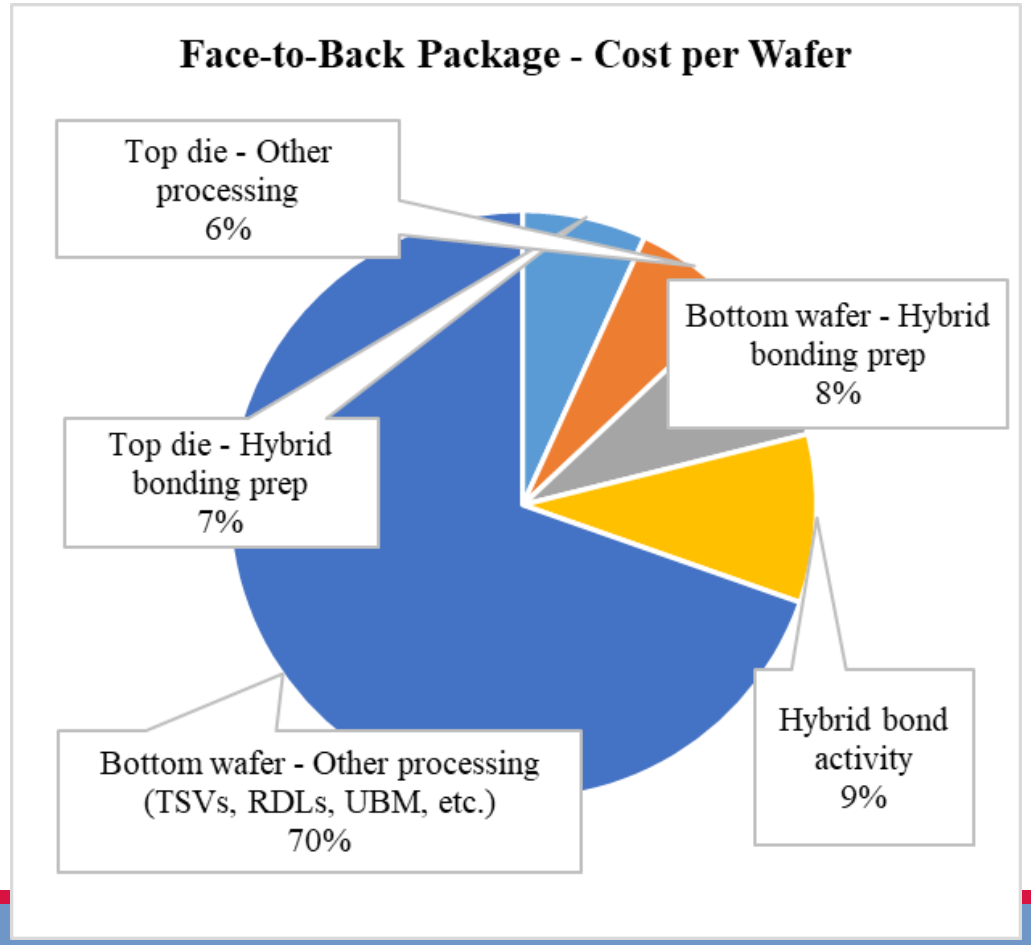
- Start with incoming wafer
- Create TSVs
- Bond to carrier wafer to work on backside
- TSV reveal and thinning
- Optional RDL(s)
- Carry out hybrid bonding metallization
- Final hybrid bonding preparation
- Carry out hybrid bond of incoming die

Final Activities

- Debond from carrier wafer
- Bond to new carrier to work on face of main wafer
- Optional RDL(s)
- C4 bumping
- Dice die-to-wafer stack into final package size

Cost Breakdown: Total Package

- Design details: Two 4x4mm die (mature node) placed on a bottom wafer (advanced node), final package size after bonding is 12x12mm



*Silicon cost and yield loss excluded

Cost Breakdown: Total Package

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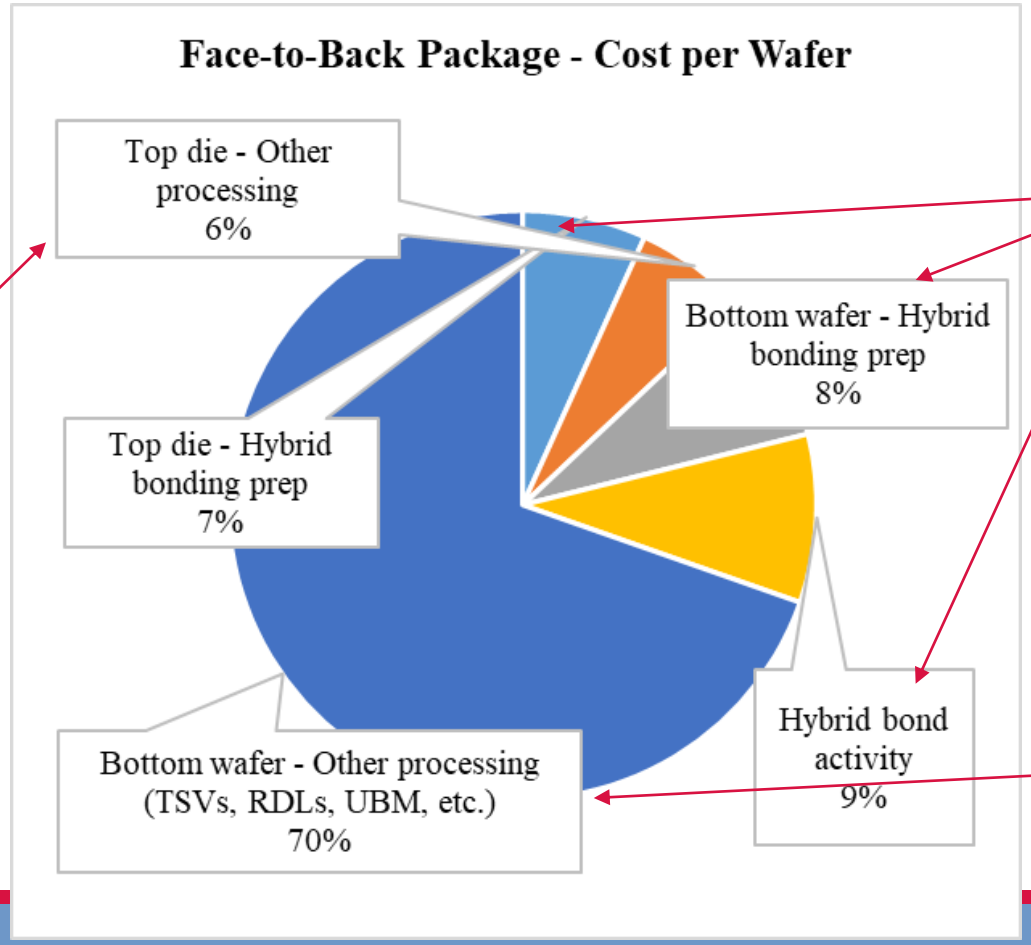
Top die does not represent a major portion of cost. This makes sense, as limited processing occurs.



Hybrid bonding prep is not negligible, but not a major cost driver. Same goes for hybrid bonding itself.

Bottom wafer processing is the dominant cost category due to routing creation (RDLs and TSVs).

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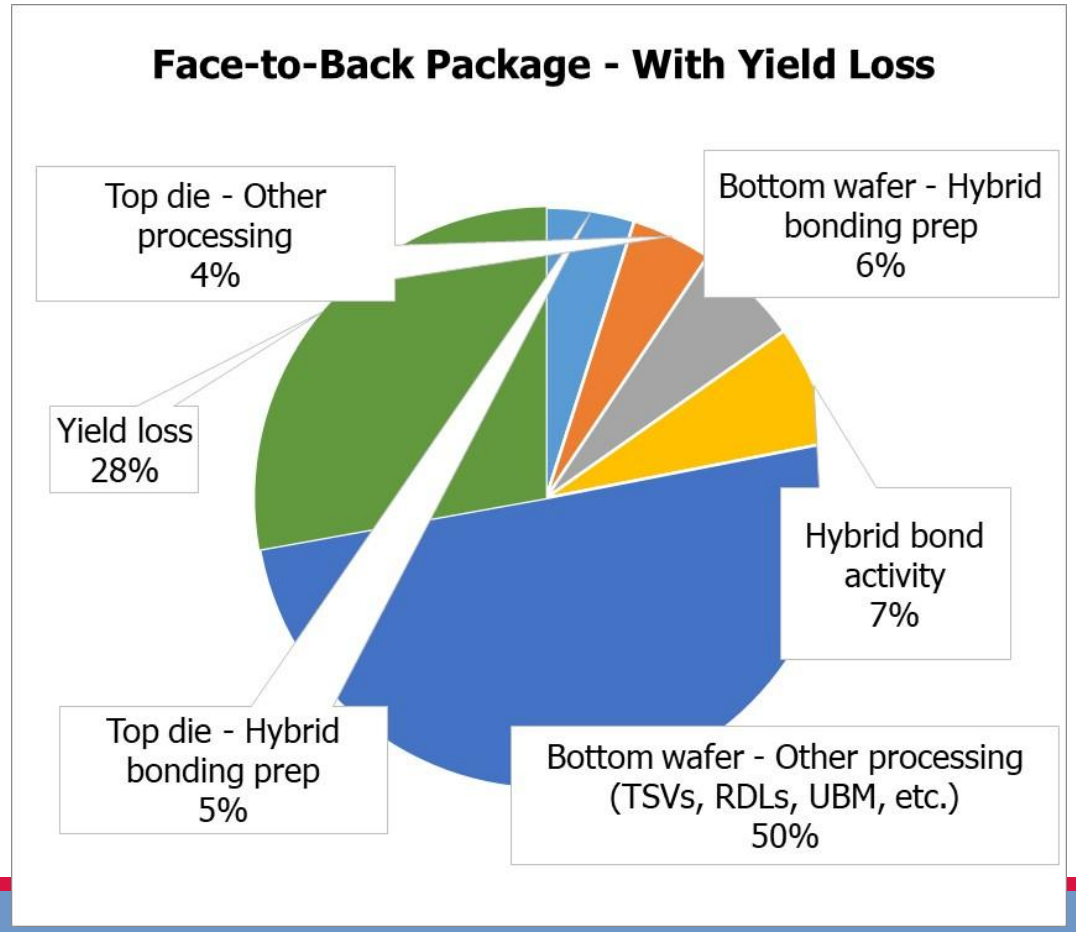

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Cost Breakdown: Total Package

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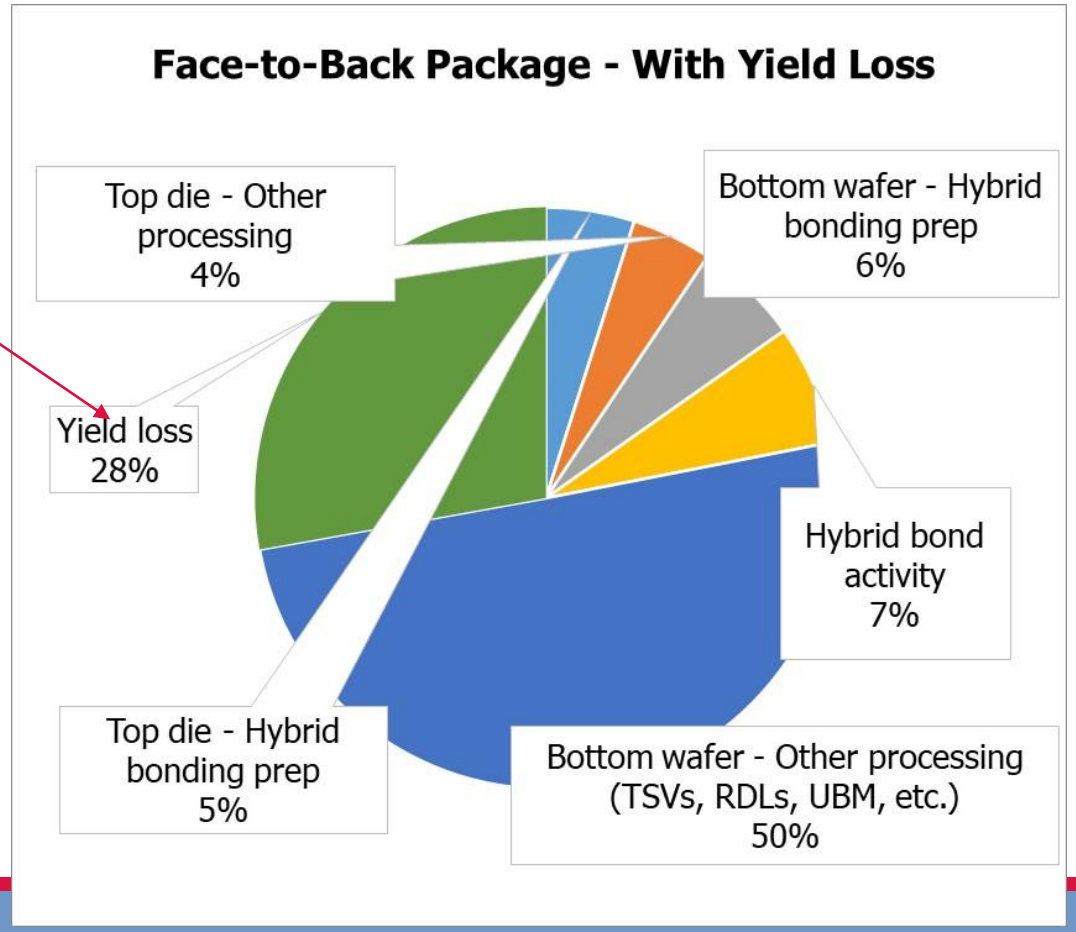
Once yield loss is included, the chart looks different.

The per-wafer cost of silicon is over $10K in this design, so even a small yield hit drives a noticeable cost.



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Cost Breakdown: Top Wafer/Die

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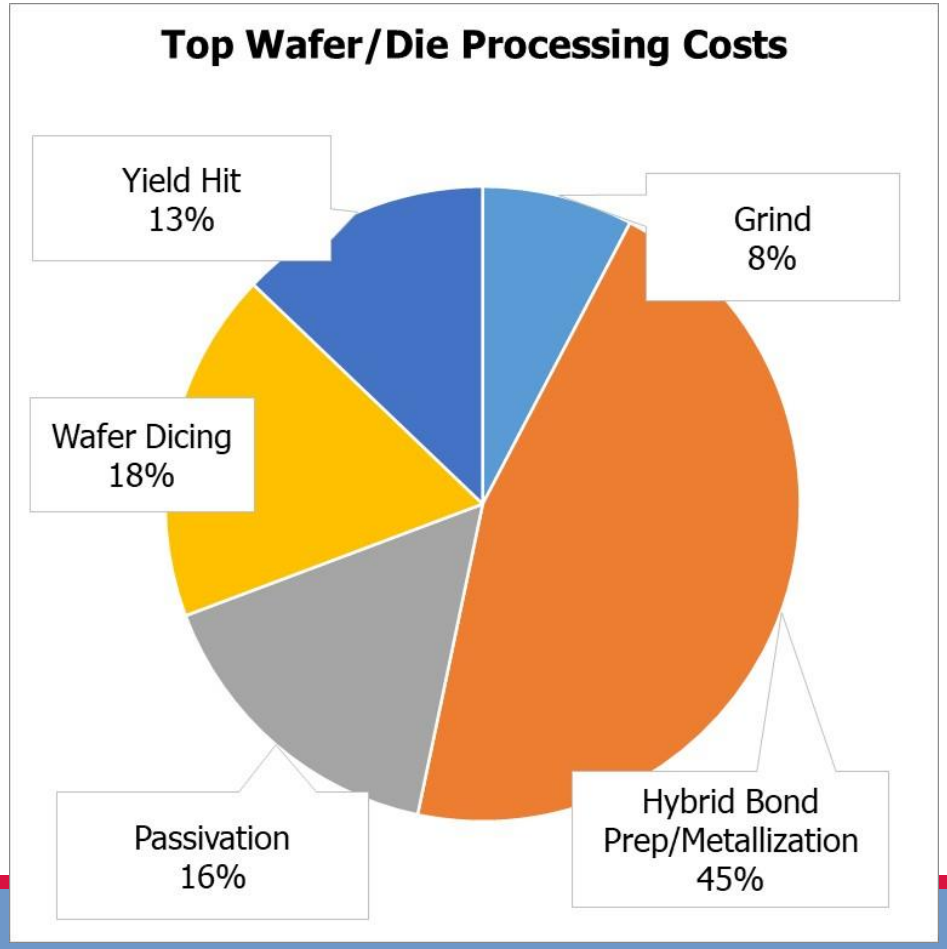

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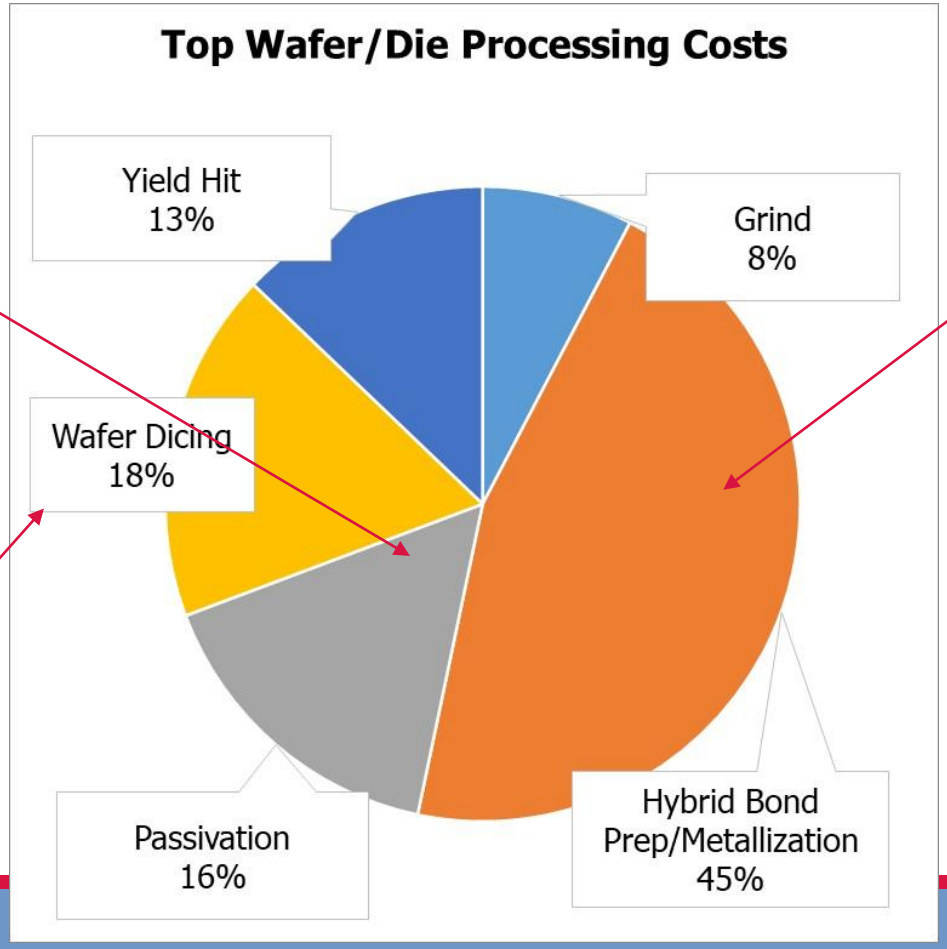
Cost Breakdown: Top Wafer/Die

- Design details: Two 4x4mm die (mature node) placed on a bottom wafer (advanced node), final package size after bonding is 12x12mm

Passivation prior to hybrid bonding metallization is the third-highest cost contributor.
Process involves lithography, which carries capital and material costs.

Dicing is the second highest cost driver. Not a complicated or new process, but the smaller the die—in this case, 4x4mm—the longer the process takes.

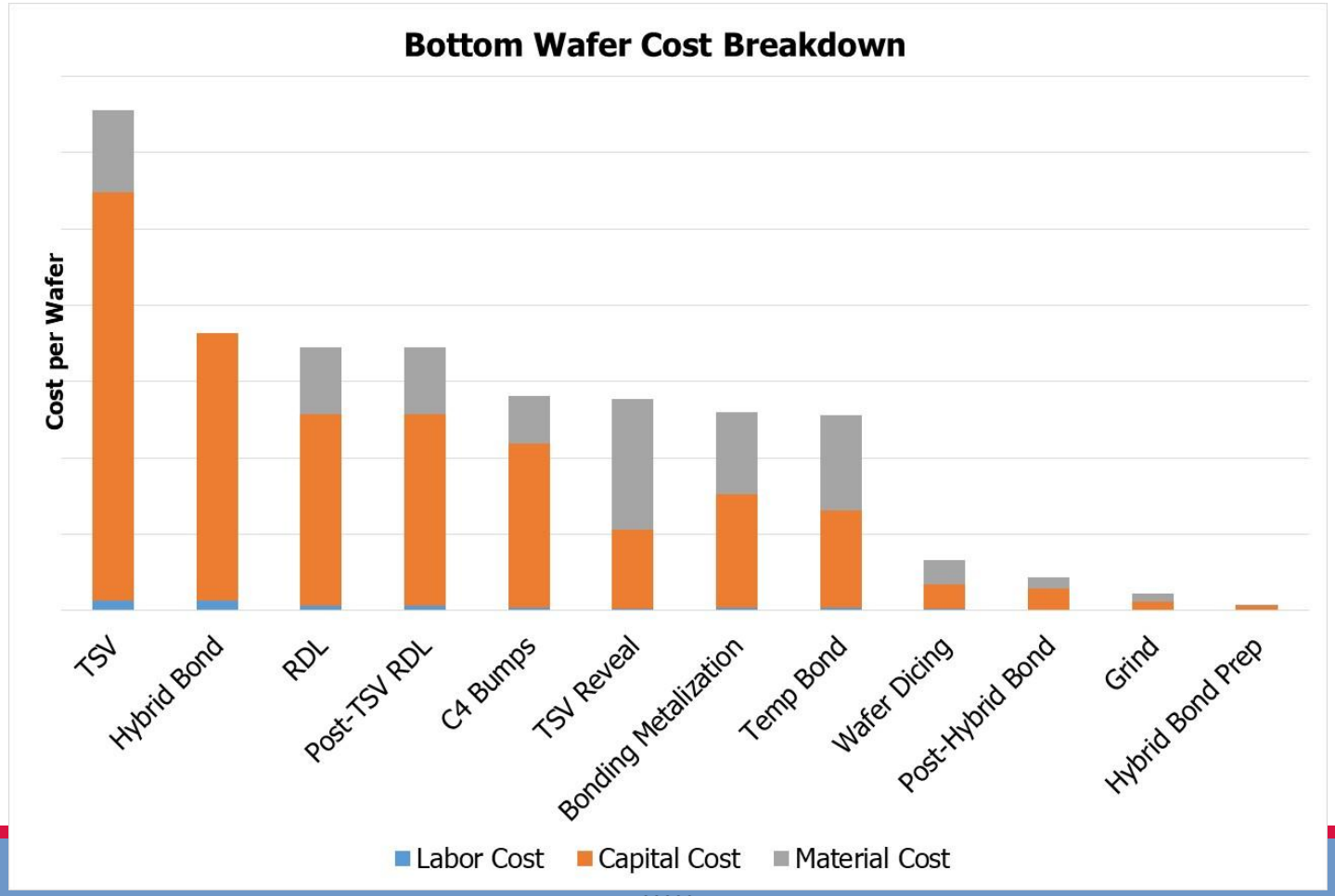


Major cost driver for top wafer/top die is hybrid bonding metallization.

*Silicon cost excluded

Cost Breakdown: Bottom Wafer

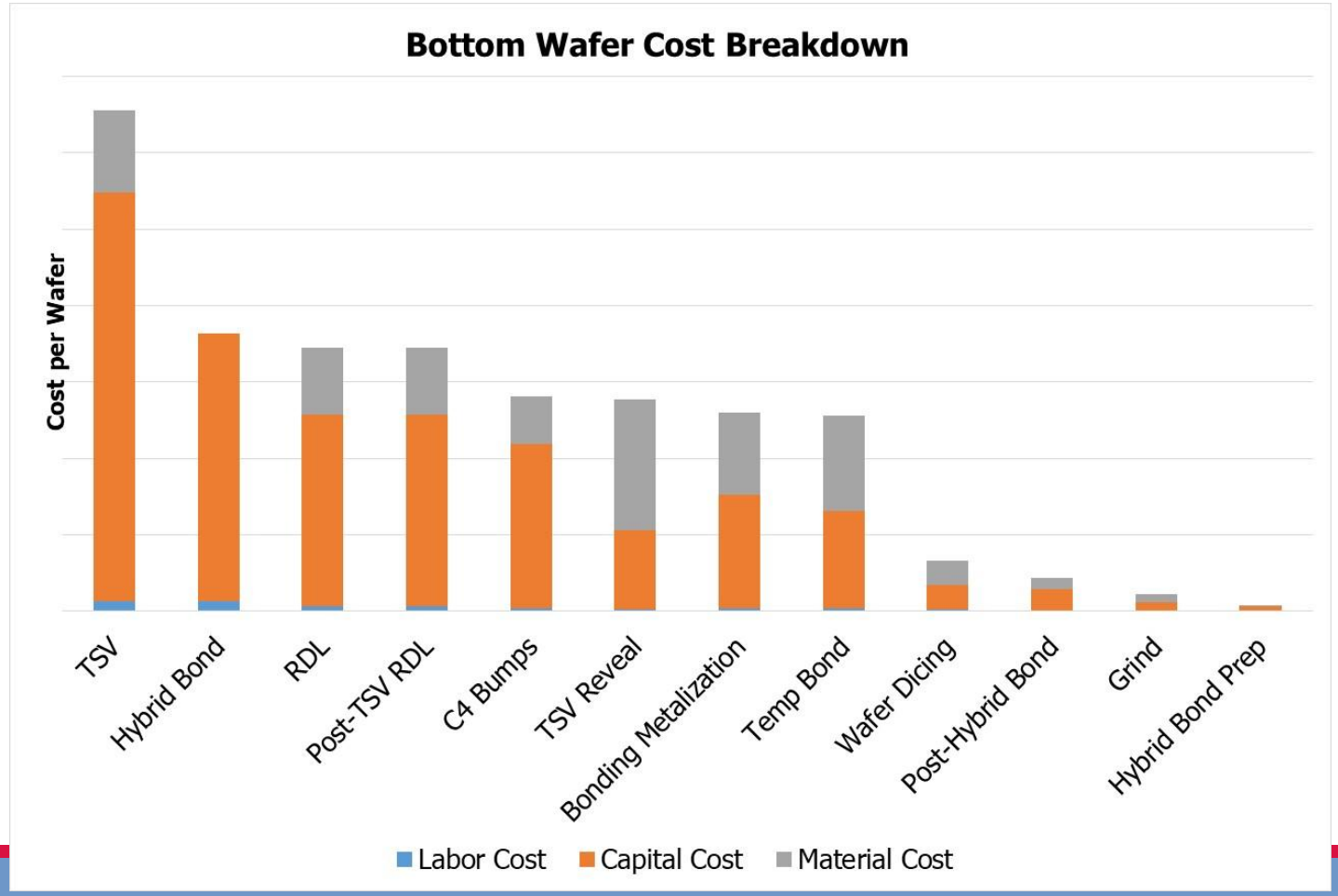
- Design details: Two 4x4mm die (mature node) placed on a bottom wafer (advanced node), final package size after bonding is 12x12mm



Cost Breakdown: Bottom Wafer

- Design details: Two 4x4mm die (mature node) placed on a bottom wafer (advanced node), final package size after bonding is 12x12mm

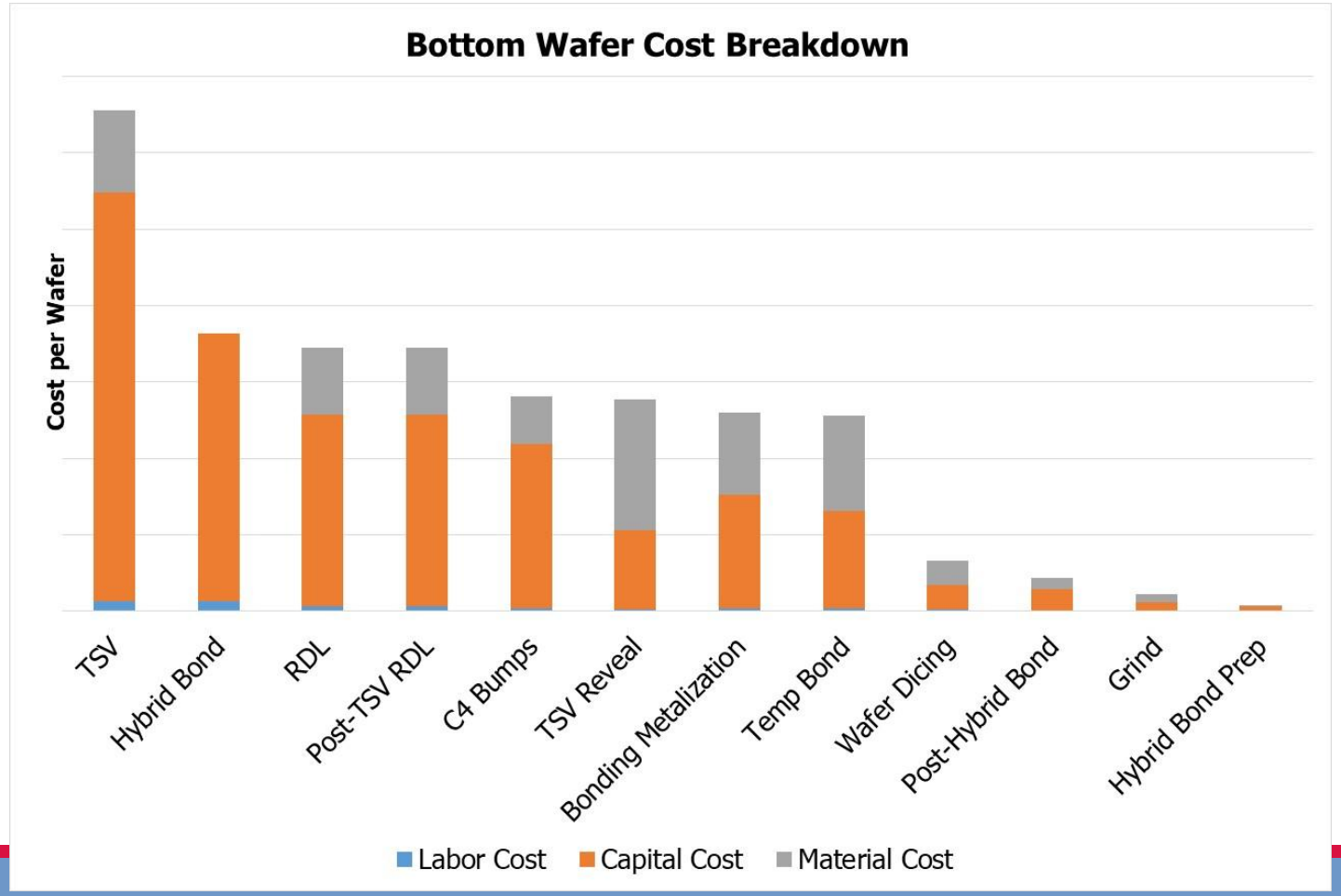
Activity	Comments
TSV	· Major cost driver in bottom wafer processing · Cost primarily capital because of expensive deep reactive ion etch equipment and lithography required to define the vias
Hybrid bond	· Refers to actual die-to-wafer hybrid bonding process · Second highest cost driver because of the time it takes to align and place the die · Actual bonding activity is a few seconds per die, but because there are 2 die per package, and there are many 12x12mm packages from a wafer, cost is notable on a per-wafer basis
RDL	· Two RDL processes occur during bottom wafer processing · Some designs may not require both (or any), but for this design, there is: 1 RDL after TSV creation, 1 RDL before C4 bumping · 1 RDL represents ~1/10th of bottom wafer processing costs, so it's easy to understand the impact if one/both are removed · RDL creation process driven primarily by the capital and material costs associated with lithography and plating



Cost Breakdown: Bottom Wafer

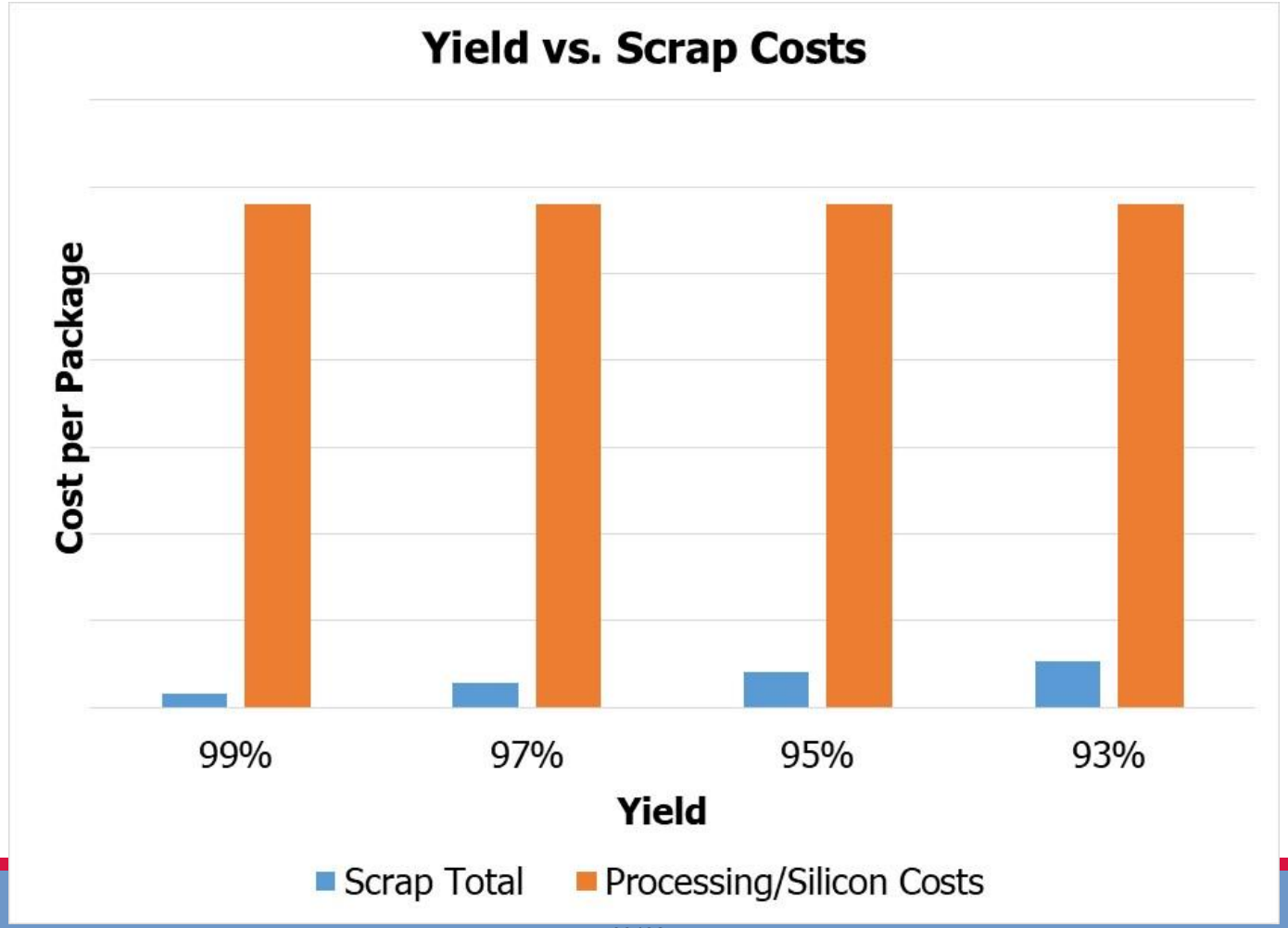
- Design details: Two 4x4mm die (mature node) placed on a bottom wafer (advanced node), final package size after bonding is 12x12mm

Activity	Comments
C4 Bumps	· Creation of C4 bumps similar to RDL creation · Lower cost than RDL, but the cap. and mat. costs still come from litho and plating
TSV Reveal	· TSV reveal includes the cost to temp. bond wafer to carrier · TSV reveal itself—grinding the wafer—more capital than material · But including temporary bonding adds other considerations (see next category)
Temp Bond	· Final activity driving not-insignificant cost · First bond to temporary carrier included in TSV reveal activity · Debonding from that carrier, then bonding to another carrier for C4 bumping, captured here · Temporary bond/debond is a material-heavy process · In addition to the material cost of a quality reusable carrier (which tend to be reused a handful of times, not hundreds of times), there is the material cost of a release layer · Cost model incl. material to clean wafer post-bond + clean carrier



Yield

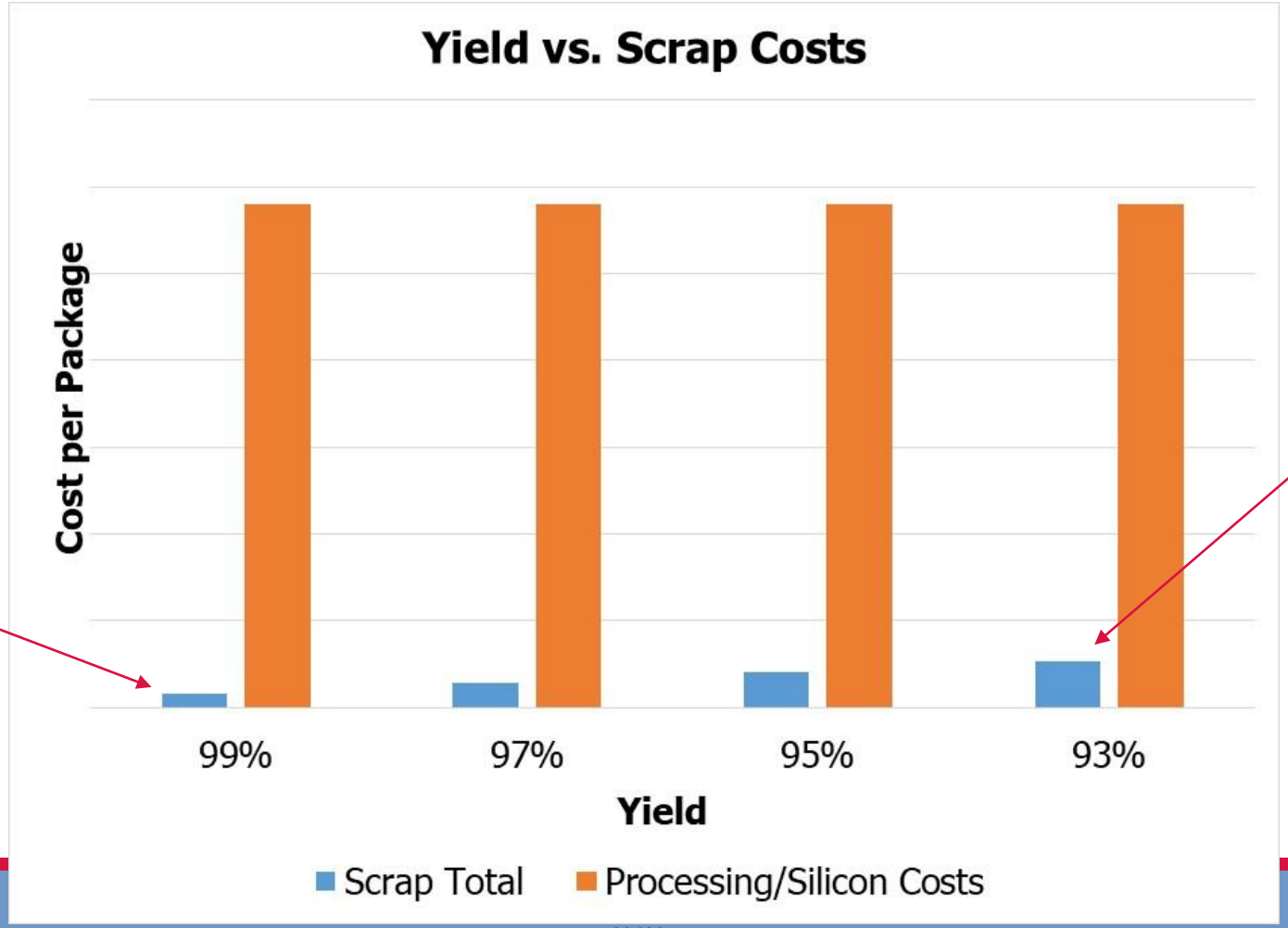
Key Takeaway: When an expensive process is carried out with expensive wafers (top or bottom), small yield changes matter.



Yield

Key Takeaway: When an expensive process is carried out with expensive wafers (top or bottom), small yield changes matter.

When the yield is high, total scrap cost is small compared to the cost of the silicon and packaging process.



As yield drops in 2% intervals, scrap cost rises. In this case, scrap cost is nearly 10% of the total package cost.

Summary

- Face-to-back 3D stacking with hybrid bonding is a complicated advanced packaging process
- Main cost drivers associated with this process and the chosen design are:
  - TSV creation
  - Hybrid bonding metallization (on top and bottom wafers)
  - Hybrid bonding activity
- Hybrid bonding is not always a cost driver on a per-package basis
  - But when small die are being bonded and the cost-per-wafer is evaluated, cost can appear high
- Yield is a major cost driver
  - Small yield change has a major impact on the per-package cost, unless the only die being handled are from mature (i.e. inexpensive) nodes