Fraunhofer IZM

Fraunhofer Institute for Reliability and Microintegration IZM

Development of a High-Density Adaptive Redistribution Technology for Embedded High I/O Components

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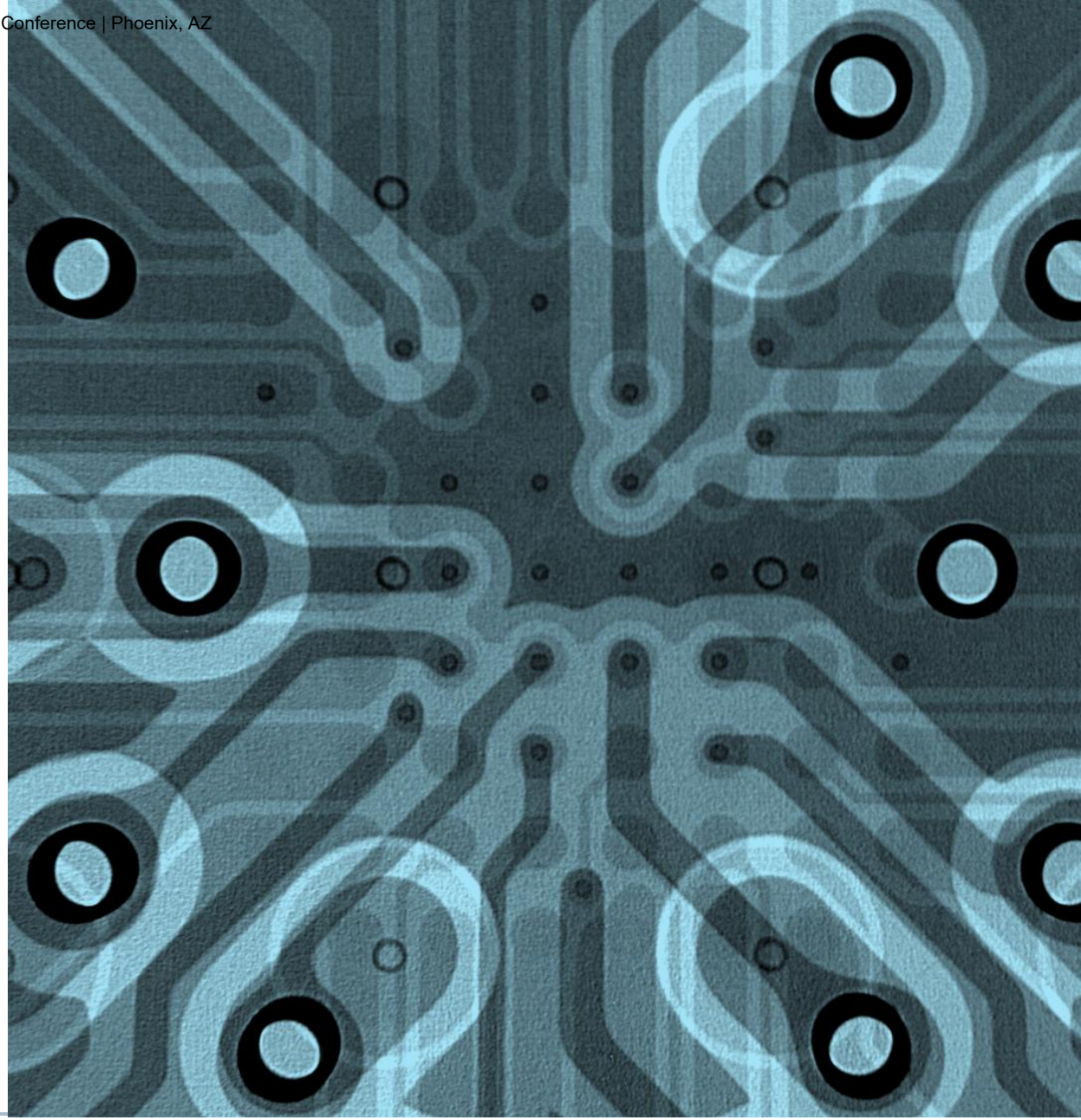
Outline

1. Introduction to High Density Substrates Technologies

2. Advanced Semi Additive (aSAP) - RDL Process
   - Overview
   - Vertical Interconnects - Via
   - Horizontal: Lithography, Plating, Strip & Etch

3. EU Project “CHARM”
   - Project introduction
   - Adaptive Processing
   - RDL formation

4. Conclusion

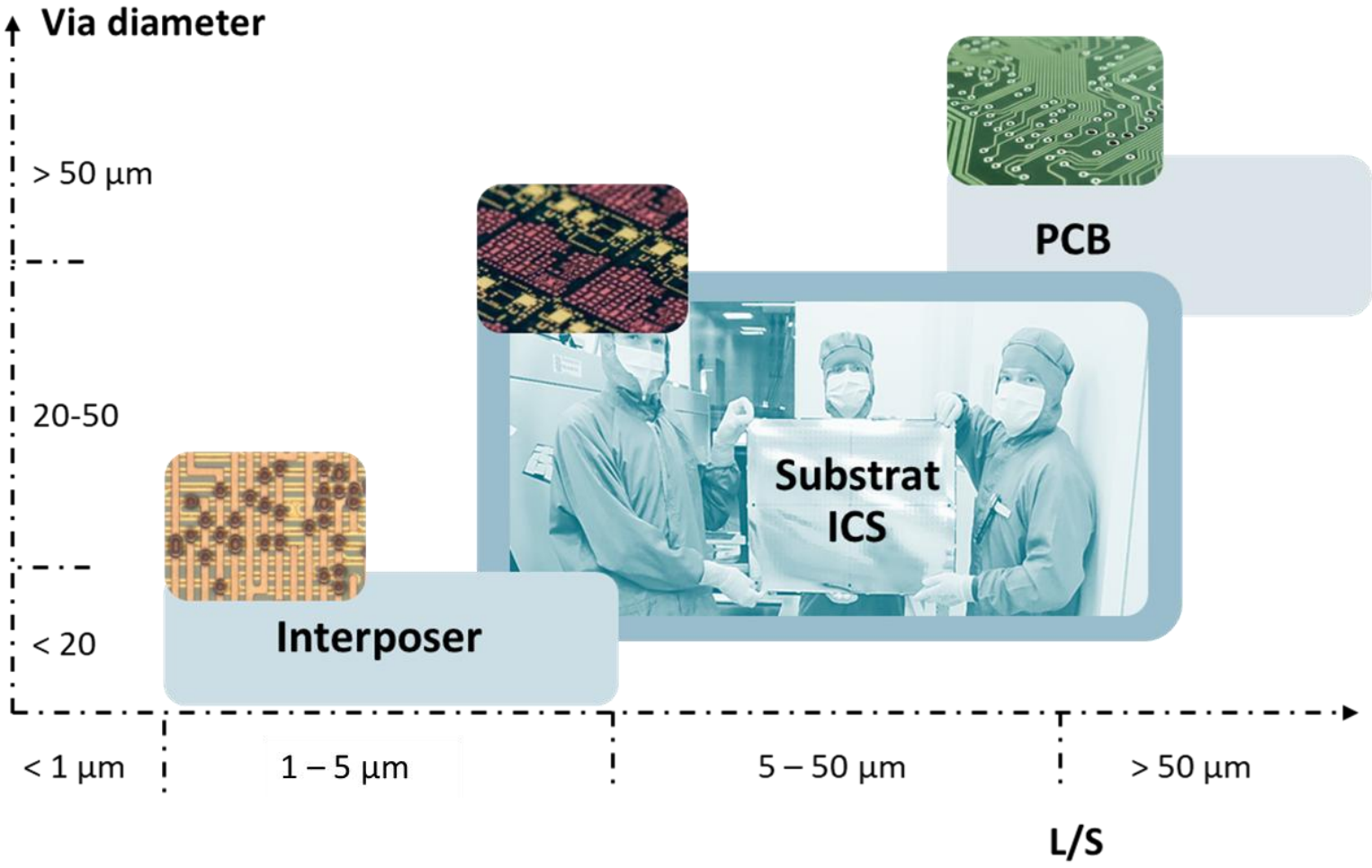


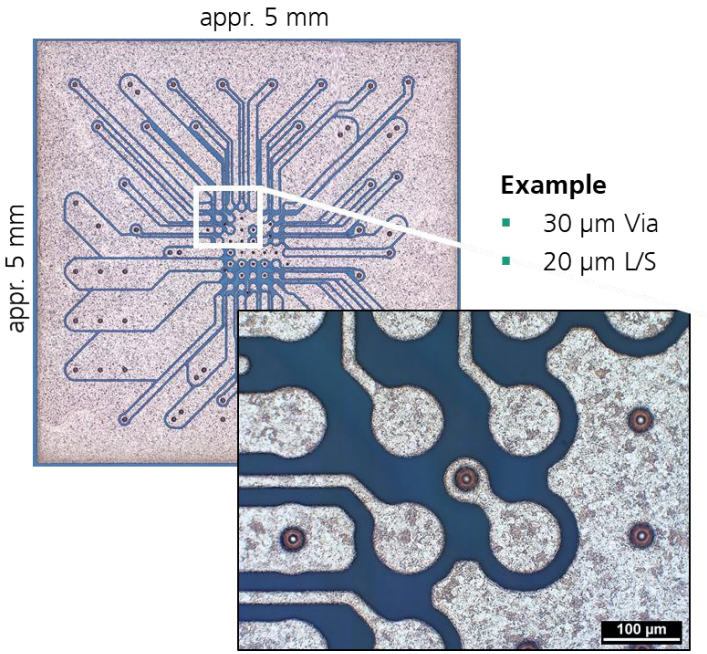
01

Introduction to High Density Substrates Technologies

Introduction Advanced Substrates Technologies

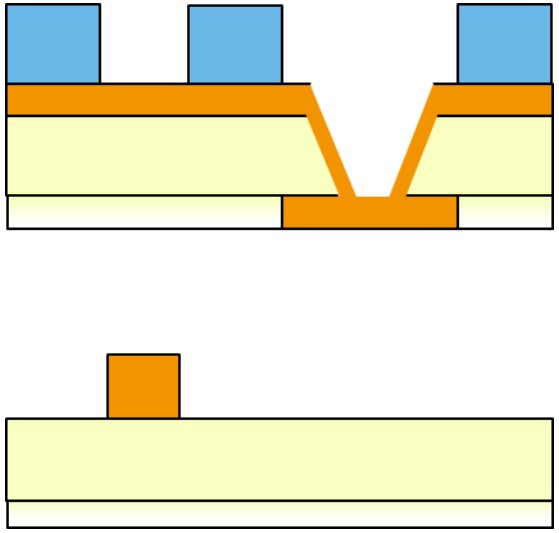
Landscape of Advanced Substrates





mSAP, SAP, aSAP - Panel technologies towards smaller line pitch

mSAP / amSAP

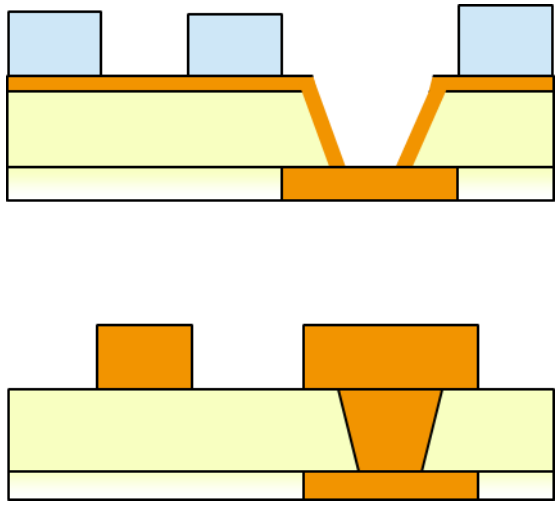


Uses CCL like HDI but thinner

E-less Cu: 1 - 2 µm

50µm to 15µm

SAP

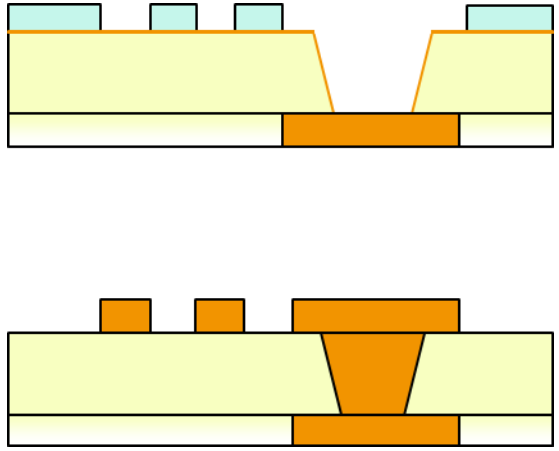


No CCL, uses ABF

E-less Cu: 1 - 2µm

25µm to 8µm

aSAP



No CCL, uses ABF

PVD Seed:

Cu: 50 - 500nm / Ti: ≤ 100nm

10µm - 5µm and below

IZM Panel Level Packaging Line

Process line for the production of IC substrates at the IZM – Feb 2025

Drill

Mechanical drill

Etch

Horizontal DES

Laser Drill

UV Pico Laser

Cleanroom

Clean / Condition

Horizontal Spray

PVD Sputter

Panel PVD

VAC Lamination

Multi layer / Vacuum lamination

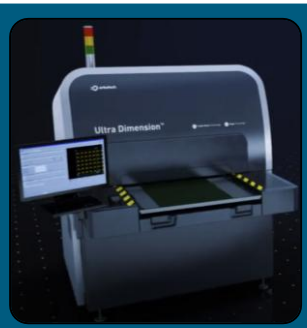
DI Image

LDI / MDI

Cu Plate

Panel plating line

Metrology



Coordinate measurement / AOI

E-Test

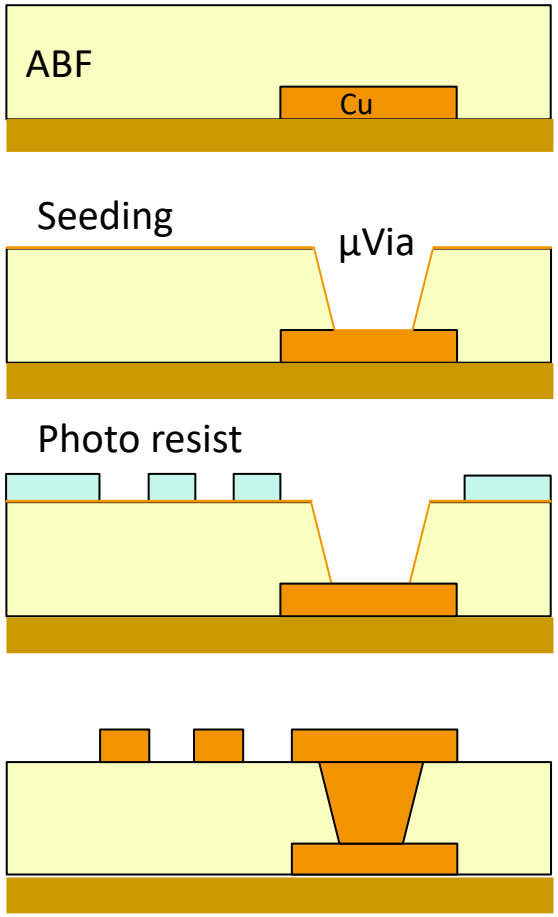
Flying probe testing

02

Advanced Semi Additive (aSAP) - RDL Process

Advanced Semi Additive (aSAP) - RDL Process

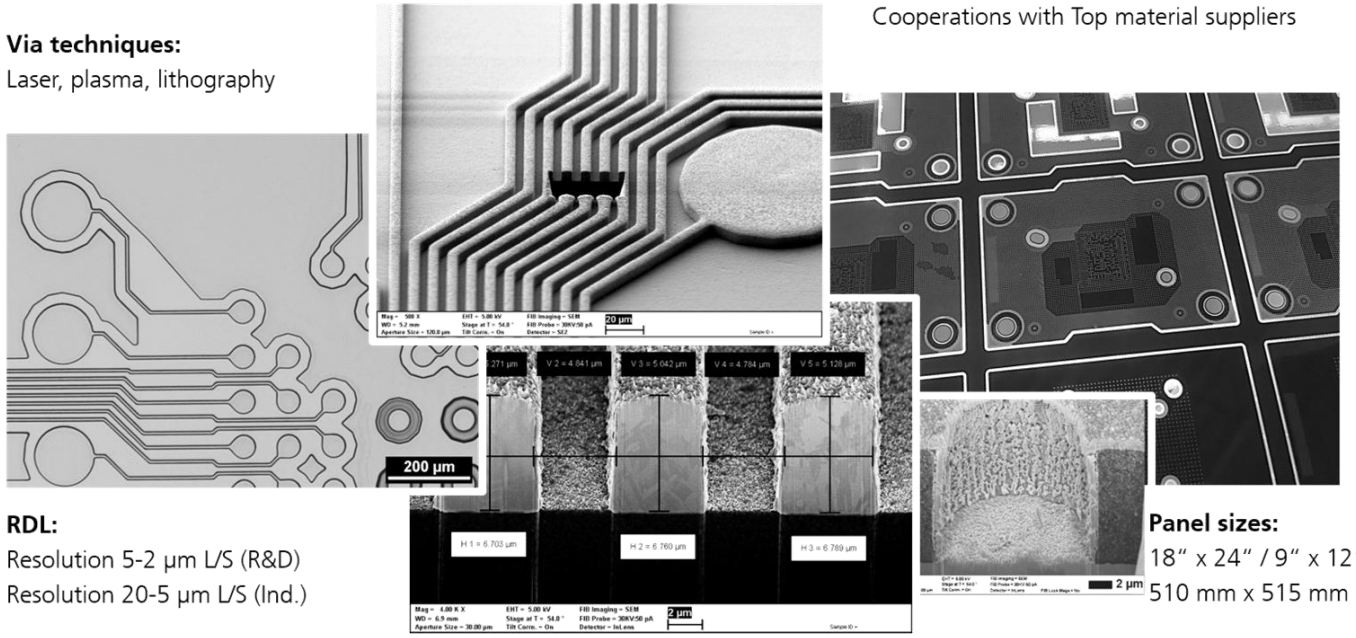
Process Overview



- Dielectric application
- Via formation
- PVD seeding
- Photo resist application
- Lithography
- Electrolytic Cu deposition
- Differential etch

Via techniques:
Laser, plasma, lithography

Materials:
Cooperations with Top material suppliers



RDL:
Resolution 5-2 µm L/S (R&D)
Resolution 20-5 µm L/S (Ind.)

Panel sizes:
18“ x 24“ / 9“ x 12“
510 mm x 515 mm

Substrate Technologies

Via Technologies

Laser Via

- Established process, derived from HDI substrates
- Research Topics:
  - Yield improvement for small via diameter
  - Reduction of minimum via diameter, limits?

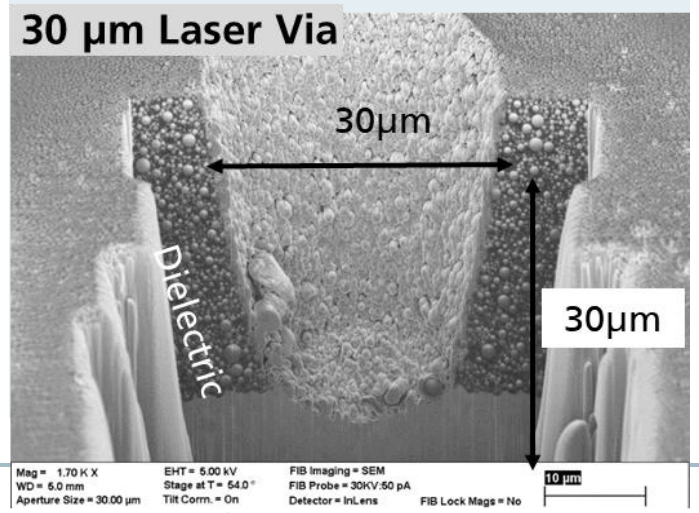
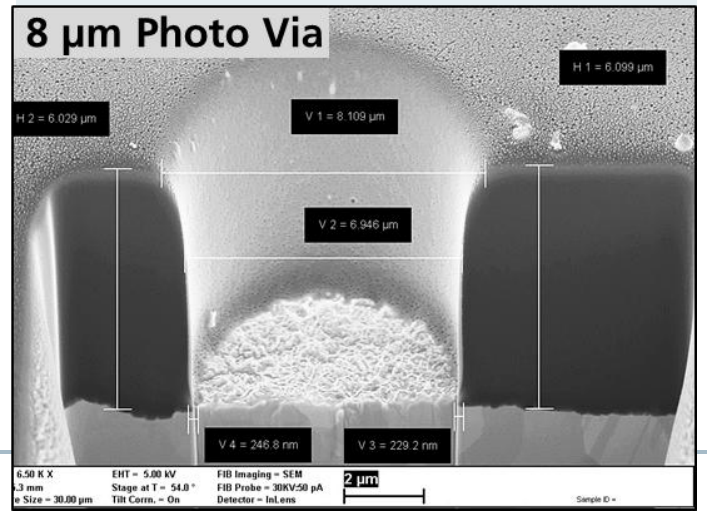


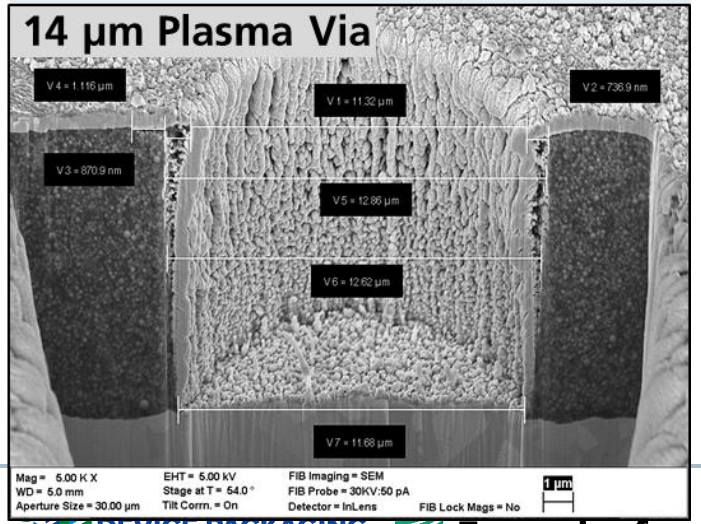
Photo Dielectric (PID)

- New approach on panel level
  High resolution, fast parallel processing
- Research topics:
  - PID materials:
    Application, processability (exposure, develop, post treatment
  - Limits of process



Plasma Via

- New process using dry etching with mask on dielectric
- Research topics:
  - Process: Masking, gas formulation, post treatment
  - Etch rates
  - Via dimensions



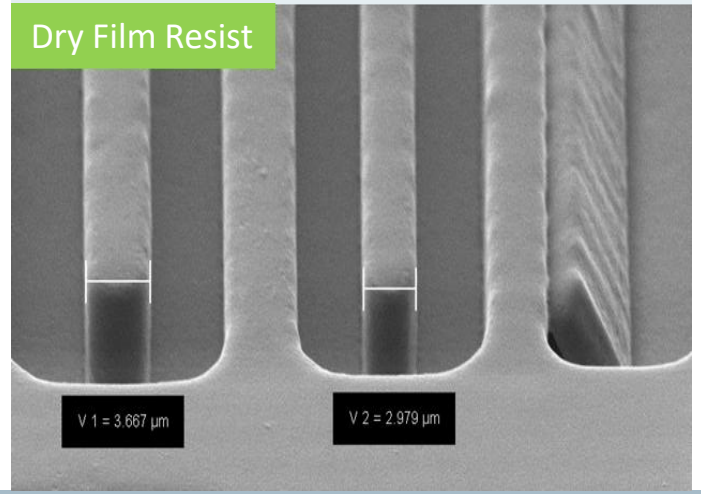
Substrate Technologies

RDL

Litho

- Task: High Resolution DI Exposure
- Research topics:
  - Photoresists and processing
  - Overlay accuracy
  - Target: stable process down to 2µm resolution

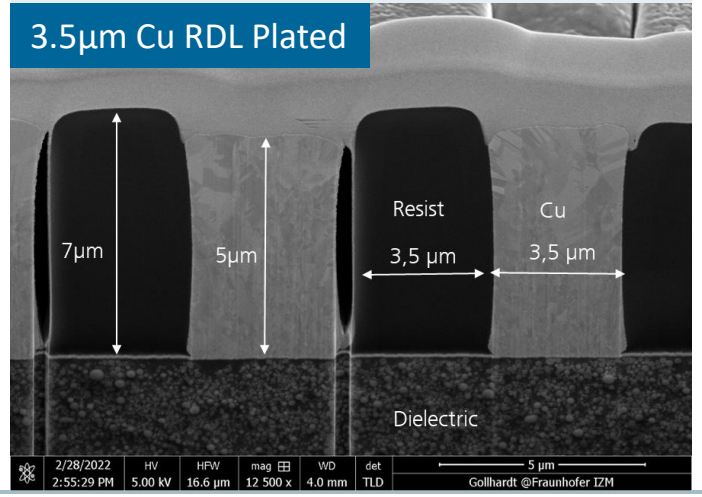
Dry Film Resist



Cu Plating

- Task: Ultra fine line plating on large panel
- Research topics:
  - Overall process
  - Plating uniformity vs. plating speed
  - Uniform plating lines and via

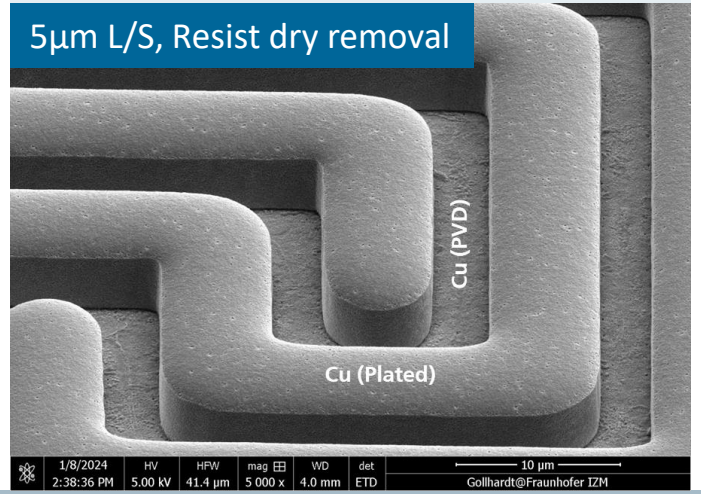
3.5µm Cu RDL Plated



Strip & Differential Etch

- Task: Removal of photo resist and seed metal
- Research topics:
  - Methods: Wet and dry etching
  - Uniformity
  - Defects → Yield

5µm L/S, Resist dry removal



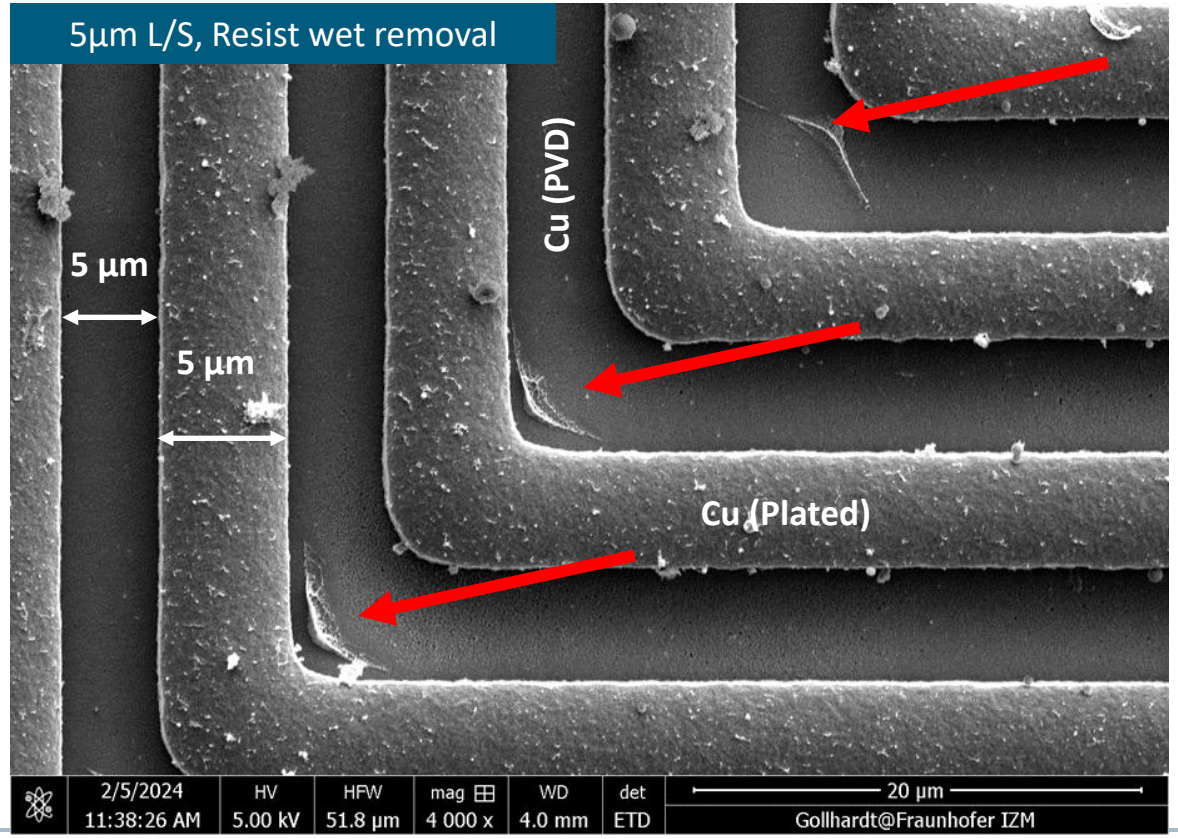
Substrate Technologies

RDL Resist removal

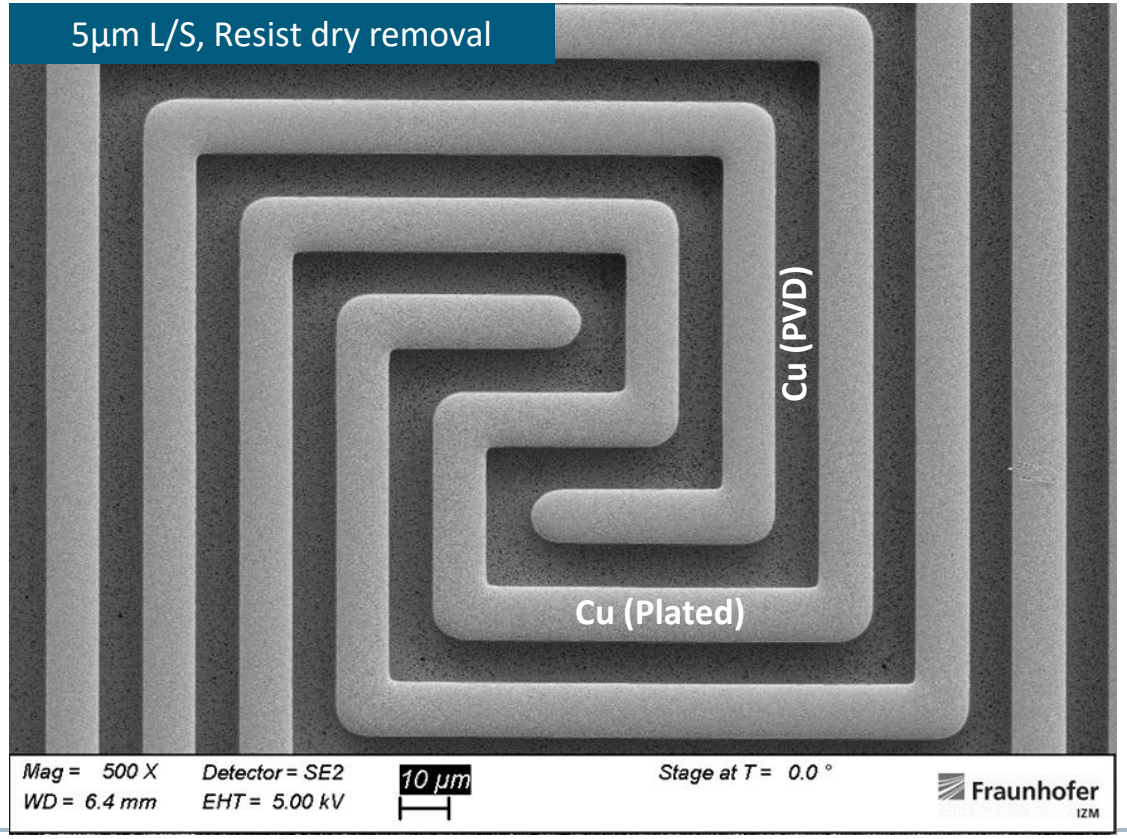
Resist removal after cu deposition

- Left: Wet chemically removed and descum
- Right: Dry etched (Plasma) and wet cleaning

5µm L/S, Resist wet removal



5µm L/S, Resist dry removal

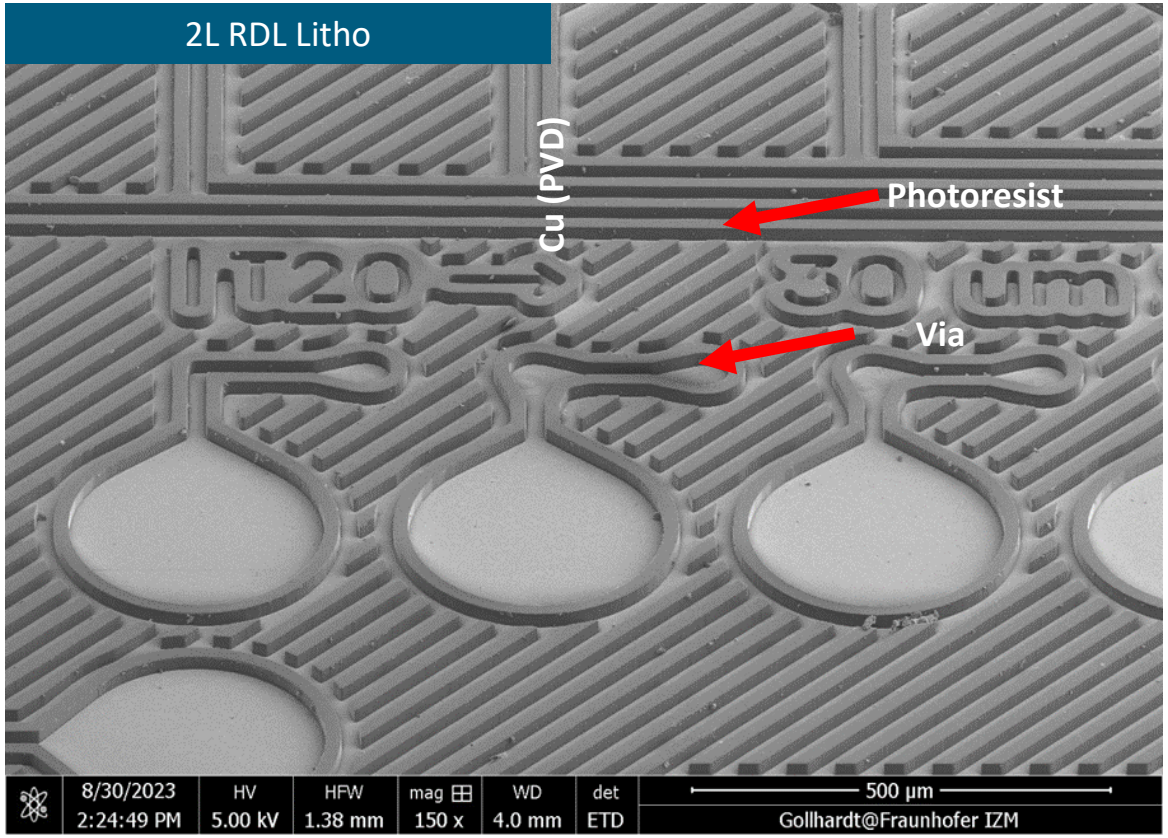


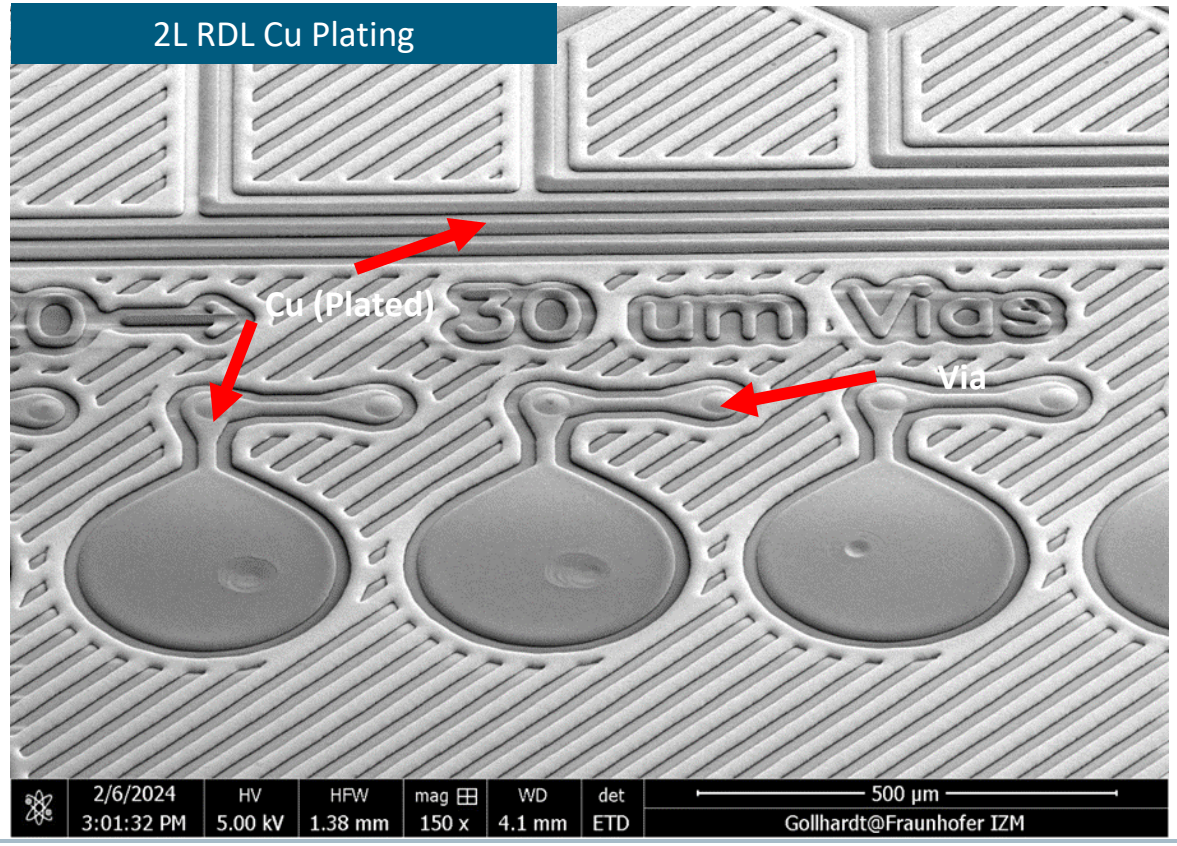
Advanced Semi Additive (aSAP) - RDL Process

RDL – Litho & Plating

Plating of Lines and Via

- Left: Photoresist exposure & developed
- Right: SAP Cu plating and resist removal



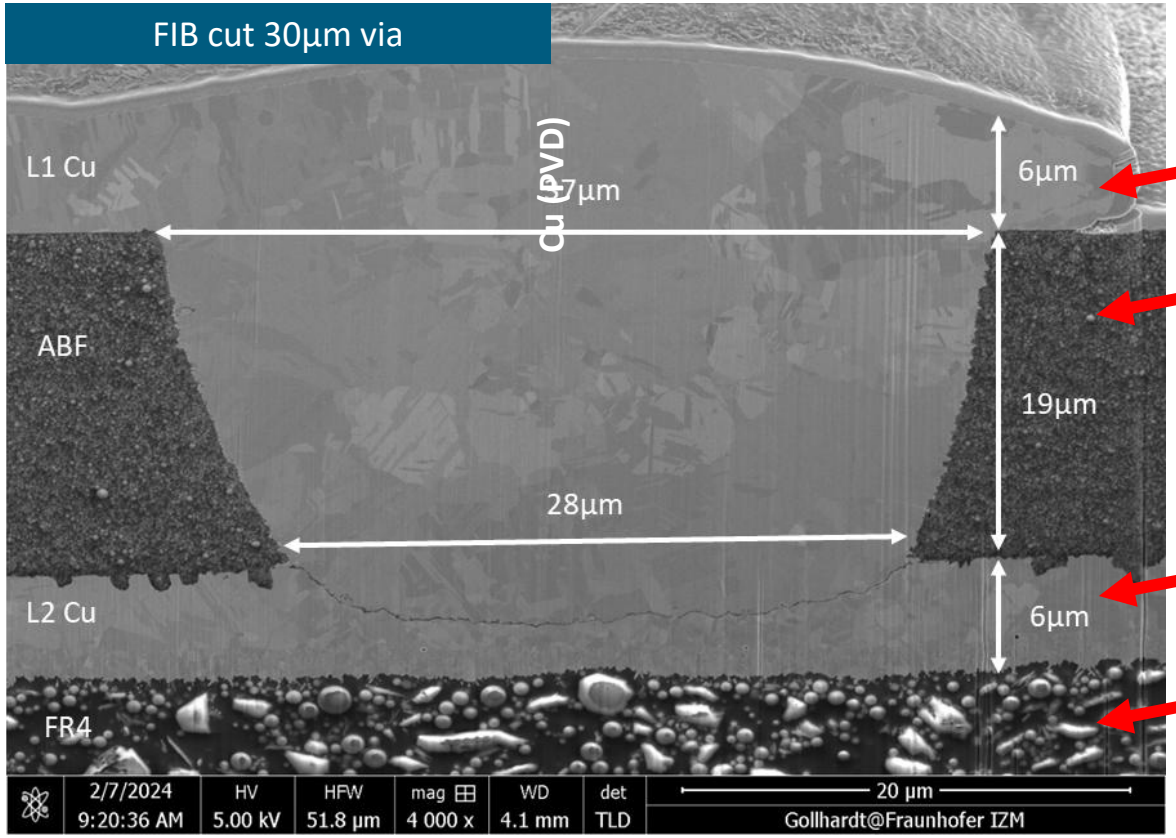


Advanced Semi Additive (aSAP) - RDL Process

RDL – Litho & Plating

FIB cross section

- 30µm via after SAP copper plating of lines and blind via



Plated Cu

Dielectric

Cu on Core

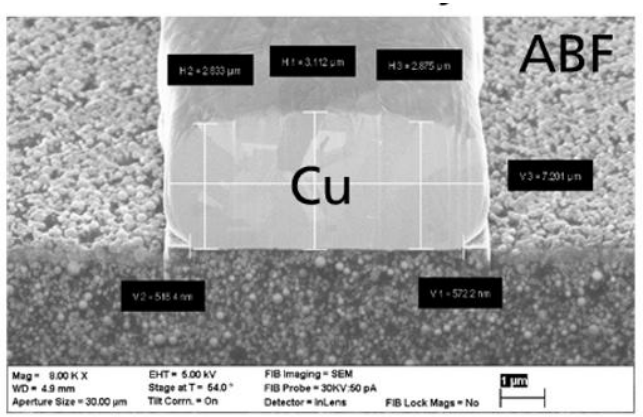
Core

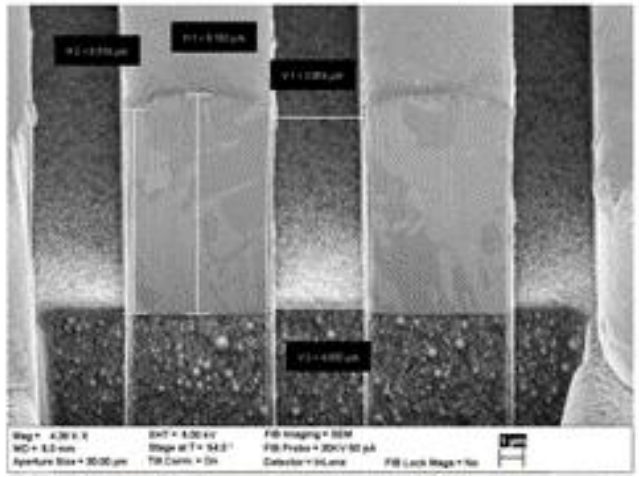
Advanced Semi Additive (aSAP) - RDL Process

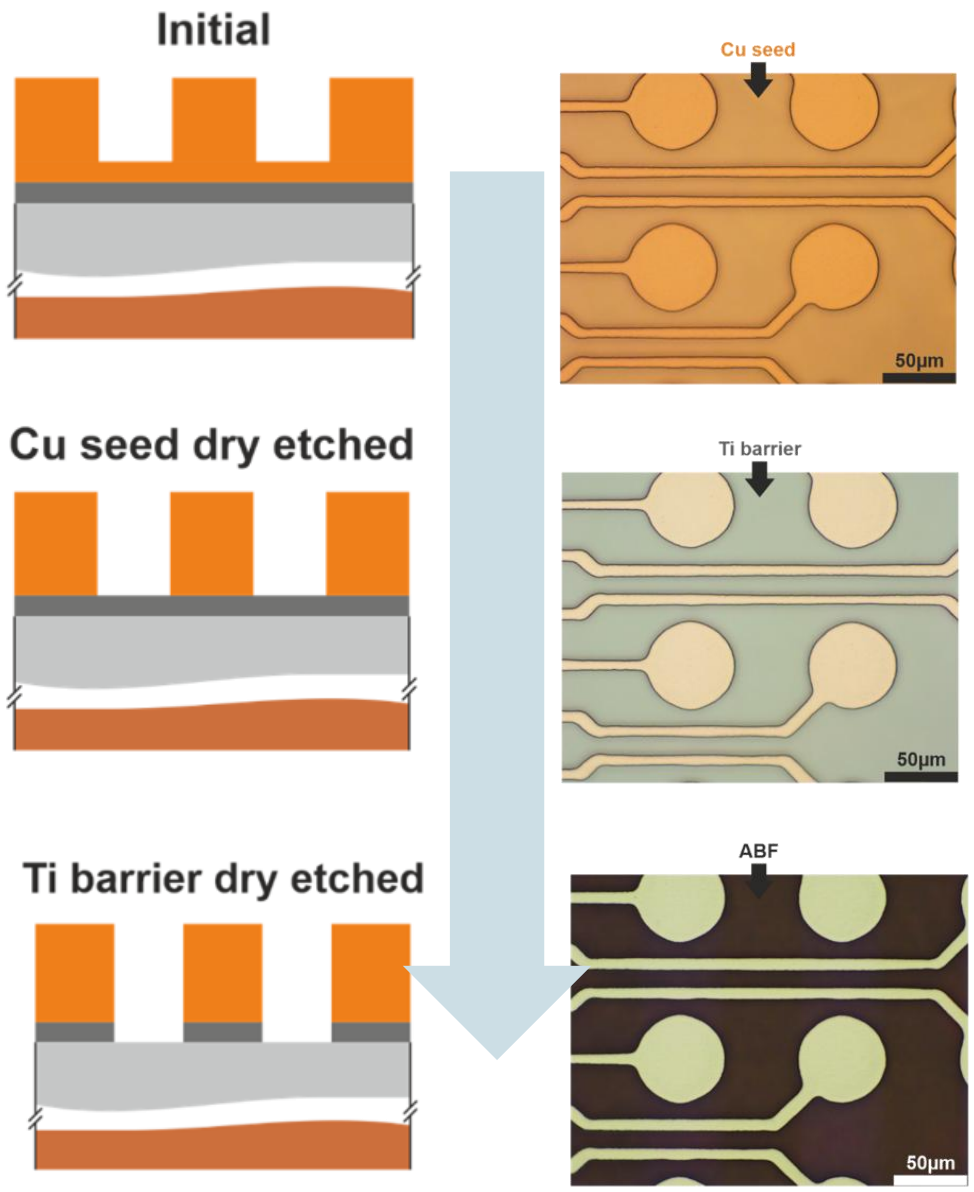
RDL - Seed etch

Cu and Ti differential etching

- Wet chemical methods limits minimum line width and space due to under etching of plated copper
- Structures below 5µm require minimum under etching
- Dry etching with almost anisotropic process could be an alternative





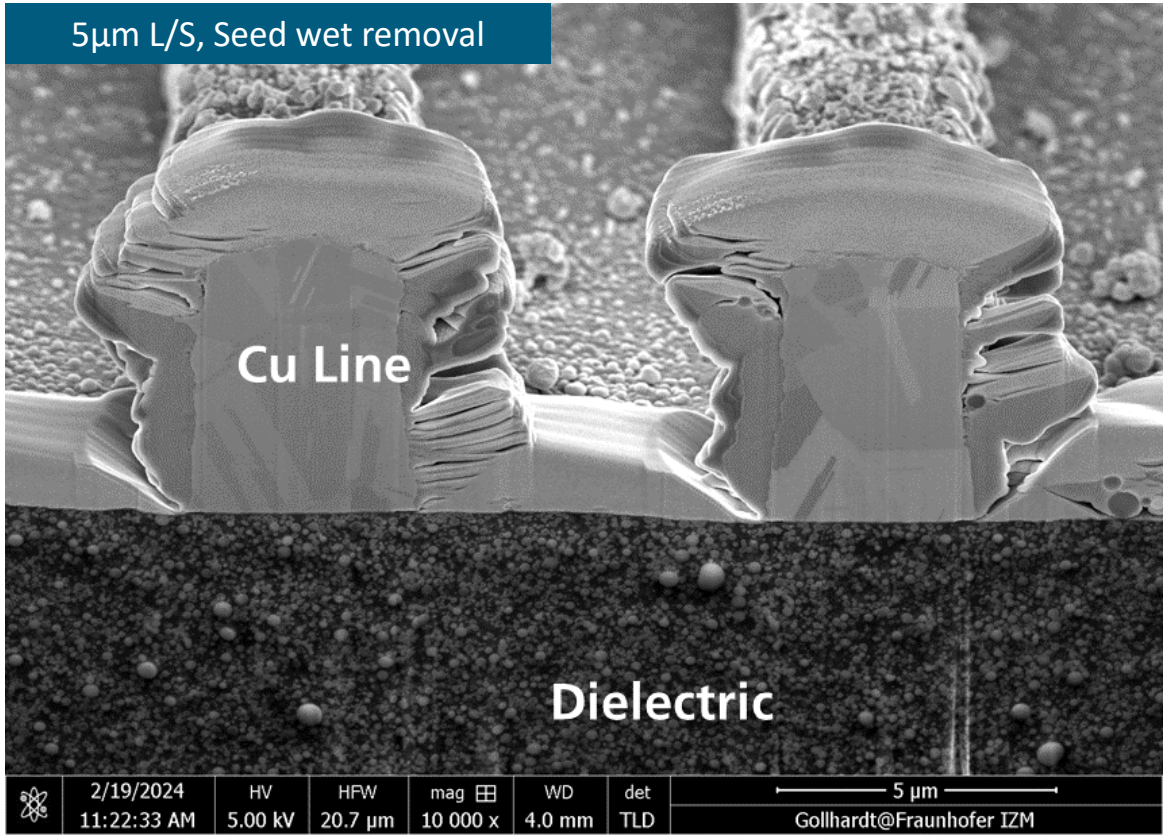


Advanced Semi Additive (aSAP) - RDL Process

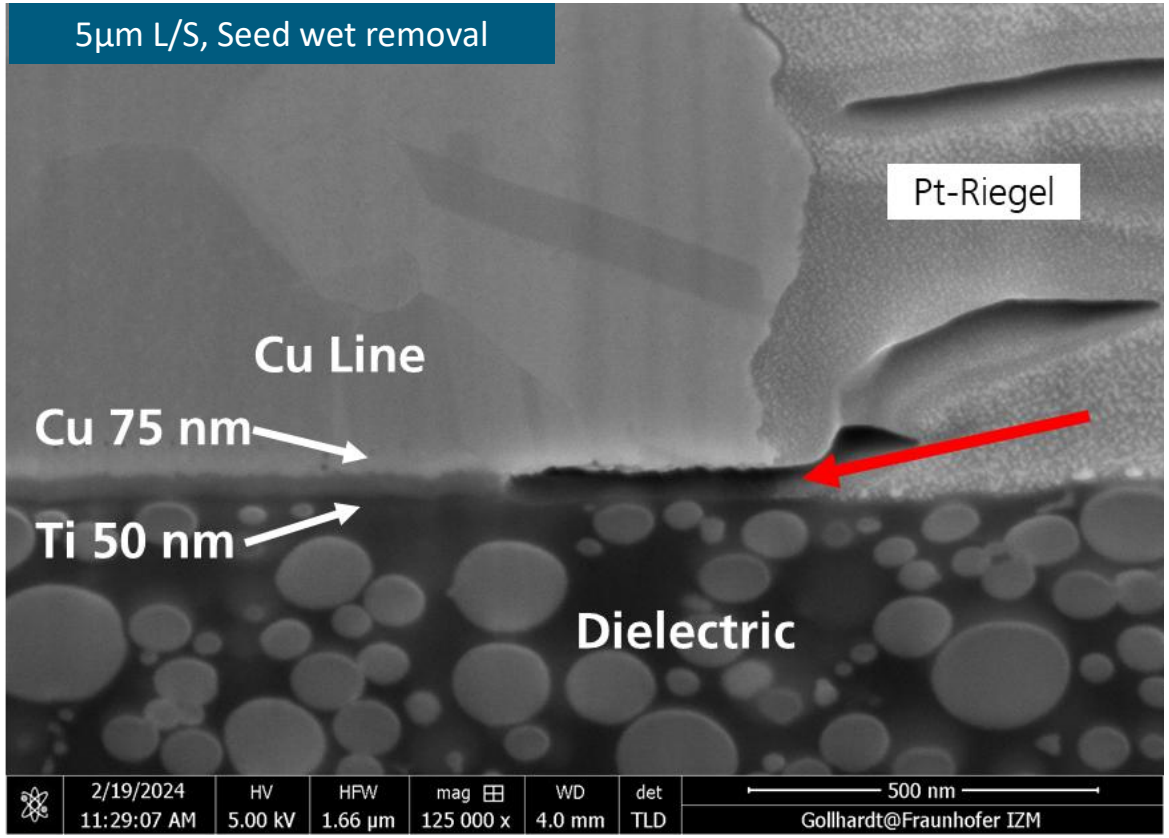
RDL – Wet vs. Dry Seed etch

Wet chemical Cu and Ti differential etching

5µm L/S, Seed wet removal



5µm L/S, Seed wet removal

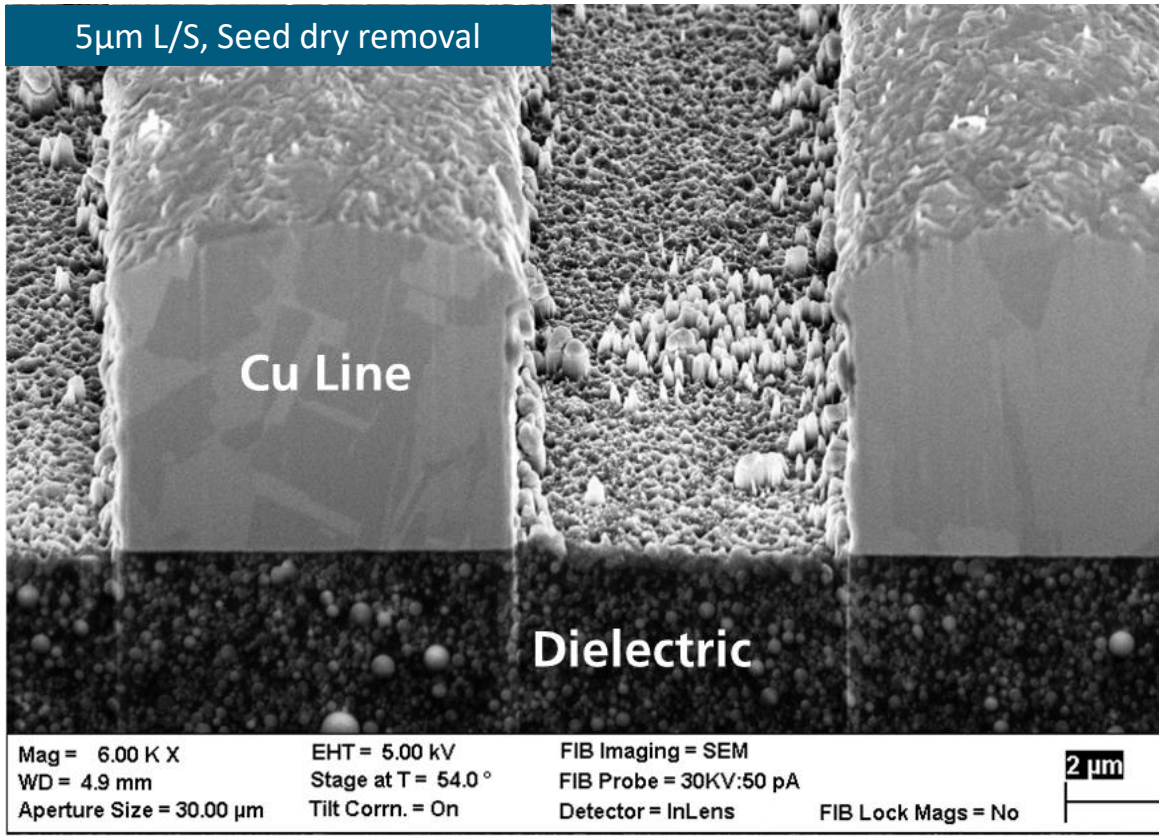


Advanced Semi Additive (aSAP) - RDL Process

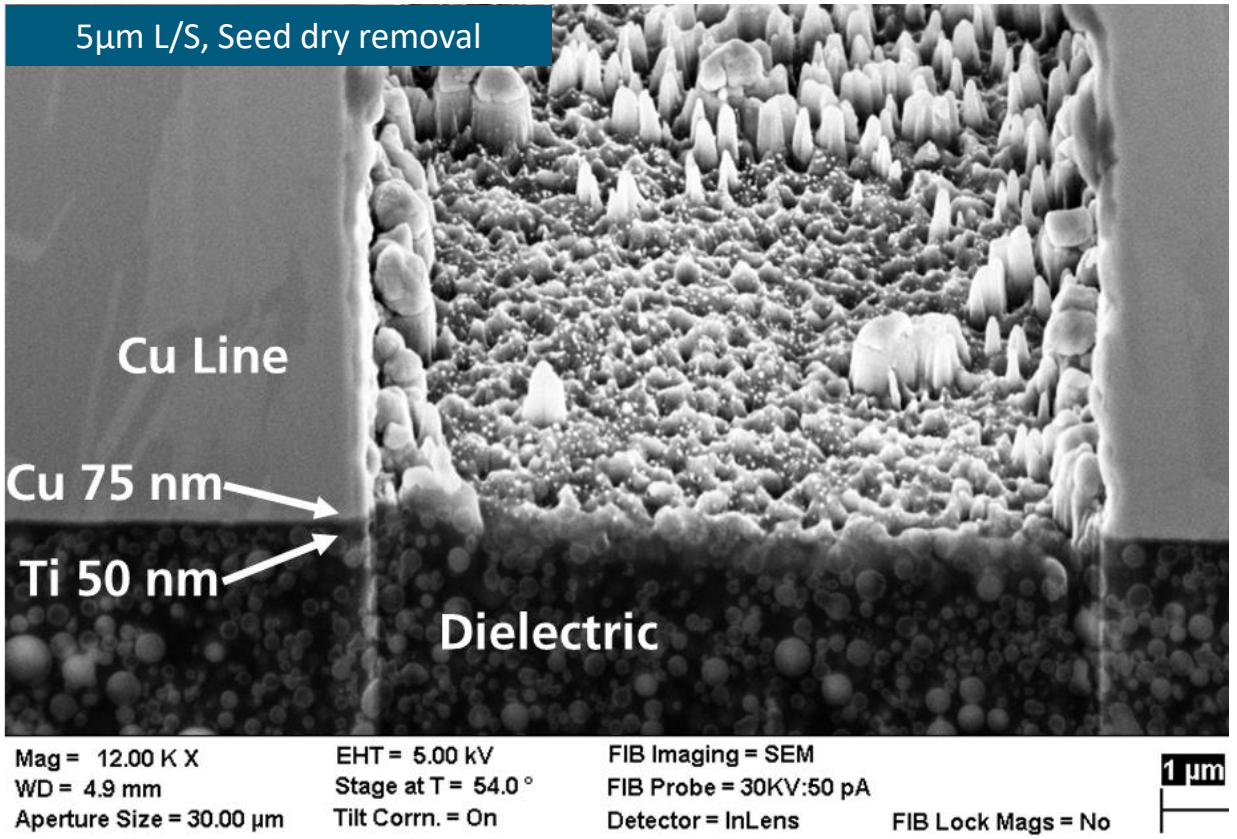
RDL – Wet vs. Dry Seed etch

Dry Cu and Ti differential etching

5µm L/S, Seed dry removal



5µm L/S, Seed dry removal



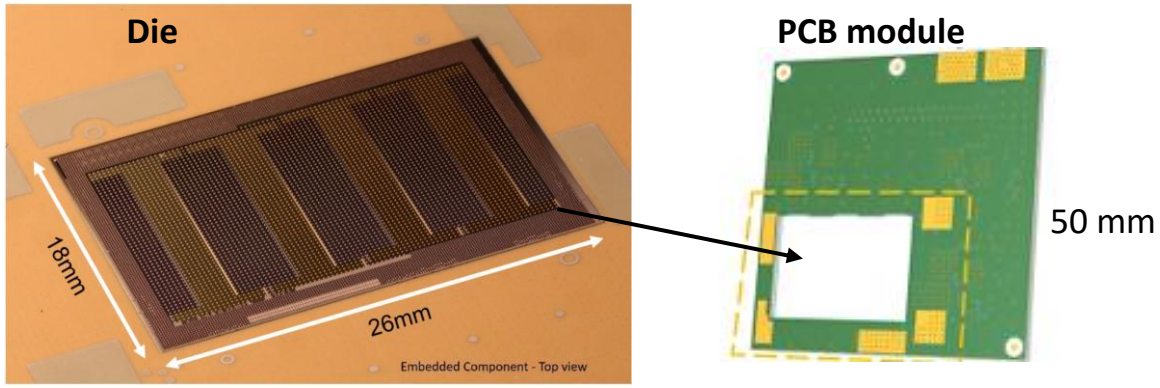
03

EU Project “CHARM”

Introduction to EU project CHARM

- **CHARM** (**C**reating **H**olistic **A**pproaches for **R**esilience and **M**ental health in the European Labour Market)
- European Union-funded project that aims to improve the mental health and well-being of workers
- One target was to build enablers for autonomous mining vehicles
- A high performance module containing a large compute die in an innovative embedding approach was developed and build up

9179 contacts
50µm diameter
150µm pitch



Partner

Valmet, aixACCT systems, Applied Materials, AT&S, beneq, Besi, Canon Production Printing, EUNET, csem, TU Delft, E+E Elektronik, Fraunhofer IZM, imec, InnoSenT, Lapin AMK, LGE, Łukasiewicz, mcl, nome, PacTech, QPLOX, Quantavis, Reden, Riga Technical University, SAF, Sandvik, Smart Motion, SSH.COM, sylvac, Tampere University, TU Chemnitz, Tornos, TIPb, ÚJV, University of West Bohemia, Würth Elektronik

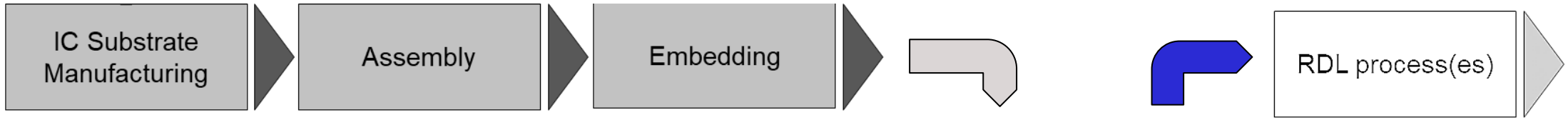
Founded by:
BMBF FKZ 16MEE0012

Gefördert vom Bundesministerium für Bildung und Forschung

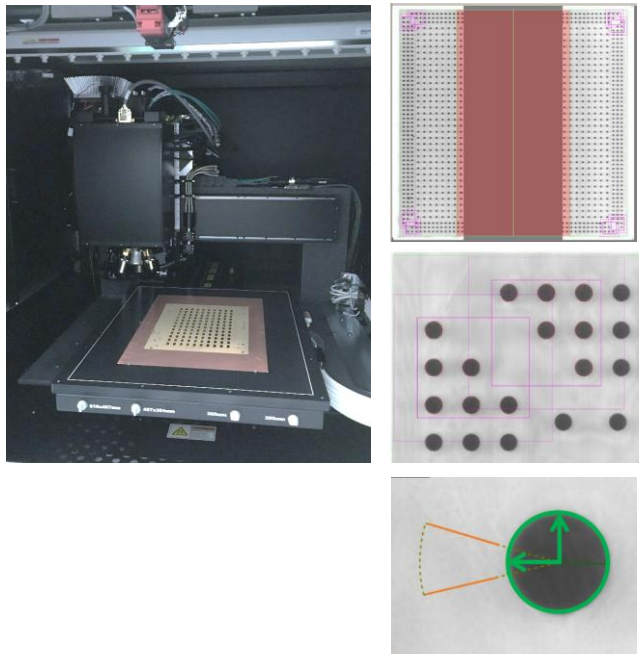
CHARM, ECSEL JU

Basics of an adaptive redistribution patterning process

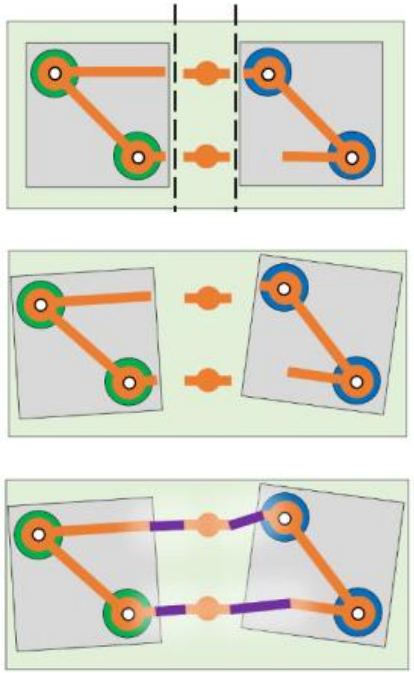
Process sequence

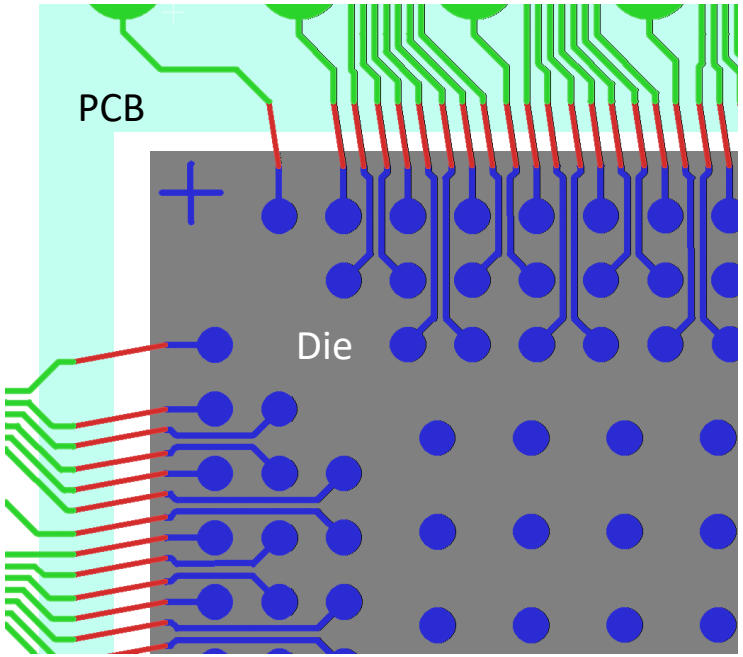


1. Coordinate Measurement (CMM)



2. Artwork / CAM Data Manipulation / DRC and Output to RIP process





red
flexible
traces

blue
artwork
rotated
+translated

green
artwork
fixed

Adaptive RDL process

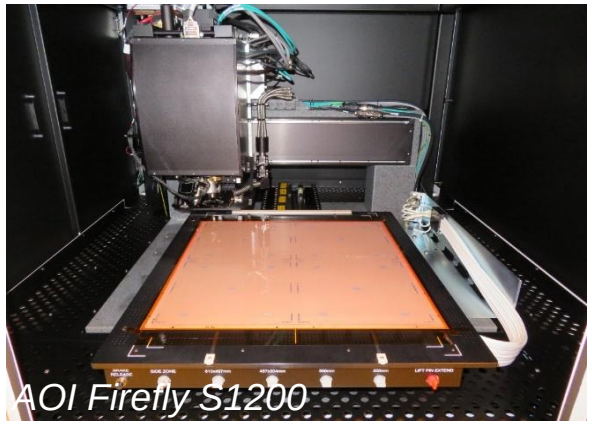
Coordinate measurement

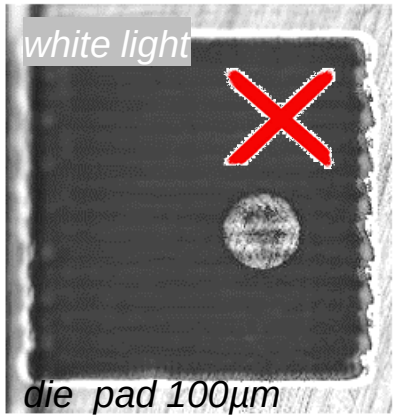
Method

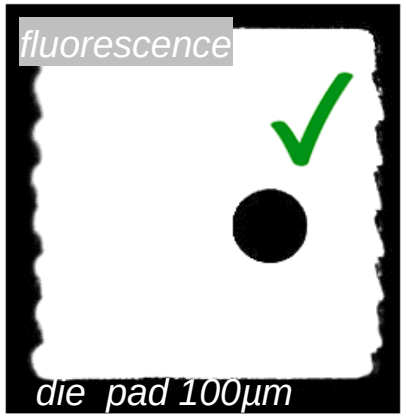
- Opening of marks on substrate and dies (etching or laser)
- Use of high precision coordinate measurement machine (CMM)

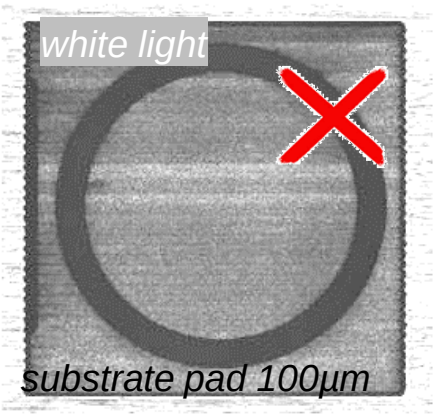
Results

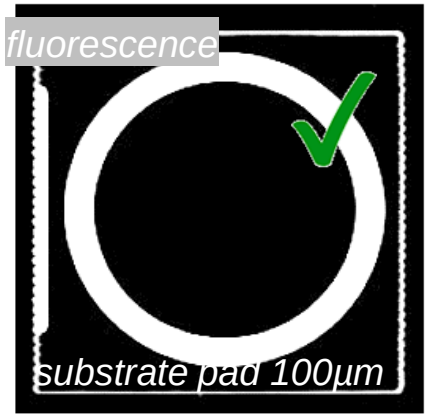
- Measurement of using fluorescence sensor yields in best detection rate of contrast ABF dielectric to metal (copper)
- Measurement time: 95s for 25 large dies with each 2 registration marks and 20 substrate marks











Adaptive RDL process

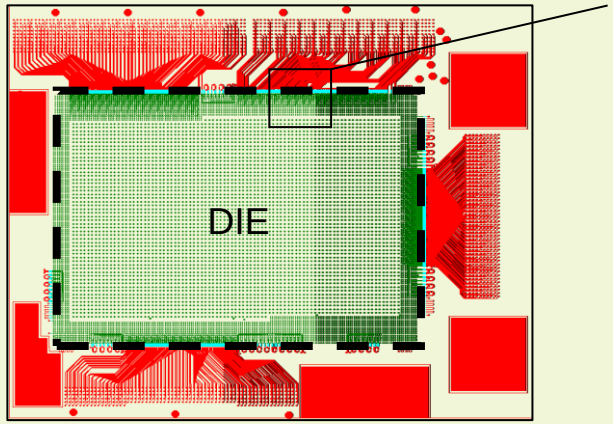
Artwork and data processing

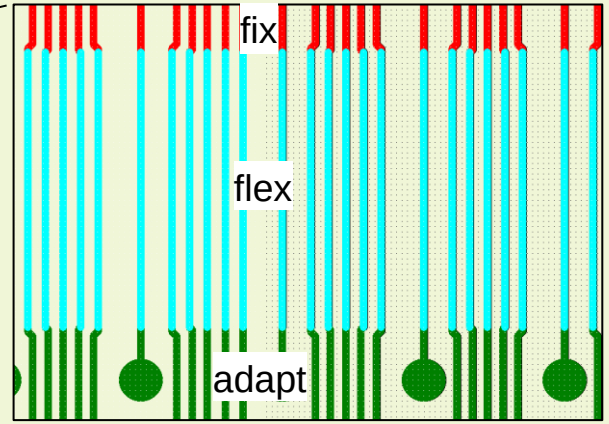
Method

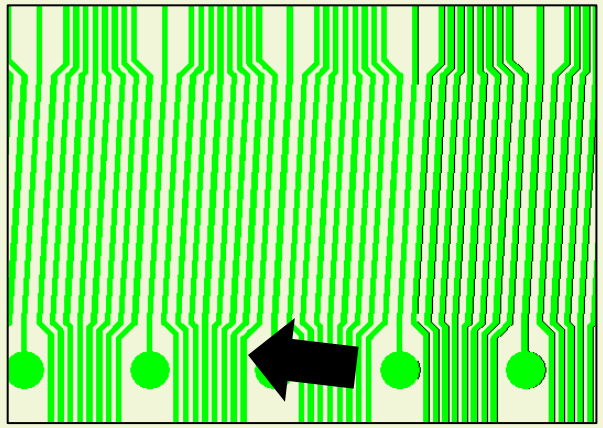
- Artwork redrawing based on coordinate data and vector data
- Artwork calculation: GBR based script programmed at IZM and processing optimized with multi threading, and 64Bit usage of RAM

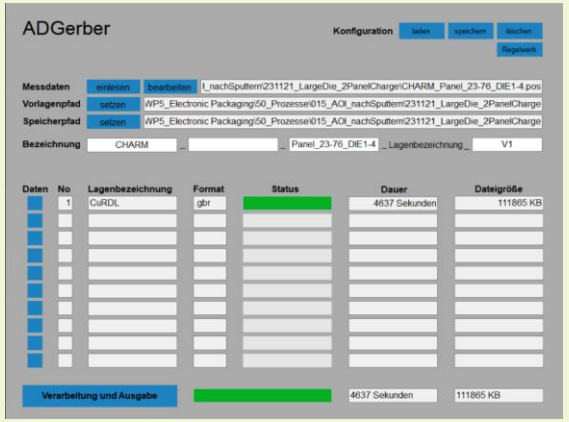
Results

- Thousands of connections, pads and elements needed to be processed
- Optimization of algorithm yielded in reduction of calculation time per adapted artwork per module from hours to 15min per module







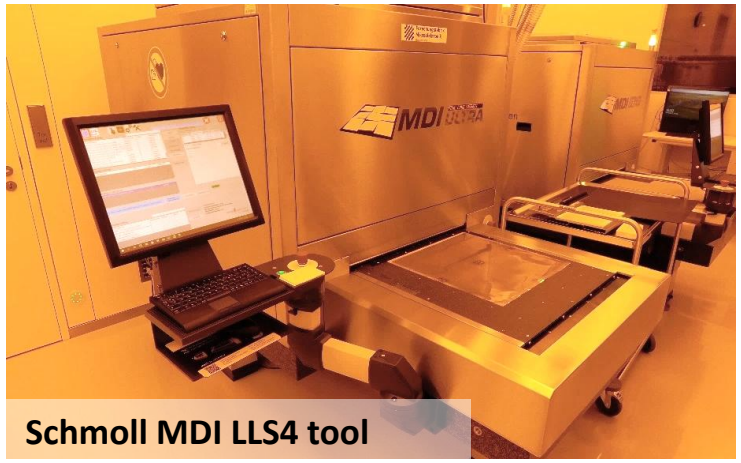


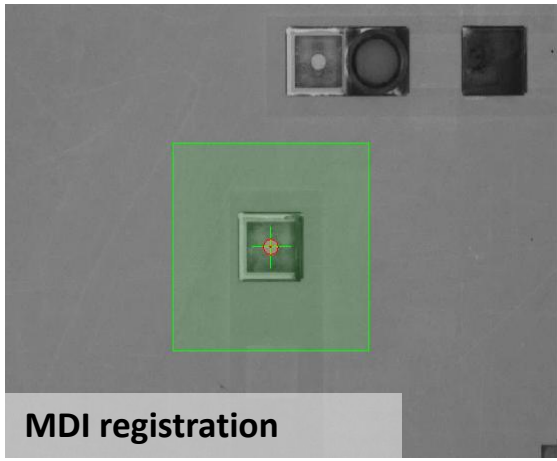
Adaptive RDL process

Lithography

Method

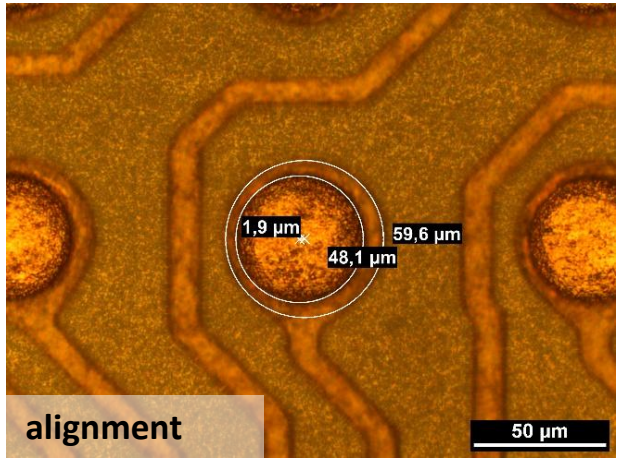
- Processing of raster image data out of adapted layout, exposure using high resolution direct imaging system (DI)
- Co-calibration of DI and CMM using panel size quartz calibration master





Results

- Alignment error between 2µm and 6µm
- 5µm L/S using 10µm thick DFR achieved
- Surface quality of substrate does highly effect lithography result (roughness/scratches)



Adaptive RDL process

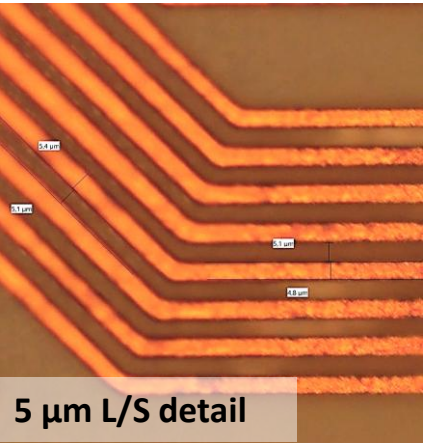
RDL process

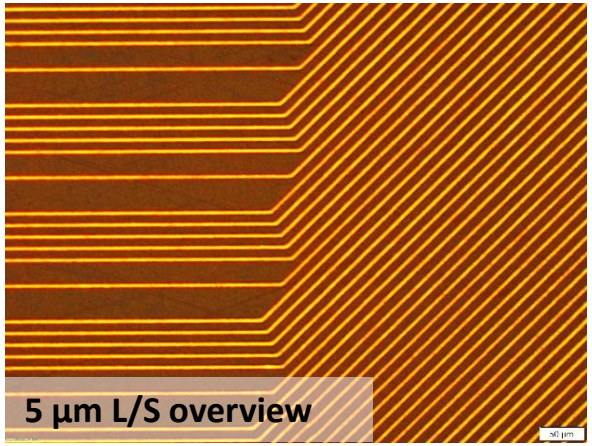
Method

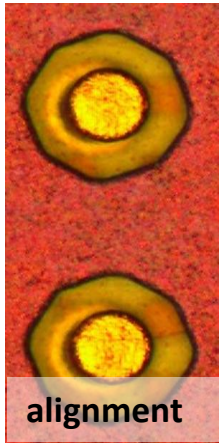
- RDL plating: Electrolytic Cu plating, resist removal and differential sees etch
- Double sided SAP on 610x47mm² large and 150 thin substrates with embedded dies with a size of 26x18mm²

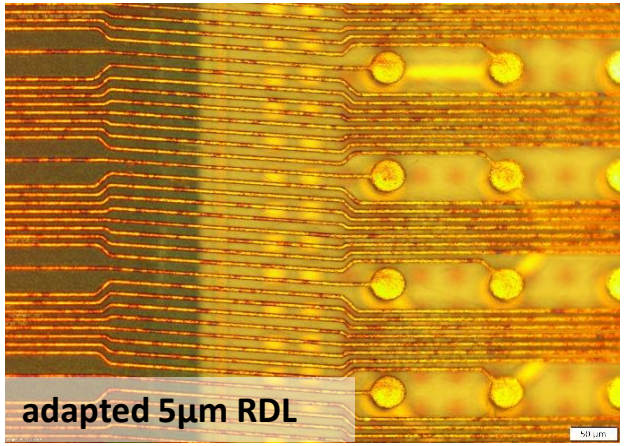
Results

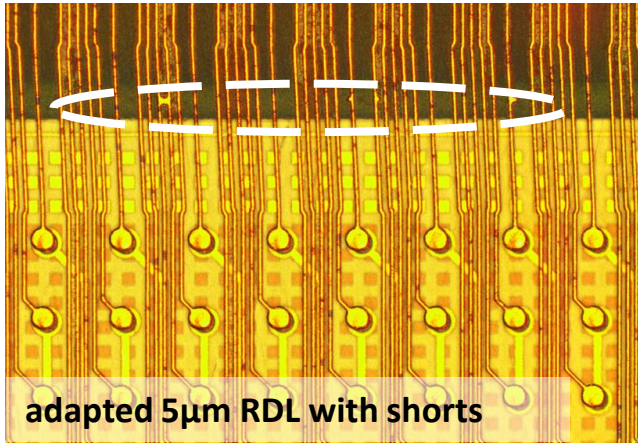
- Successful demonstration of 5 µm L/S RDL
- Connection of 9152 I/O on the dies with a maximum of 2 to 6µm alignment tolerance
- Yield of 5µm structures still low, due to limited number of available substrates allowing only a few iterations and optimization runs


5 µm L/S detail


5 µm L/S overview


alignment


adapted 5µm RDL


adapted 5µm RDL with shorts

Project CHARM

Summary

Adaptive Imaging:

- Measurement of die positions on each panel after placement, embedding, pillar reveal and sputtering
- Adaption of the design data stack for each unique package and panel
- Generation of raster imaging data (RIP) for direct imaging

Adaptive RDL formation:

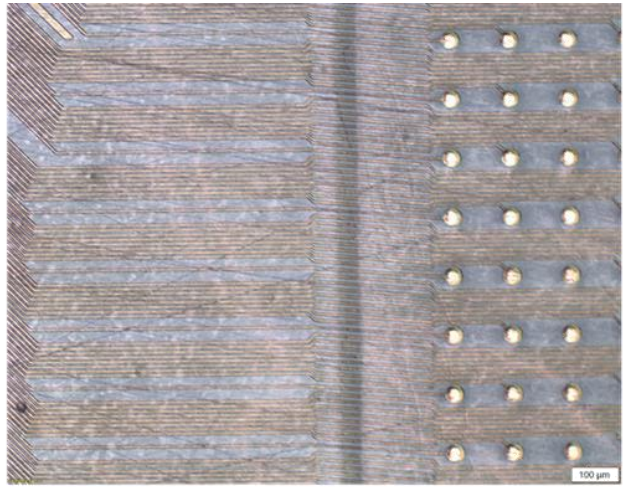
- Direct exposure using adapted, genuine layout data
- Ultra fine-line Cu plating, resist strip and seed etch

Results:

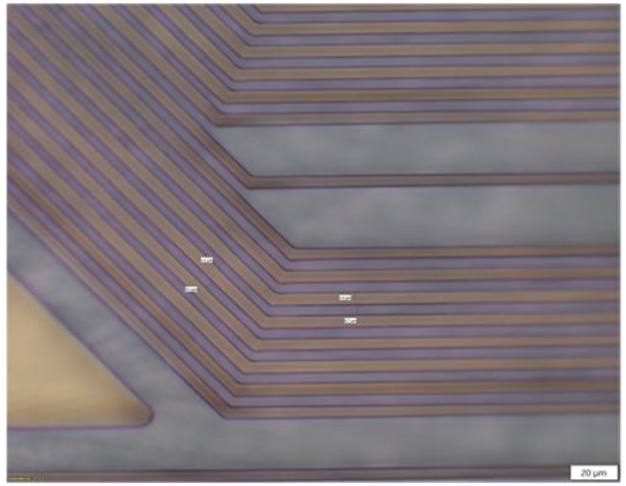
- Development of core steps for adaptive imaging: measurement of die shift and rotation, processing of adapted layout data and rasterization of imaging data for exposure
- Implementation of complete process chain for adapted semi-additive (SAP) RDL process of embedded fine pitch dies down to 5µm lines and spaces high density routing
- Successful demonstration of RDL process on the computing module manufactured by AT&S in UC1b

Project CHARM

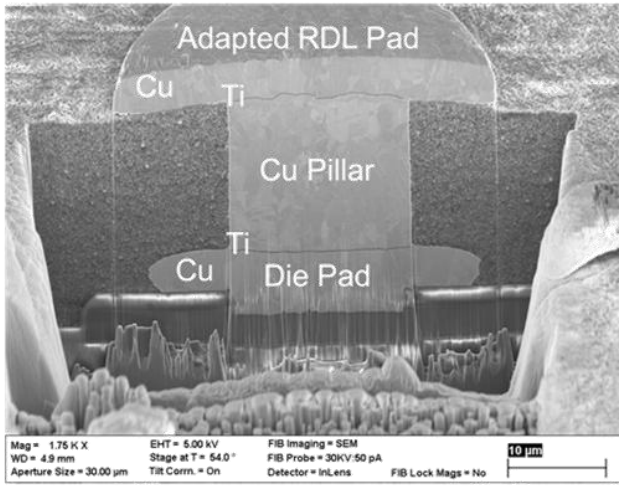
Summary



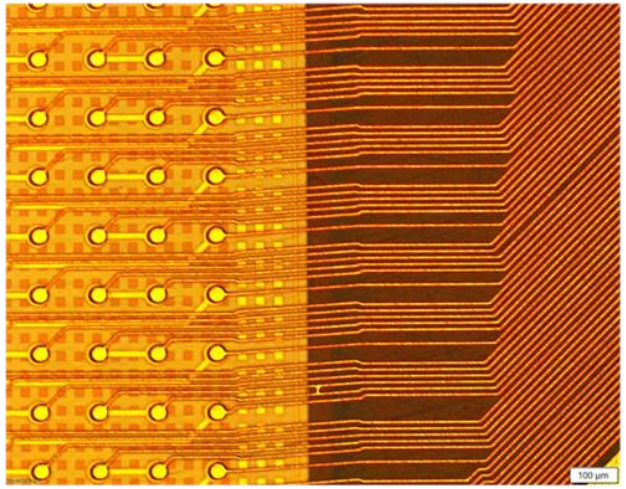
5µm L/S Litho over die/substrate gap



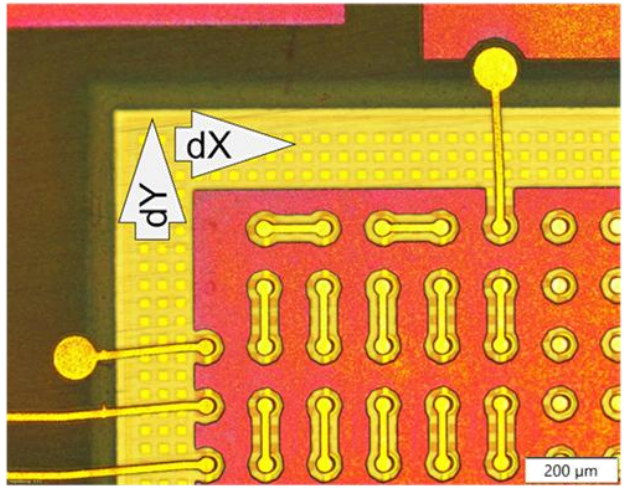
5µm L/S fine resist after development



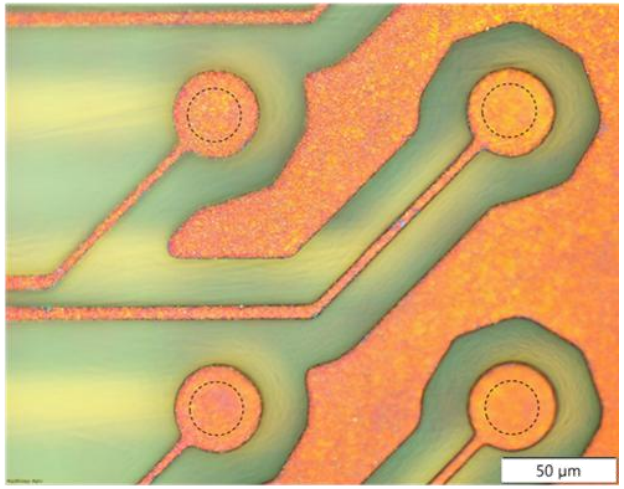
FIB/SEM analysis of connected Cu bump



overview of adapted 5 µm L/S RDL



detail of an adapted 20 µm line



detail of matching bump to RDL
with layer to layer accuracy < 5µm

04

Conclusion

Conclusion

1. aSAP process flow, with different process options for vertical and horizontal interconnects for RDL of high-density organic substrates
2. RDL processing was optimized and alternative process option like dry resist strip, and seed etch as well as dedicated panel galvanic were implemented
3. Adaptive processing provides a technology method to address RDL formation for embedded components if machine tolerances exceed component to RDL layer tolerance
4. Adaptive processing requires the highest degree of machine and data flow automation to read in coordinate data, adapt the artwork and output machine data like rasterized images for digital lithography and adapted laser drill positions
5. Successful demonstration with EU project CHARM to realize first level interconnect and redistribution for computing module with embedded large, high I/O count die

Thank you for your attention!

Contact

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