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Automated Multi-Physics Reliability-Oriented Layout Design for Multi-Chip Power Modules Using the LAREL Tool

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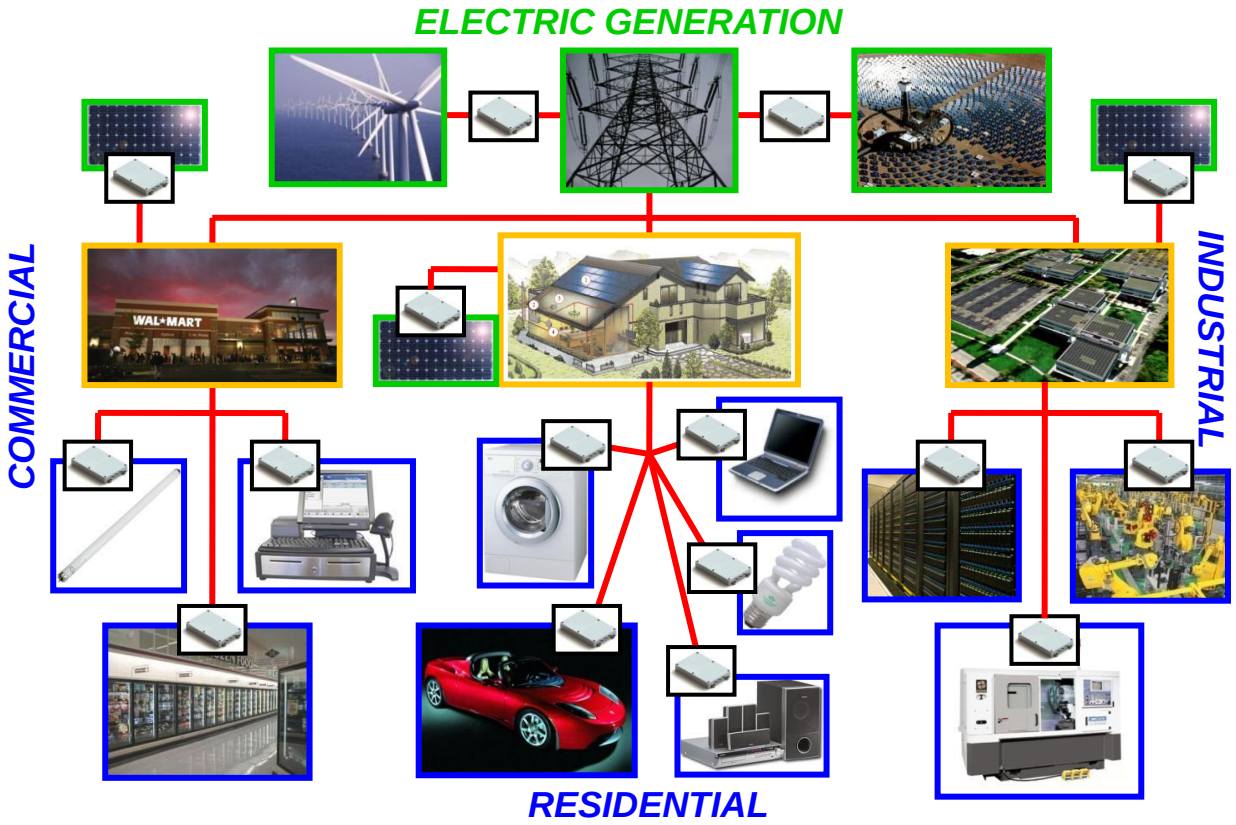
Content Overview

- Motivation
- Background
- LAREL Tool (EDA Tool Integration)
- Case Study
- Conclusions & Outlook
- Q&A

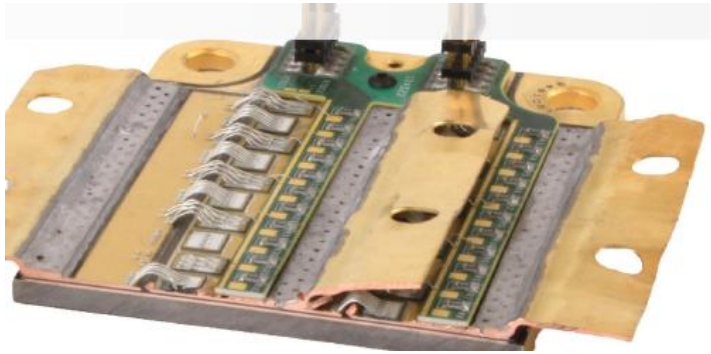


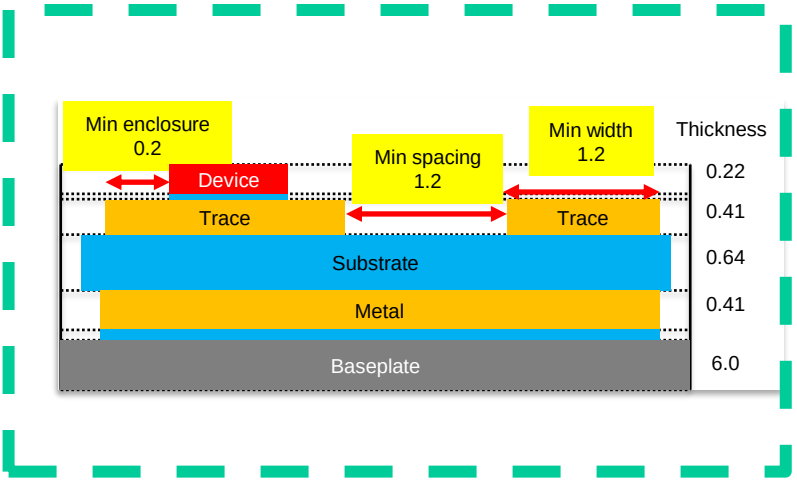
Motivation

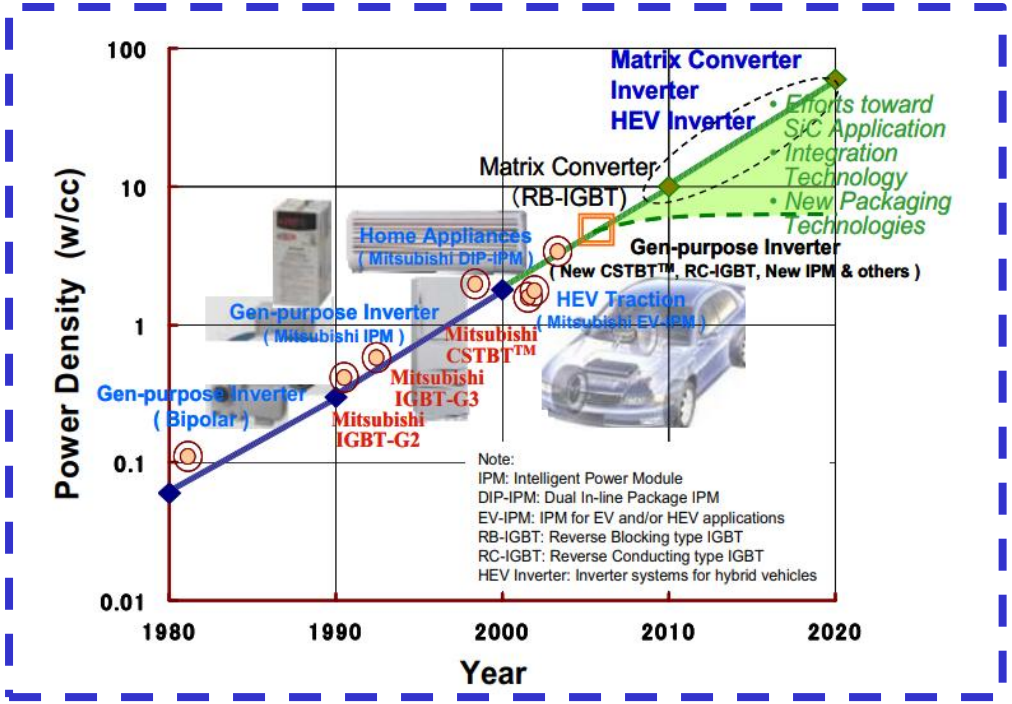
➢ State of the Art: Commercial Power Modules

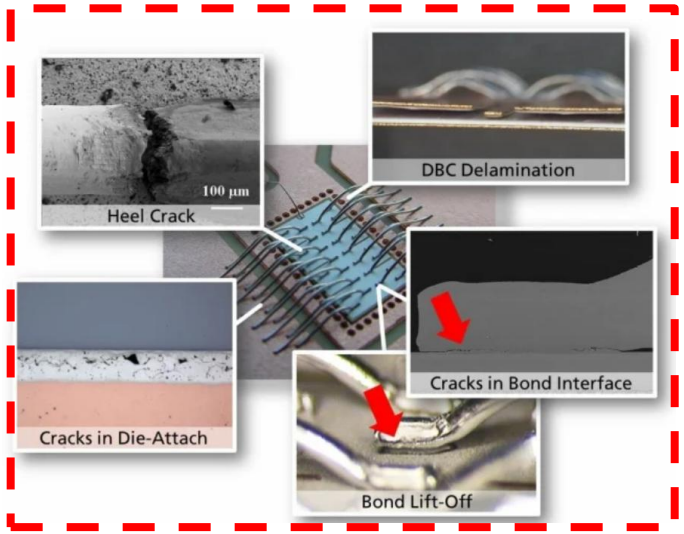
- **Challenges**
  1. **Parasitic Control**
  2. **Thermal Management vs. High loss density**
  3. **Reliability & Manufacturability**

e.g. Wolfspeed high performance HT 3000 module & cutaway



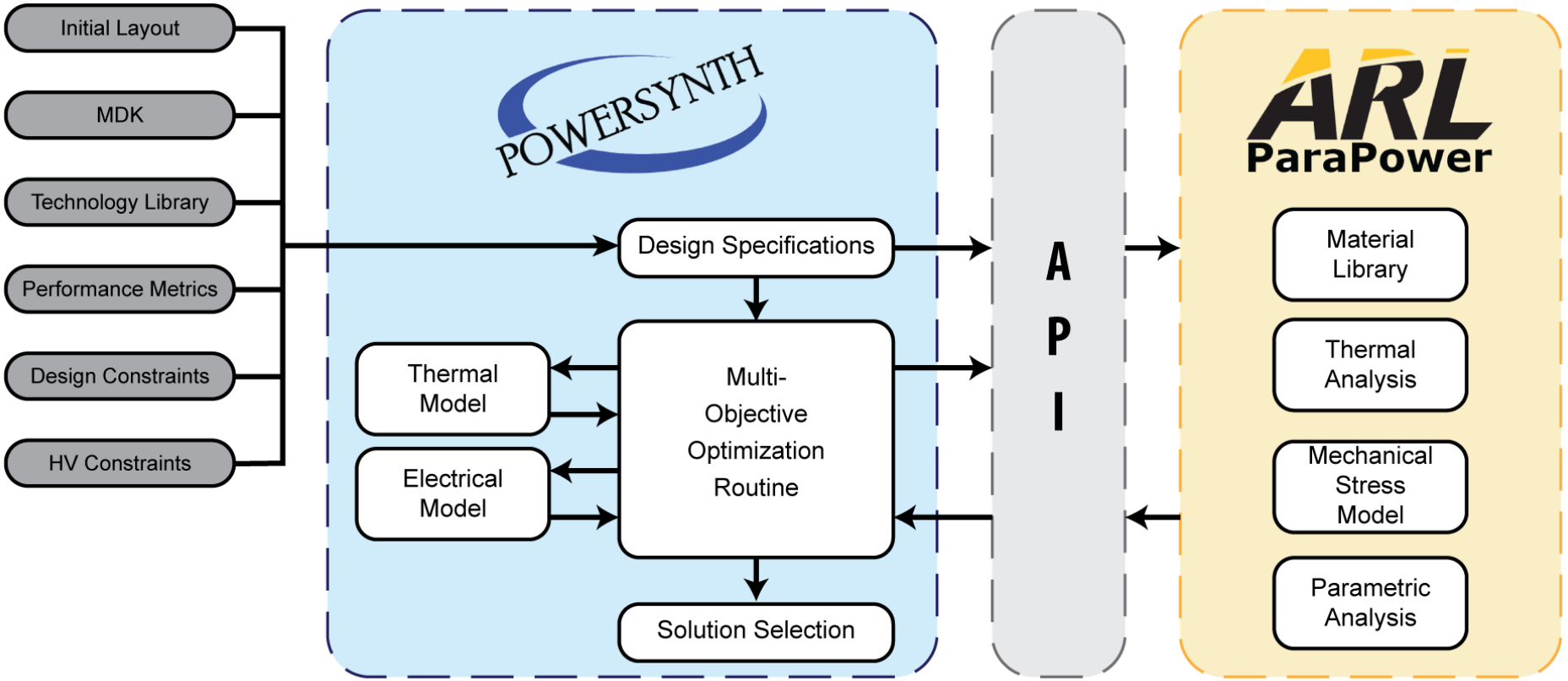






Background

PowerSynth⇄ParaPower Integration



API to leverage:

- PowerSynth layout generation and electrical parasitics extraction
- ParaPower 3D thermo-mechanical analysis
  - Fast
  - thermo-mechanical analysis
  - Parametric analysis tools & Support for phase change materials

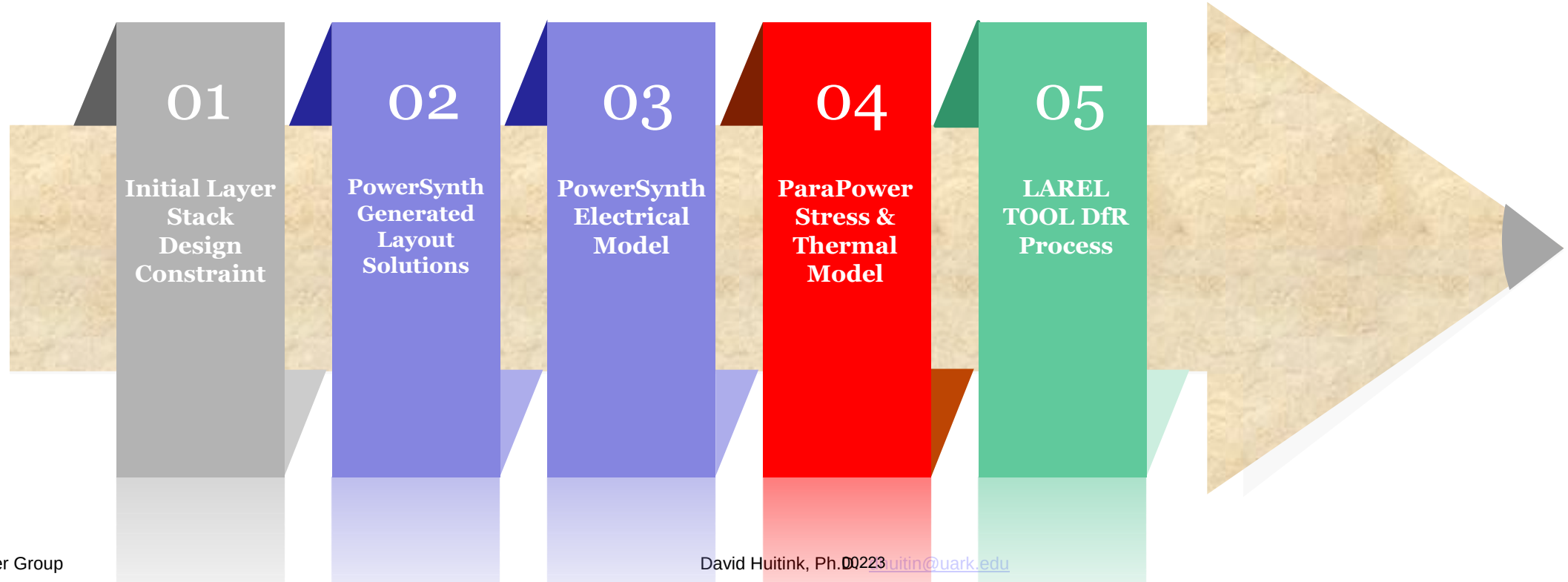
LAREL Tool

Design for Reliability (DfR) as a key strategy

- Goes beyond optimization by not only reducing stressors but also evaluating their impact on design lifespan.

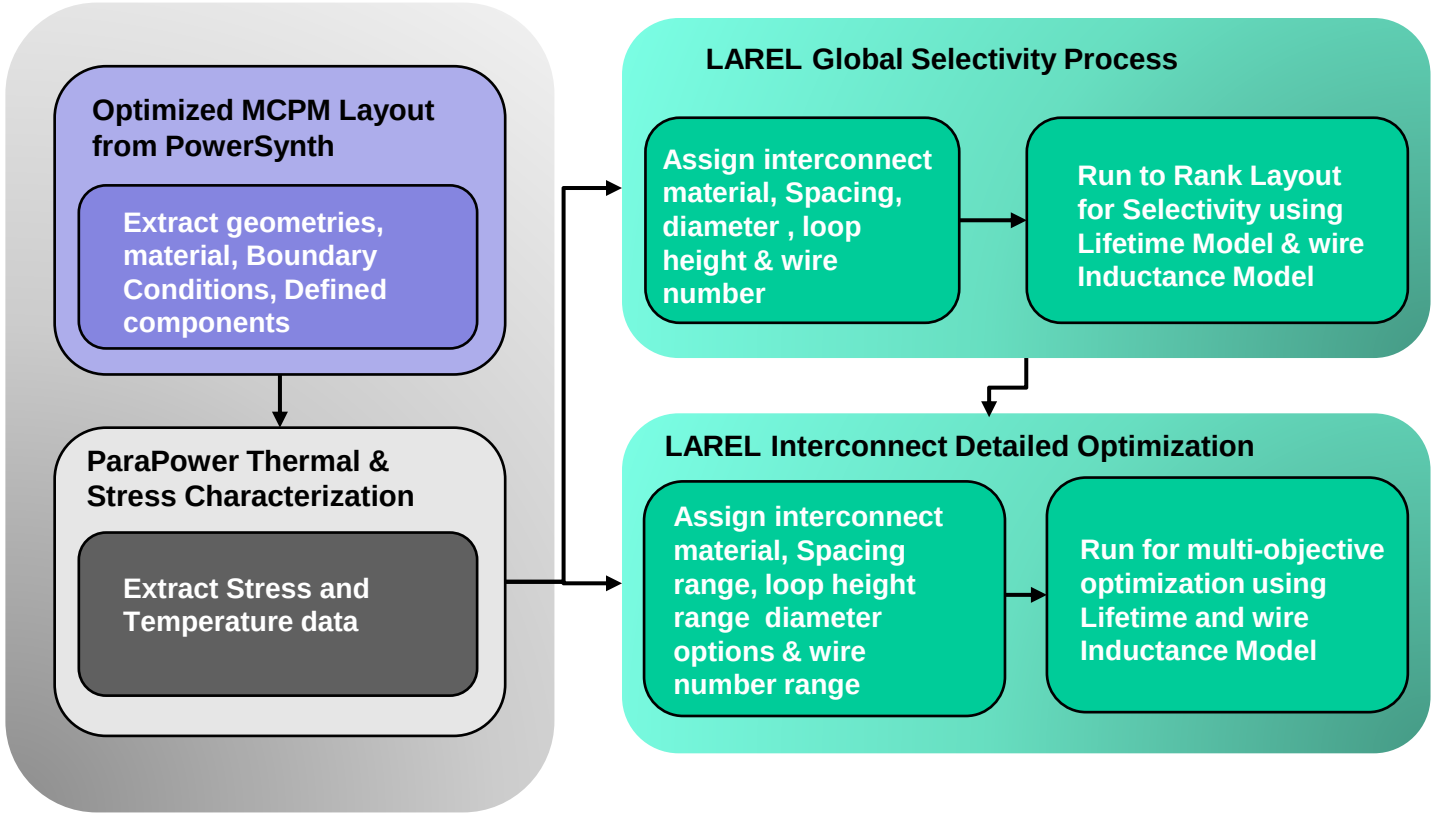
Enhancing reliability through multi-stressor analysis

- Adapts to account for interactions between multiple stresses if their severity is known.
- Provides a more comprehensive view of a device's expected lifetime.

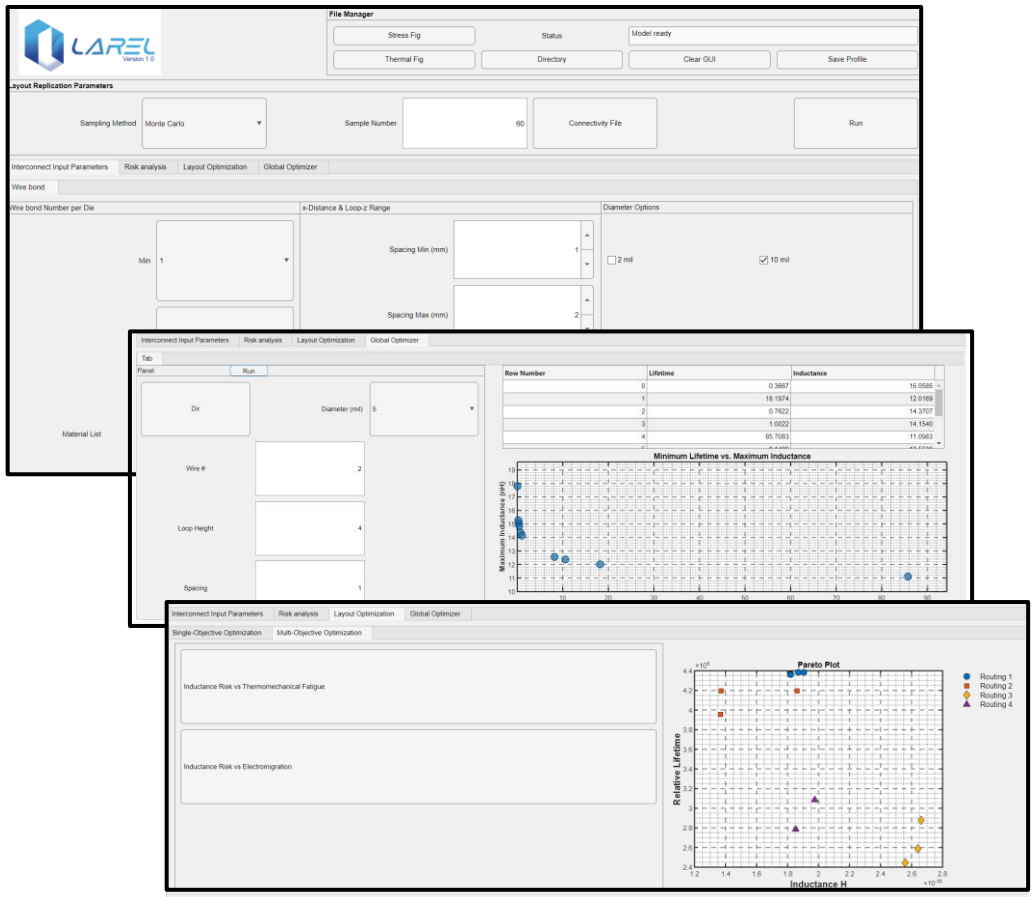


LAREL Tool Overview

- EDA Tool for Multi-chip Power Modules (MCPM) Design for Reliability
- MCPM Selectivity Process
- Detailed Multi-objective Interconnect Reliability optimization

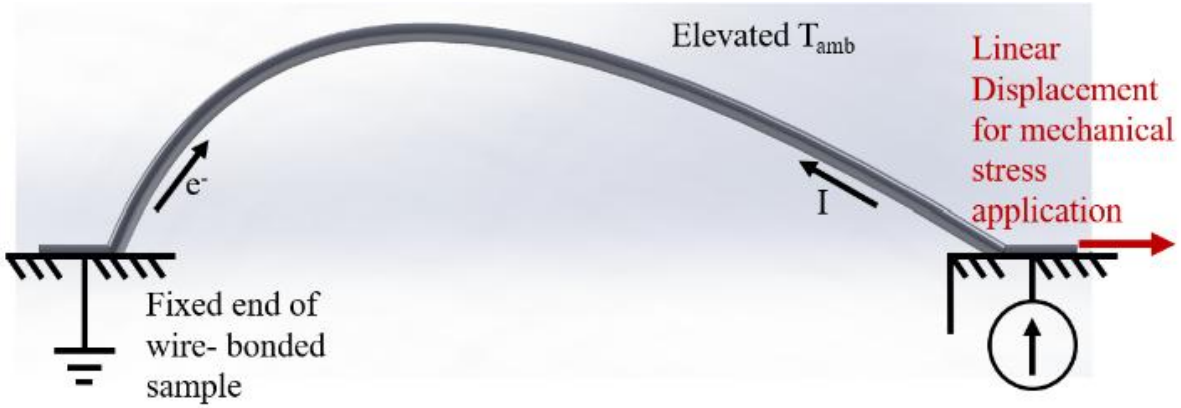


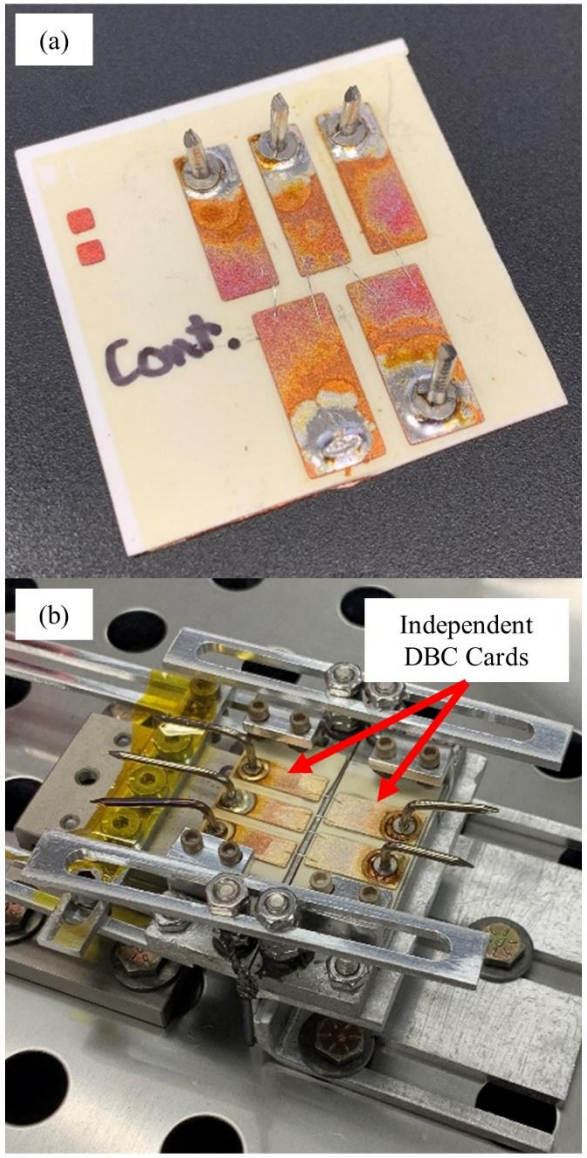
- Interconnect Lifetime models
- Pareto-front of tradeoffs
- Resulting Design Parameters

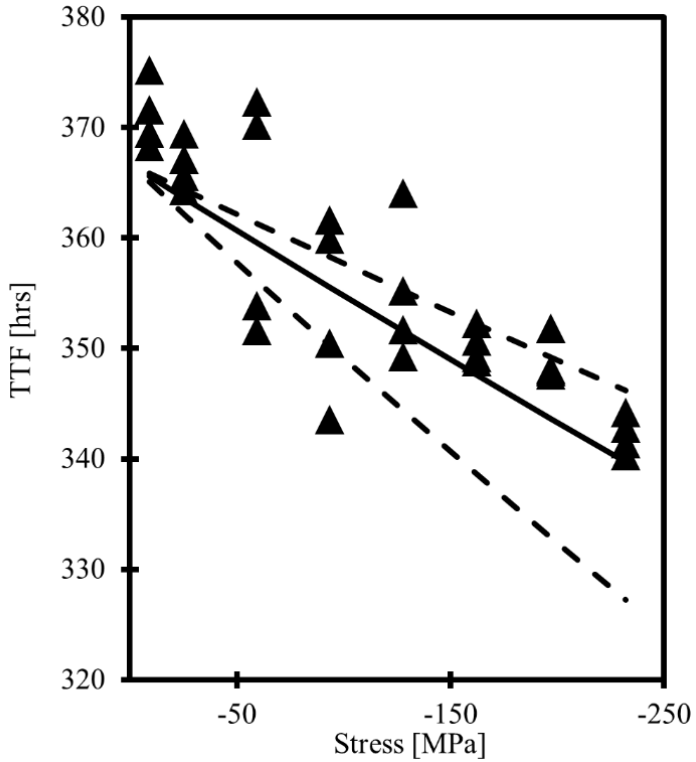


LAREL Tool– Experimental Determination of RUL

- **Al wire-bonded MCPM**
  - **Temp., current density, mechanical strain**
  - **Accelerated testing → Life Model**



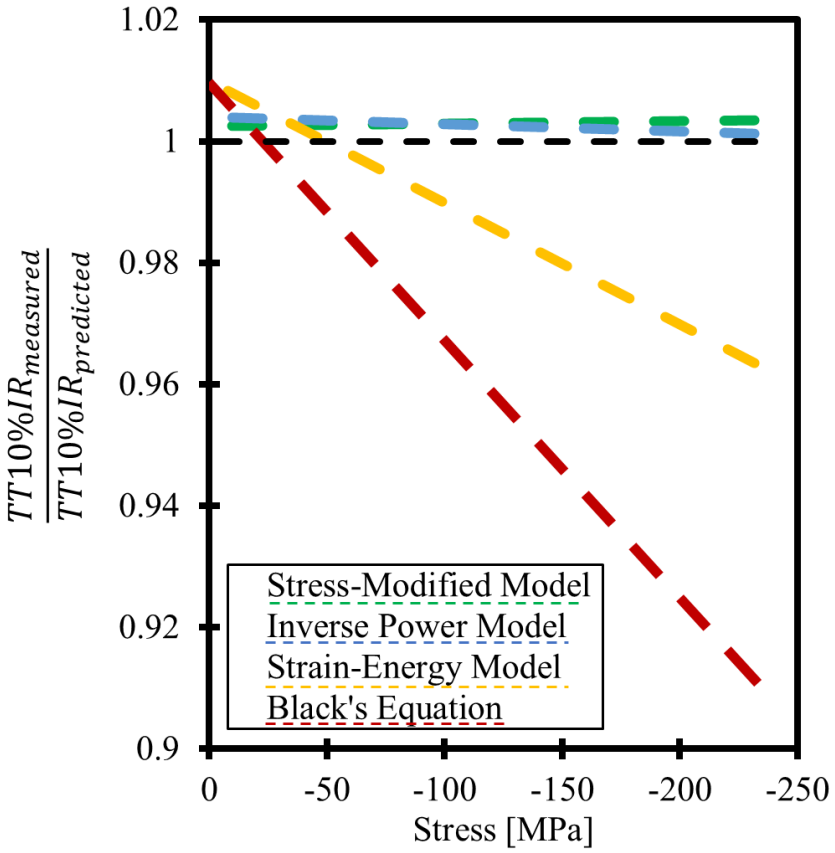




LAREL Tool– Model Determination of RUL

➢ Al wire-bonded MCPM

- **Life Model Selection & Significance**



Black's Equation:

$$TT10\%IR = \frac{A}{j^n} e^{\left(\frac{E_a}{k(T)}\right)}$$

Stress-Modified Model:

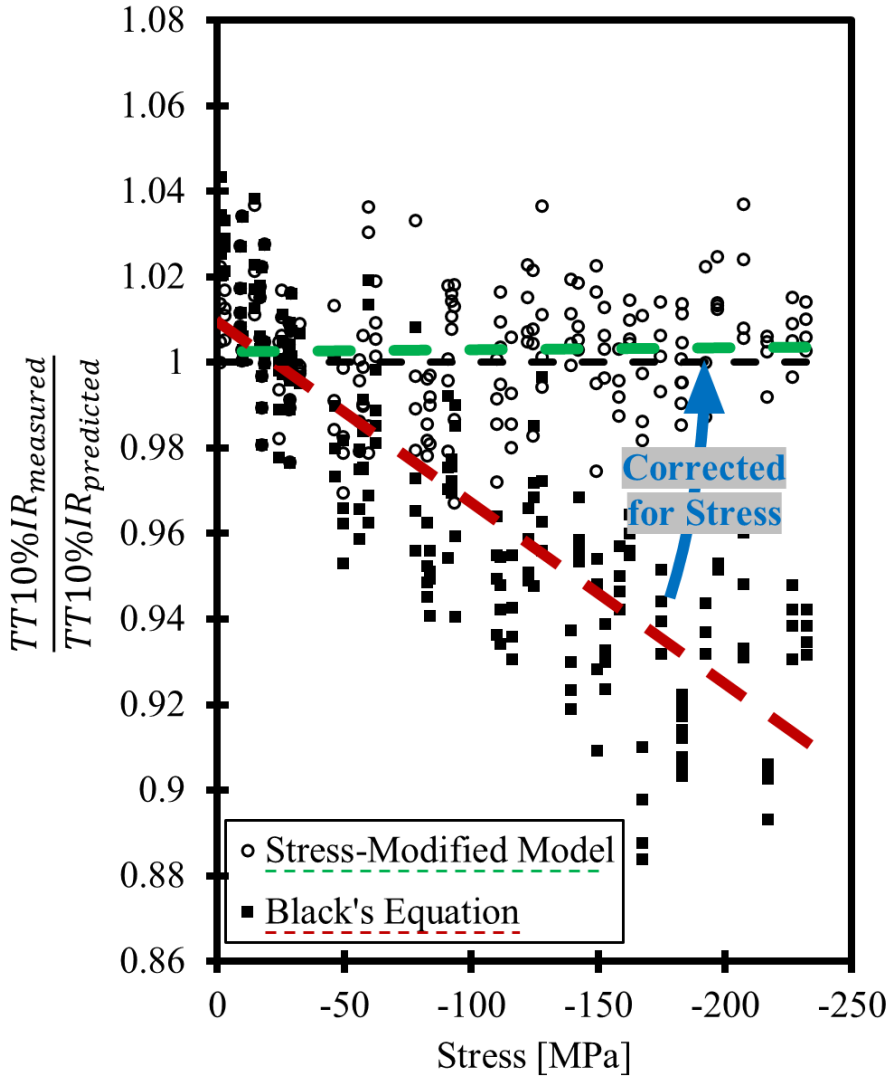
$$TT10\%IR = \frac{A}{j^n} e^{\left(\frac{E_a}{k(T)} + \gamma\sigma\right)}$$

Inverse Power Model:

$$TT10\%IR = \frac{A}{j^n(|\sigma|)^\gamma} e^{\left(\frac{E_a}{k(T)}\right)}$$

Strain-Energy Model:

$$TT10\%IR = \frac{A}{j^n} e^{\left(\frac{E_a}{k(T)} + \frac{\gamma}{U}\right)}$$



Case Study A: Fixed-Sized Layouts

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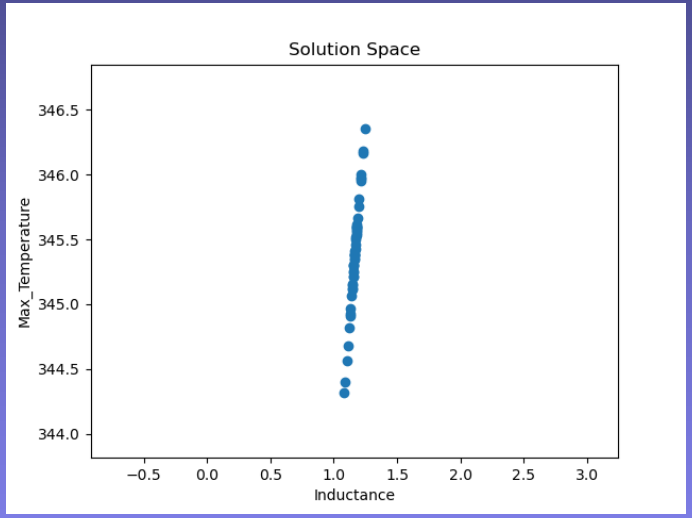
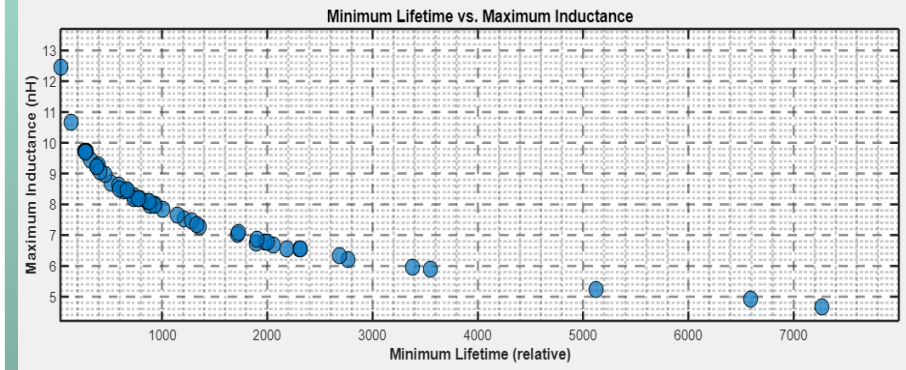
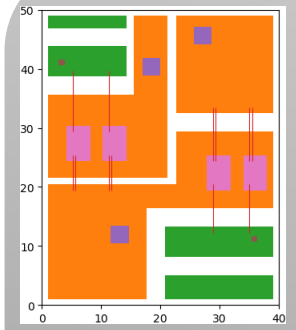
PowerSynth Layout Solutions



LAREL Layout Ranking

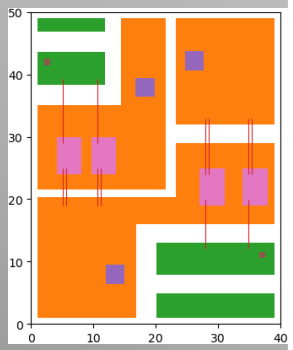
Row Number	Lifetime	Inductance
0	321.5687	9.4536
1	3.5527e+03	5.8886
2	2.7650e+03	6.2095
3	1.7161e+03	7.0231
4	2.0576e+03	6.6763

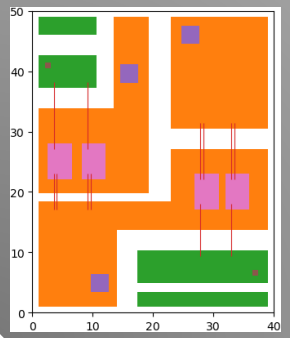




Layout A

Layout B





Layout C

Integration of PowerSynth for Multi-Physics Reliability Analysis

- **Design Import:** Enables seamless transition of layouts from PowerSynth for reliability assessment.
- **Global Selectivity Stage:** Ranks layouts based on key performance metrics for detailed reliability evaluation.
- **Optimized Workflow:** Ensures an efficient, structured approach to multi-physics reliability modeling.

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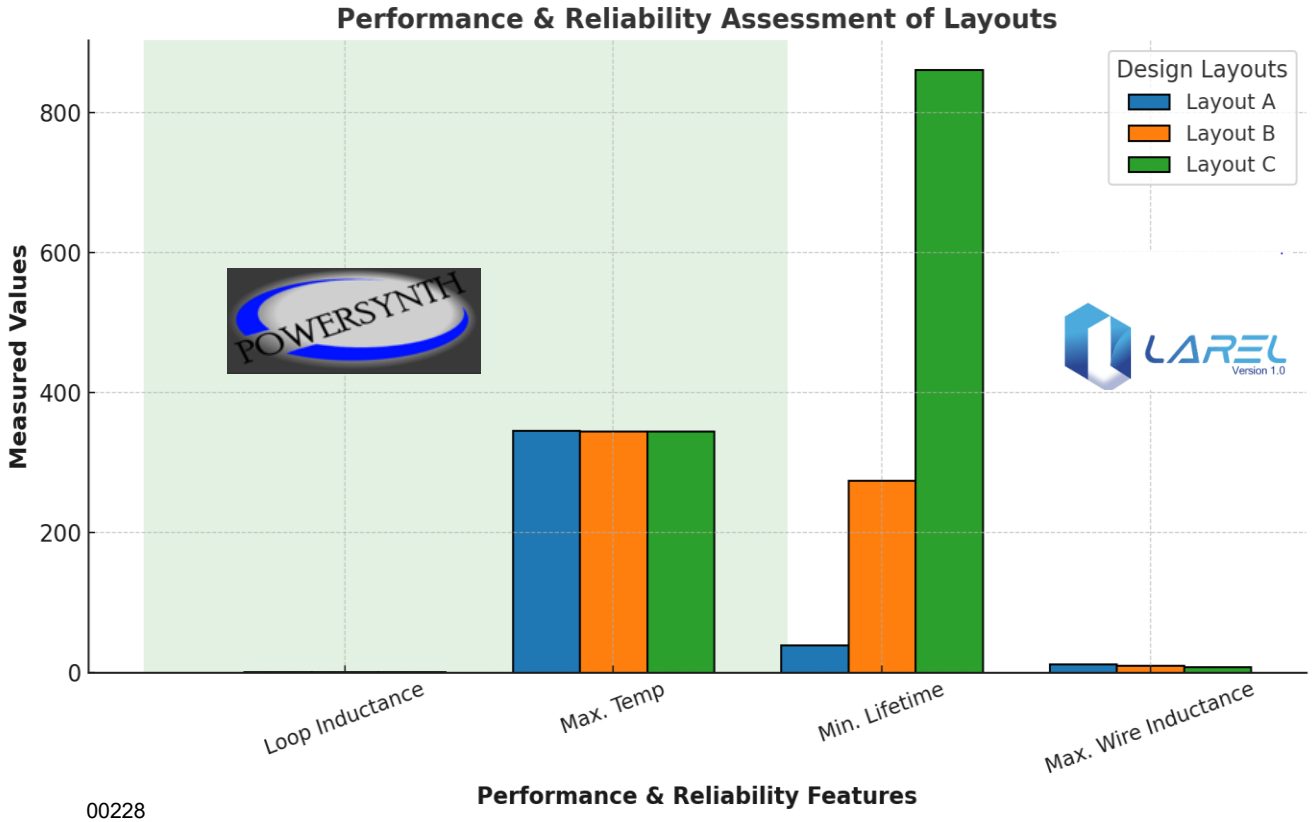
Case Study A: Fixed-Sized Layouts

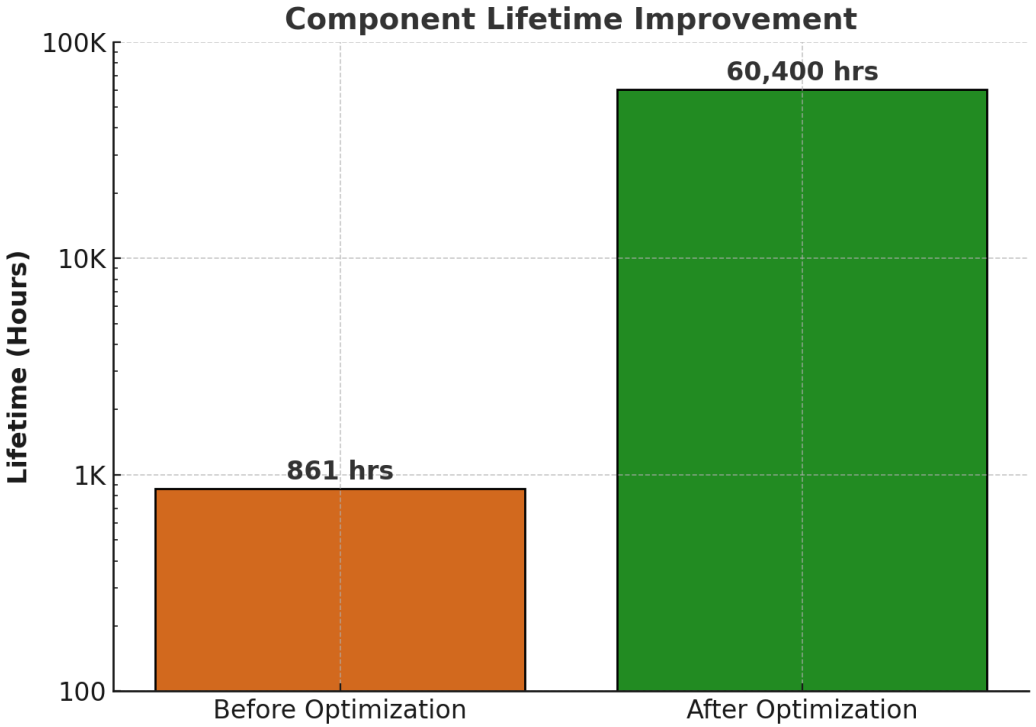
Layout Label	Loop Inductance, nH	Max. Temp, K	Min. Lifetime, Hrs	Max. Wire Inductance , nH
A	1.18	345.61	39.57	12.45
B	1.16	345.30	274.62	9.68
C	1.21	344.82	861.35	8.09

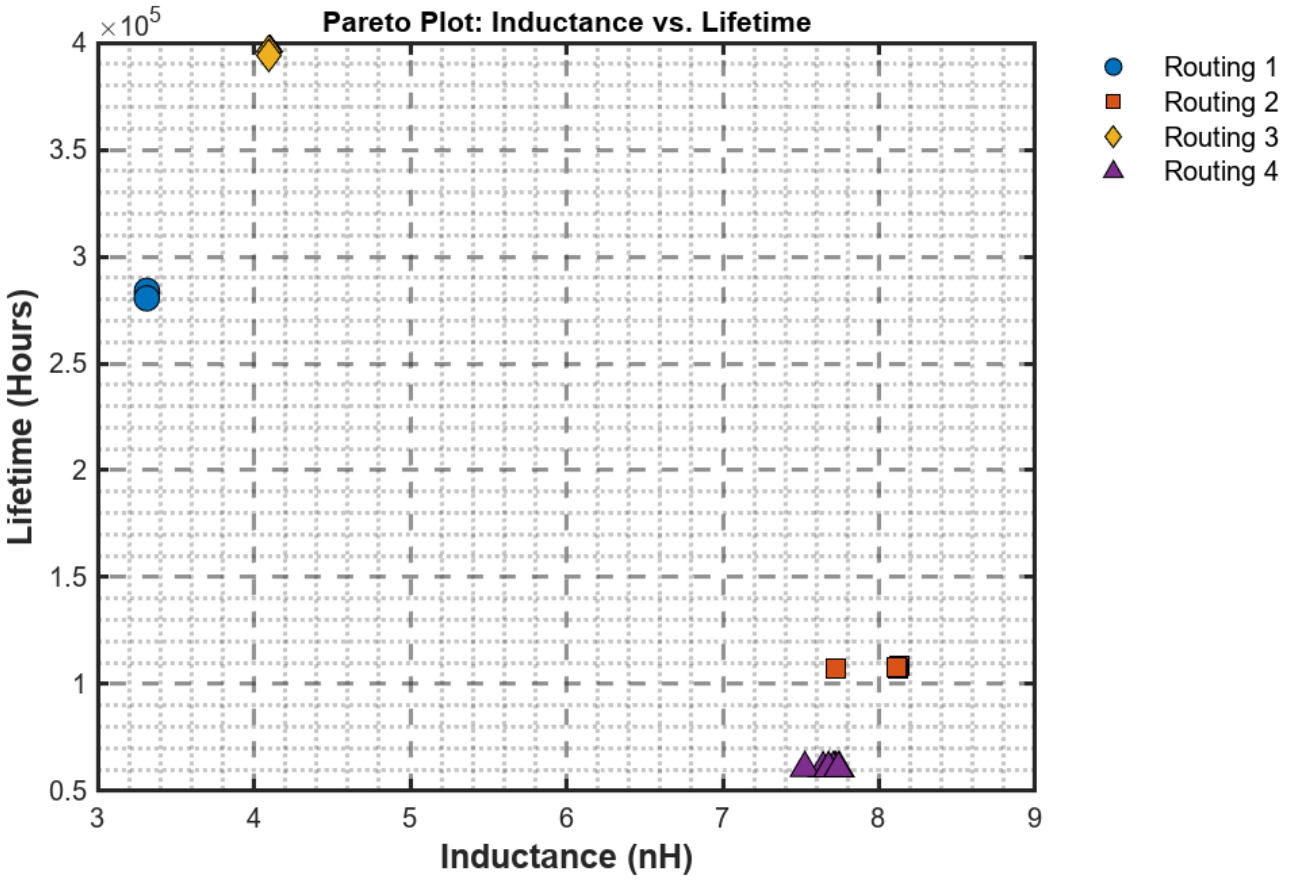
Enhanced Decision-Making with LAREL Tool

- **Fixed-Sized Layout Challenge:** Small performance differences make selecting the optimal layout difficult.
- **Advanced Assessment Features:** LAREL tool highlights variations, simplifying decision-making.
- **Improved Clarity:** Clearly visualizes key differences for a more informed layout selection.



Case Study A: Fixed-Sized Layouts





Multi-Objective Optimization for Reliability Enhancement

- **Identifying Weak Links:** Pareto plot highlights potential weak points in routing (connectivity).
- **Balanced Optimization:** Achieves fair electrical performance improvements while boosting reliability.
- **Significant Lifetime Gains:** An improvement close to 2 orders of magnitude, leading to a major increase in system reliability.

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Case Study B: Variable-Sized Layouts

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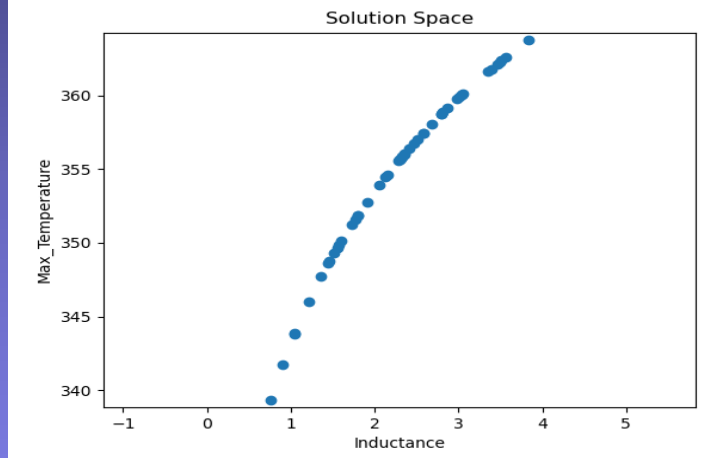
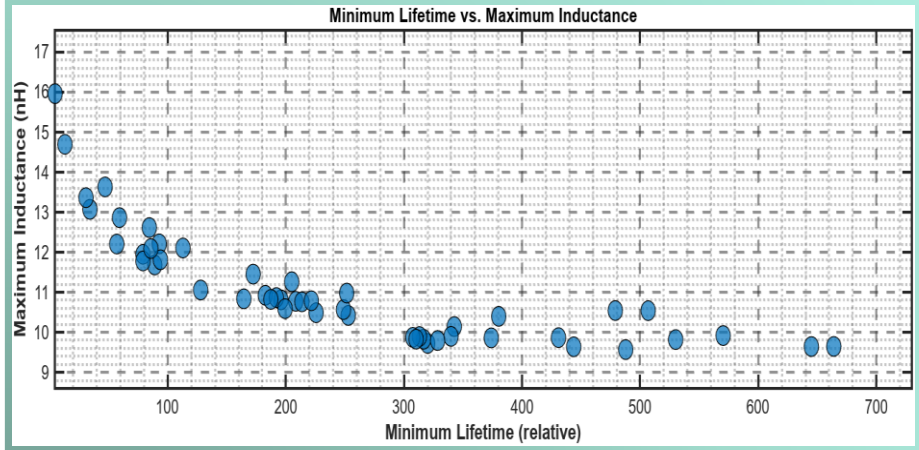
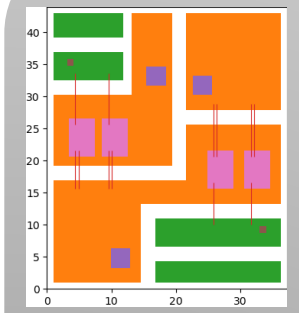
PowerSynth Layout Solutions



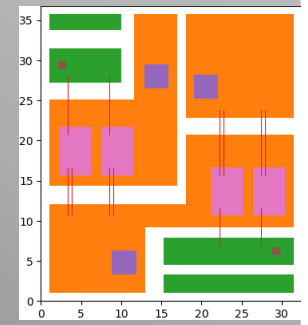
LAREL Layout Ranking

Row Number	Lifetime	Inductance
40	1.4600e+04	11.9881
41	4.4034e+04	6.3860
42	2.3643e+04	9.1522
43	6.8684e+04	7.4170
44	6.3758e+04	7.4194
45	2.3095e+04	6.6793

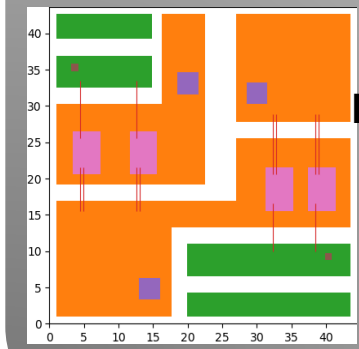




Layout A
45x40



Layout B
35x35



Layout C
45 x 45

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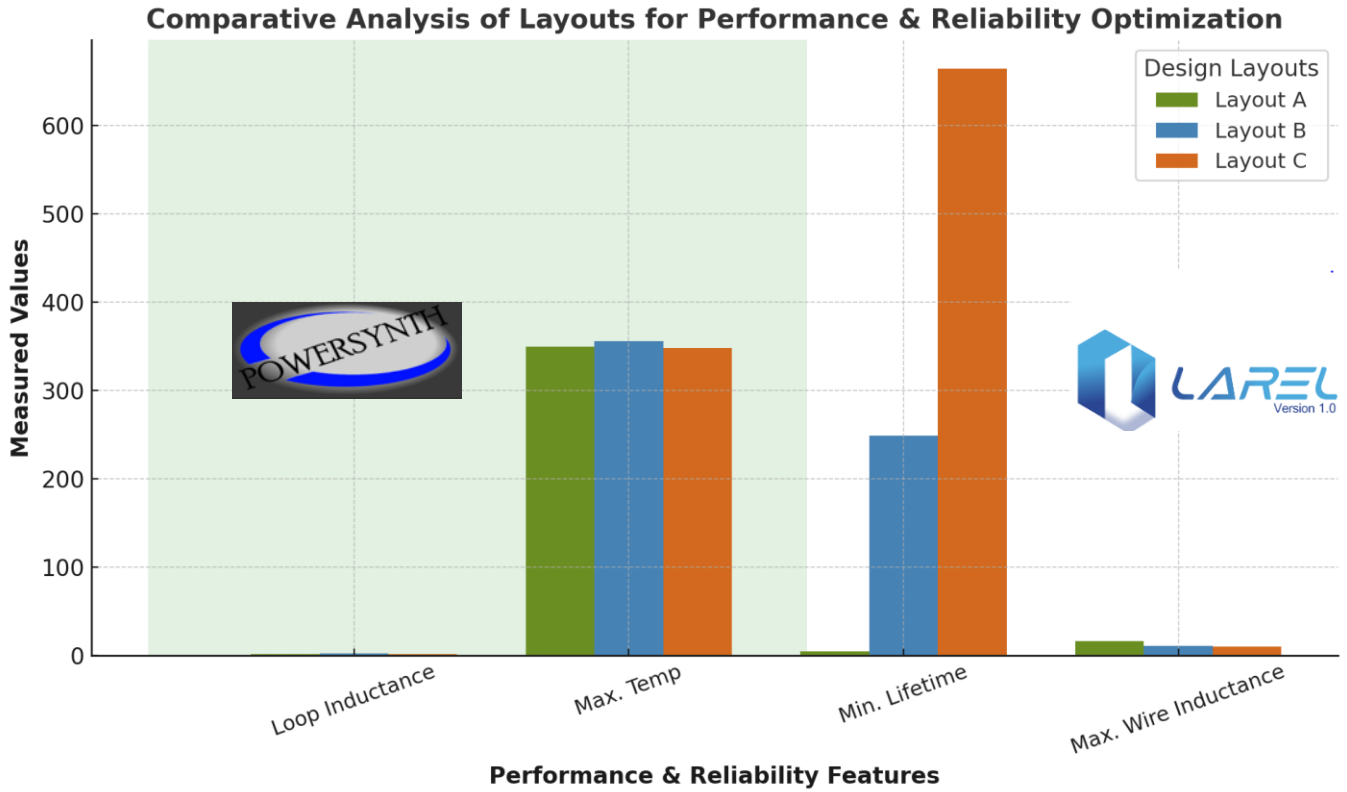
Case Study-B

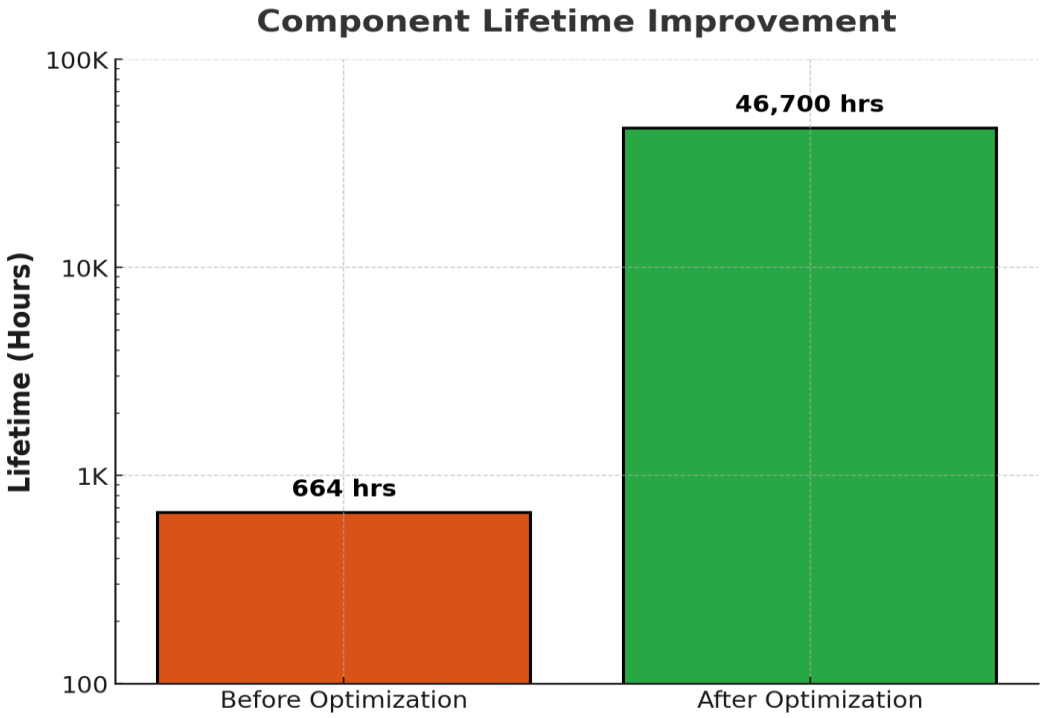
Layouts	Loop Inductance, nH	Max. Temp, K	Min. Lifetime, Hrs	Max. Wire Inductance, nH
A	1.57	349.31	4.6	15.9
B	2.33	355.89	248.78	10.57
C	1.36	347.70	663.91	9.64

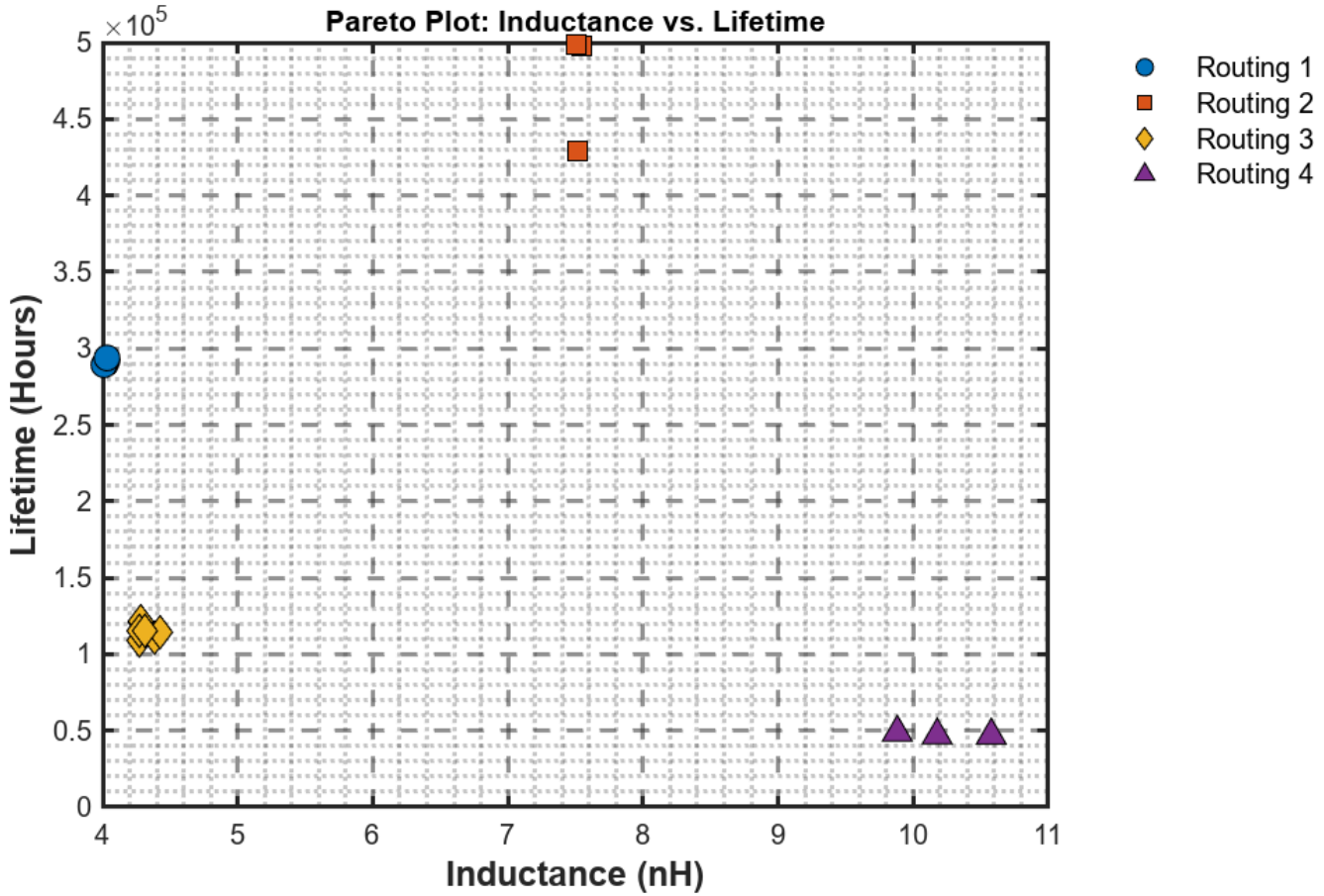
Enhanced Decision-Making with LAREL Tool

- **Challenge:** Variable-sized layouts show minimal differences, making design selection difficult.
- **Limited Decision Basis:** Small performance variations aren't enough to confidently choose a design.
- **LAREL Tool Advantage:** Brings clarity by highlighting key distinctions, enabling better-informed design choices



Case Study-B





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Conclusions & Outlook

- Higher power density increases interactions between multiple stressors, impacting system performance.
- Multi-mechanism failures shorten component lifetime compared to single-stress expectations.
- Considering multi-stress interactions is essential for designing next-generation reliable devices.
- LAREL and PowerSynth help differentiate designs, improving decision-making and reliability.

Acknowledgements:

- University of Arkansas
  - College of Engineering
  - Engineering Research Center
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  - NSF
- DEPSCoR
  - ONR

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Q&A

Thank you!

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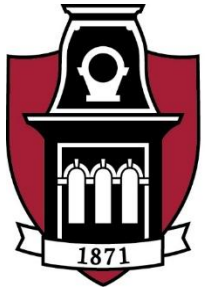

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