21ST INTERNATIONAL CONFERENCE & EXHIBITION ON DEVICE PACKAGING
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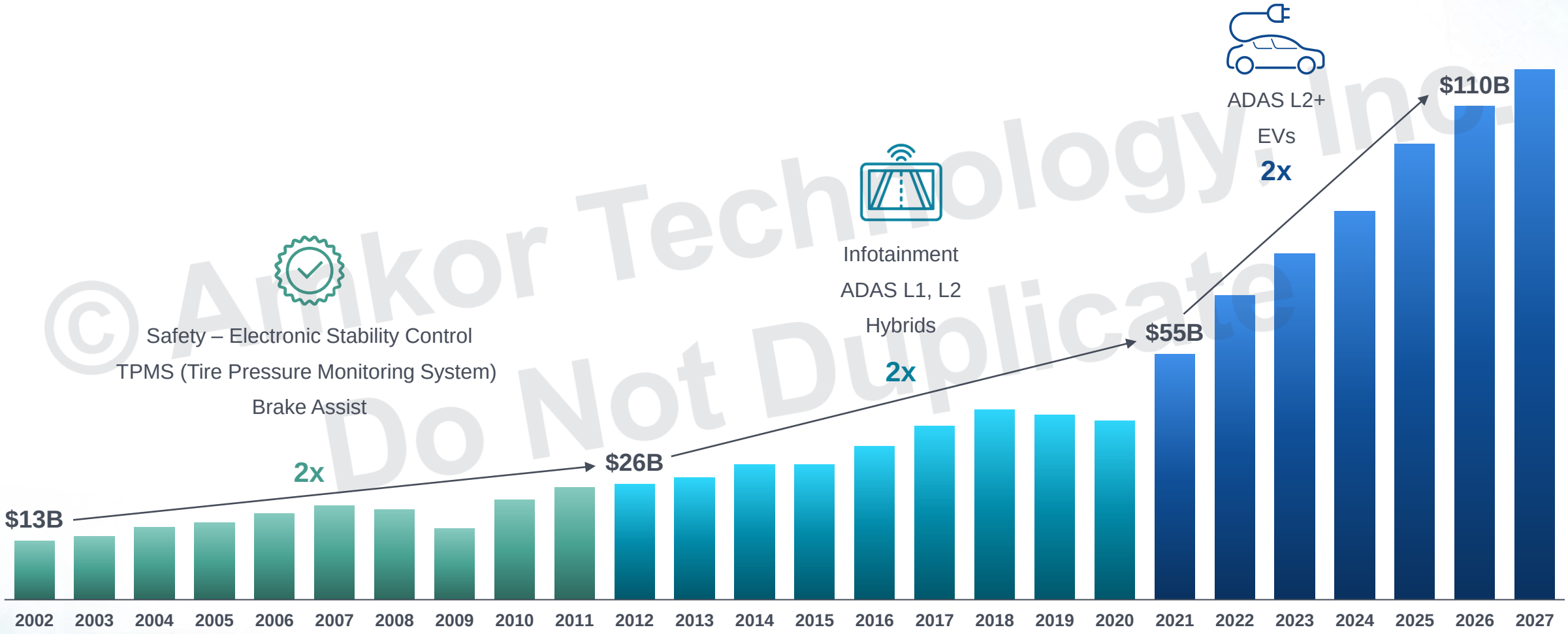
Firewalls in Semiconductor Assembly: Ensuring Quality & Reliability in Automotive Applications

Prasad Dhond l VP, Wirebond
BGA & MLF® Products

Agenda

1. Automotive Semiconductor Trends
2. Automotive Packaging Trends
3. Automotive Wirebond Packaging
4. Common Packaging Assembly Defects
5. Third Optical AOI
6. O/S Testing
7. Strip & Unit Traceability

Automotive Semiconductor Long-Term Opportunity

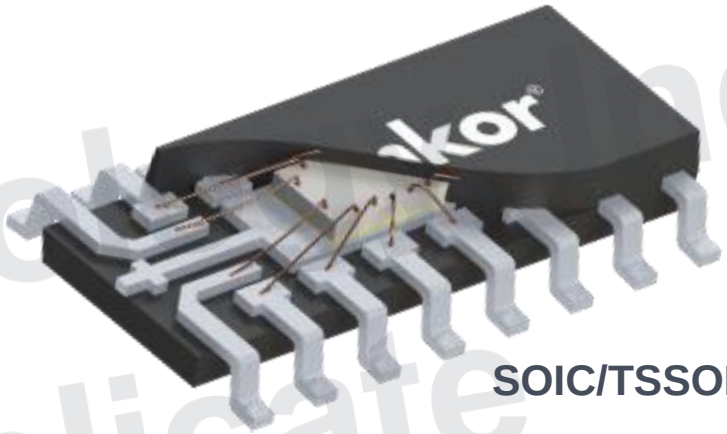


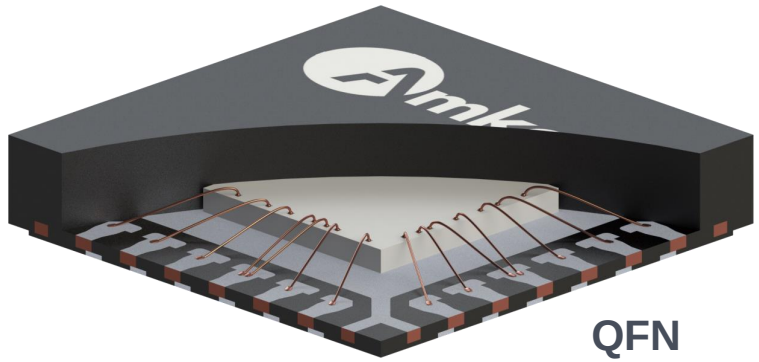
Source: Gartner

Automotive Packaging

Accelerated Adoption of Advanced Packaging

Analog	Sensors	MCU, GPU	RF/mmWave Transceivers	Processor + Memory
Power	Overmolded	LQFP	fcCSP	SiP
Dual LF	Exposed Die	CABGA	WLFO	
MLF®	Cavity	FCBGA		
	Optical Sensor			





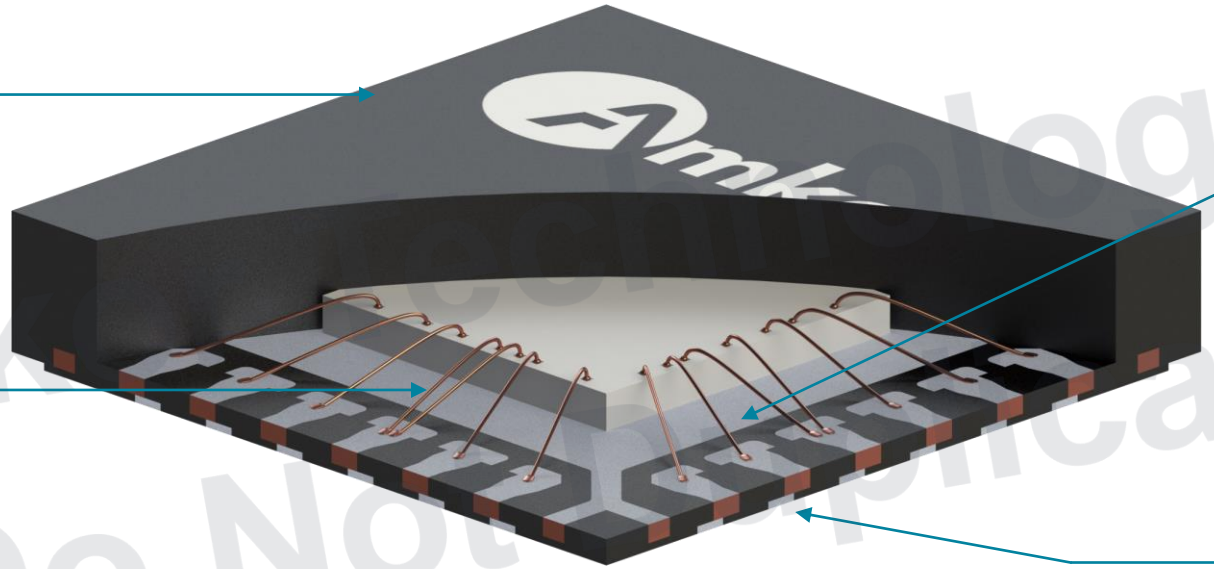
Assembly Materials for QFN Automotive Reliability

Mold Compound

- Optimized sulphur content

Copper Wire

- Robust reliability at higher temperatures
- Cost-effective



Die Attach

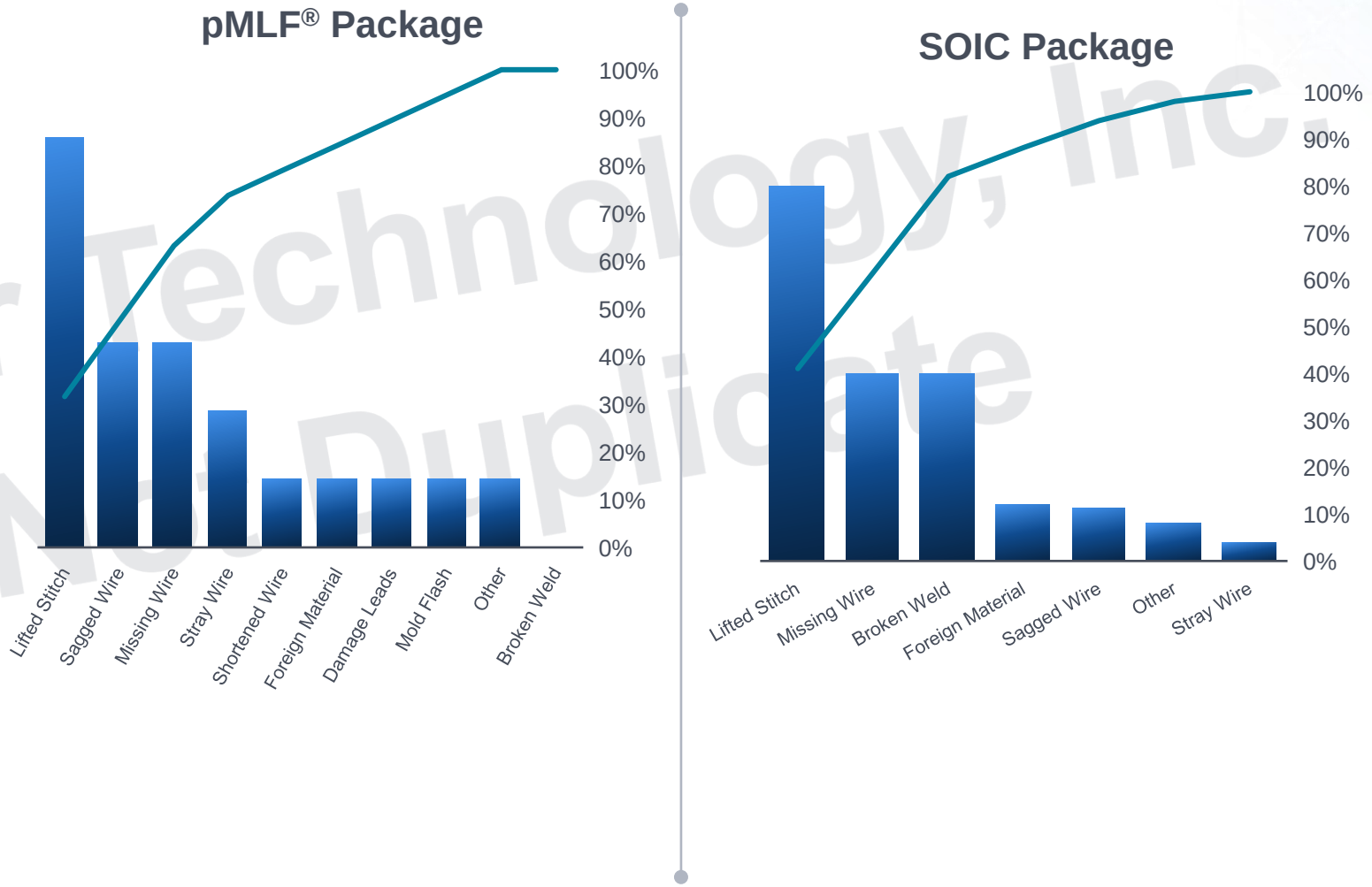
- Optimized C_{TE}

Leadframe

- Roughened for better adhesion
- Wettable flanks for solder fillet formation

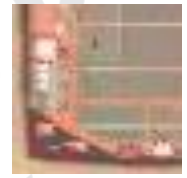
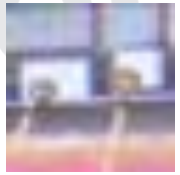
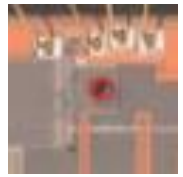
Common Package Assembly Defects

- Common Production Defects
  - Wire-related
  - Foreign Material
  - Substrate/Leadframe
  - Mold
- Most common wire-related defects
  - Lifted bonds
  - Sagged wire
  - Missing wire



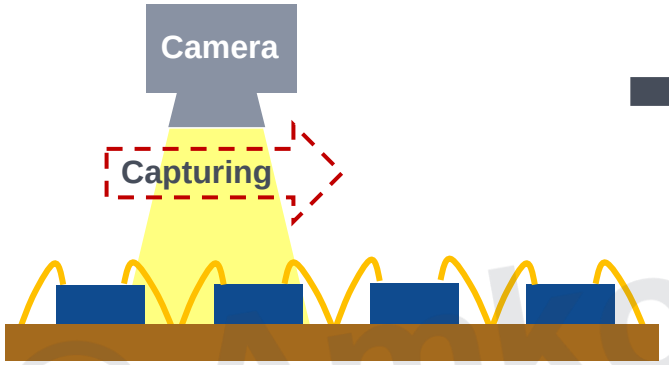
Automotive Package Process Flow

AOI 3rd Optical Inspection

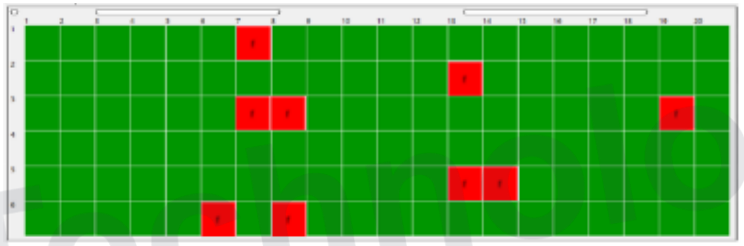
	Manual	Automated
Chipped Die		
Broken Wire at Heel		
Off-centered Bond		
Contamination		

AOI 3rd Optical Process

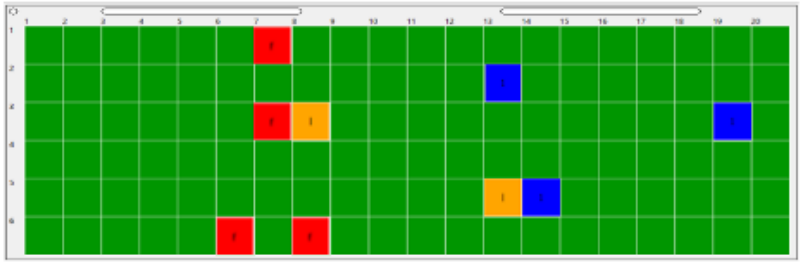
Camera Captures Image



Generate Defect Map



Reject Validation by Operator



- Good
- Valid machine reject
- Reject by the machine but not reject in actual (over-rejection)
- Valid reject but operator changed reject call-out.

Revised Map is Stored

Good

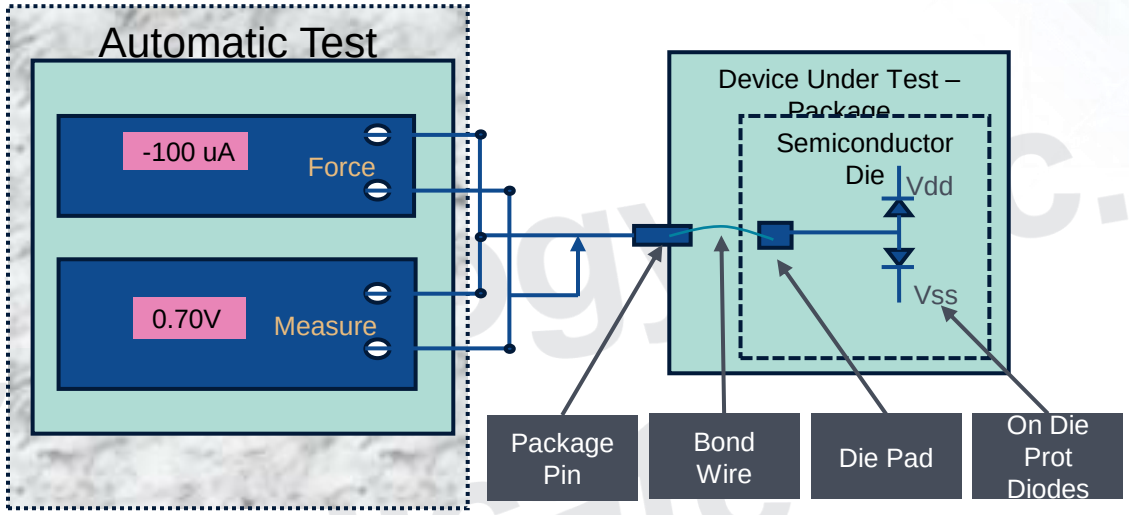
Note: Other colors are rejected per bin code/color

3rd Optical AOI Advantages

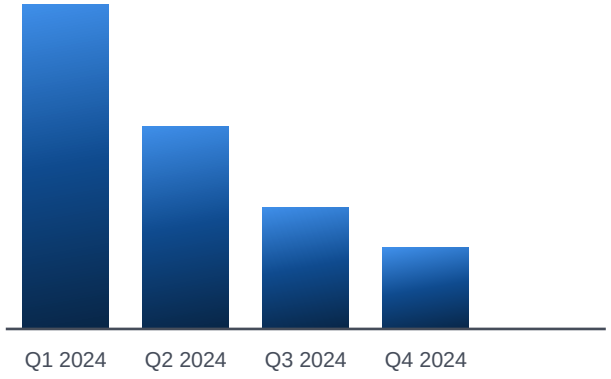
Items	3rd Opt Manual (Manual Inspection)	3rd Opt AOI (Automatic Inspection)	Advantage	
			Manual 3rd Opt	AOI
Reject traceability	No documented map	Electronic Strip Map		✓
Detection	Manual detection	Automatic detection		✓
	Subjective (operator preference)	Objective (program reference)		
Reject Analysis	Manual reject unit retention for further analysis	Database through reject images and eMAP		✓
Data Analytics	Manual yield computation	Automatic yield computation		✓
Material Handling	Semi auto	Full auto		✓
Frequency/Sample size	Sampling/Lot	100% every lot		✓
Use Cases	All	Simple wiring	✓	

Package Pin Opens and Shorts Test

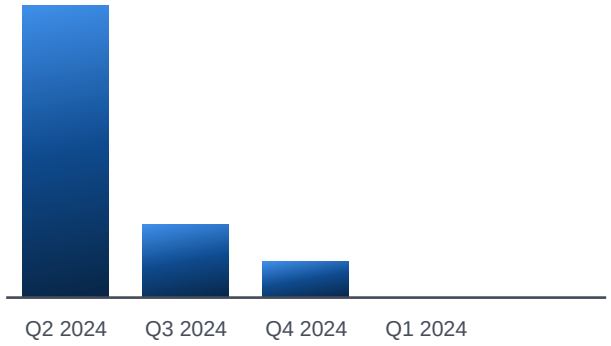
- AOI has limitations
  - Complex, dense wiring
  - Post-mold wire sweep
- OS testing is an additional screen
  - Stop defective parts from leaving the assembly site
  - Immediately identify and sequester any maverick lots
  - Provide immediate feedback to the errant assembly process such as die attach, wirebonding or molding for improvement
  - Especially effective if final test is performed at another site



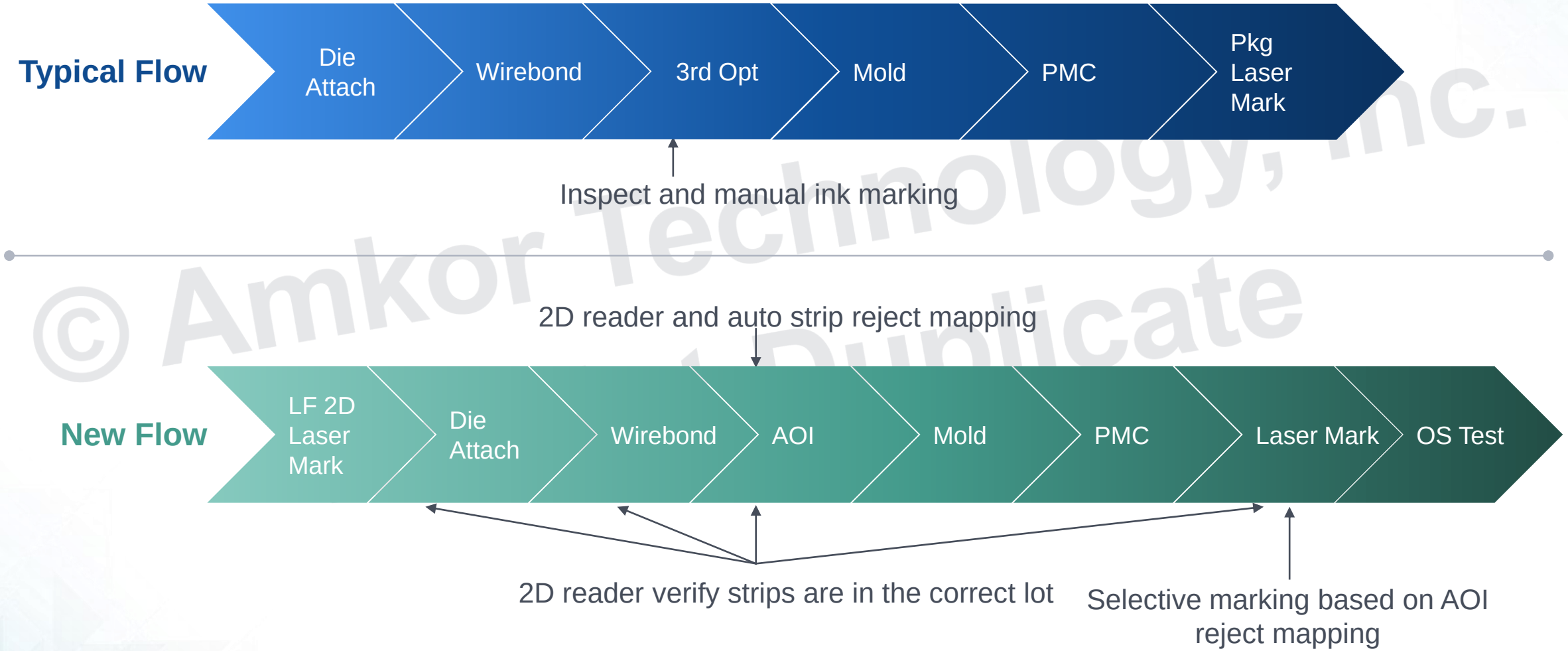
pMLF® Lifted Stitch Defects Trend



SOIC Lifted Stitch Defects Trend

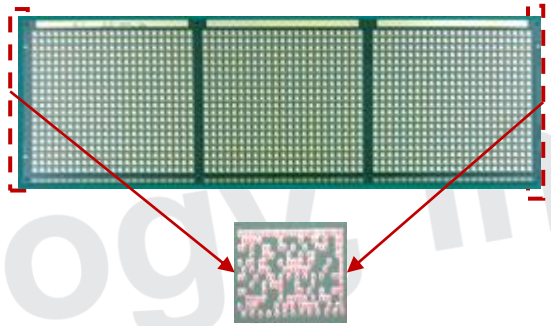


AOI & OS Reject Management

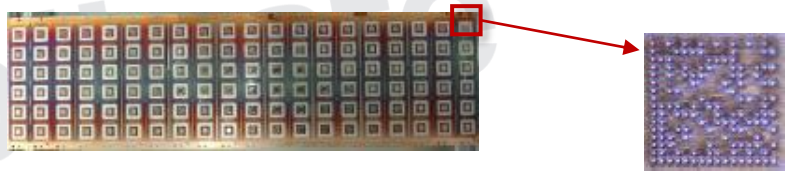


2D Strip Marking

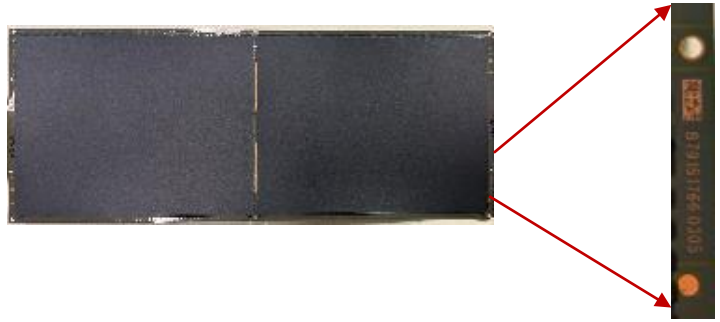
- Prevents strip level product mixing post-mold
- Logging of process failures at each assembly station
- Generate individual output map for each lot per assembly process
- Enable data for unit/die traceability
- Automate unit rejection to improve lot handling



Strip 2D Code Marking

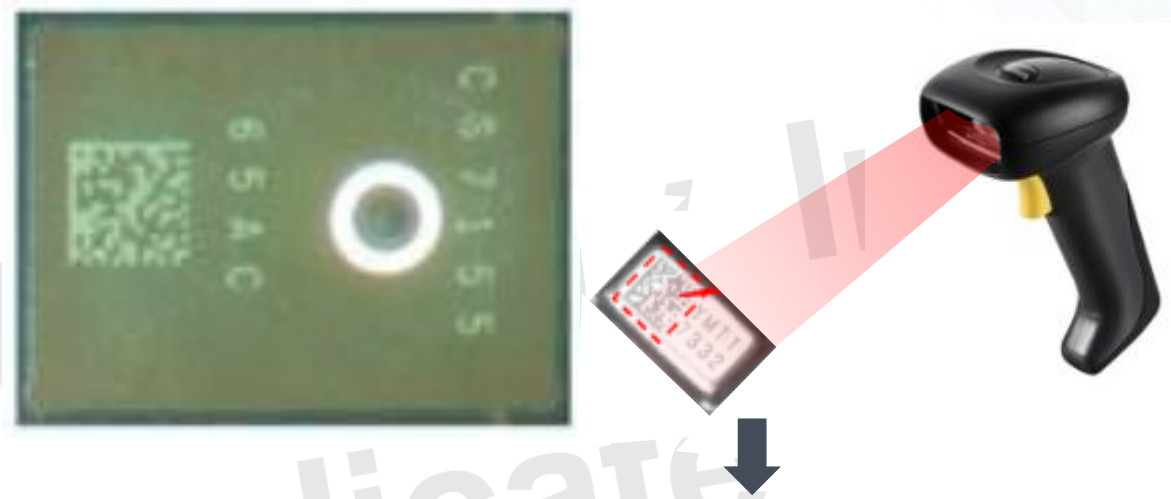


Leadframe 2D Code Marking



2D Unit Marking

- 2D code on the unit
- Track location of unit on wafer and strip
- Access to data for engineering problem solving or unit failures
  - Lot transaction history, BOM, yield and defect breakdown



- Data analytics for engineering problem solving
  - Strip map and wafer map/die location
  - Transaction history
  - Bill of materials
  - Yield and defect breakdown
  - eSPC and eStandroll

Use Case – Detecting Failure Commonality

Field Failure 1

Field Failure 2

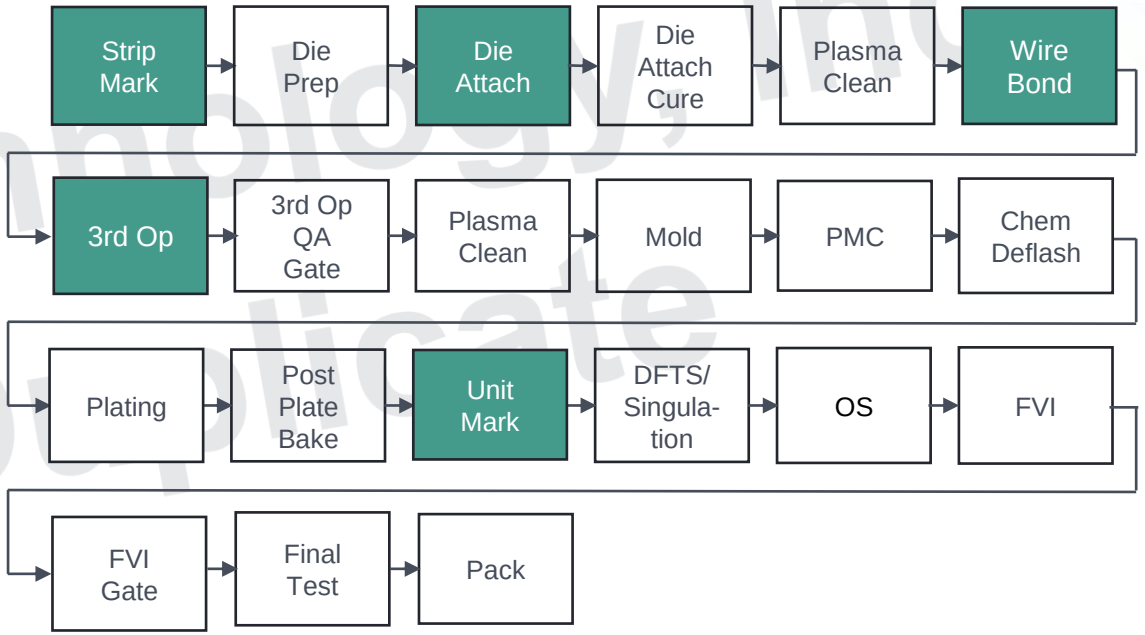
	Die		Substrate	
	Wafer ID	XY Position	Substrate ID	XY Position
Unit 1	12345	6,3	98765	1,1

Both failed units are from same wafer

	Die		Substrate	
	Wafer ID	XY Position	Substrate ID	XY Position
Unit 2	12345	12,7	78251	5,2

Current State of Traceability

- 2D strip marking provides the basis for unit traceability and commonality studies
- At die attach process wafer map + die position information is combined with strip map + unit position
- Drive strip mapping of defective units at WB
  - Units that encounter NSOP, NSOL and SHTL will report those defects to eMES which will log these in the strip map
- FOL equipment are connected and are updating the strip map with unit level assembly information
- At unit laser marking process each unit is marked with a 2D code that ties the unit to the strip map + unit information
- Additional assembly information can be stored from all connected processes



Automotive Firewall Suite

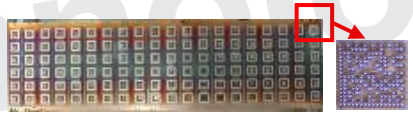
AOI 3rd Optical Inspection

- Replace manual inspection
- Detect wirebond defects

Open/Shorts Testing

- Detect wire defects from mold
- Immediate feedback on maverick lots

Strip Mark



- Prevent strip mixing
- Support reject mapping

Unit Mark

- Mark small as well as large packages
- Troubleshoot defective units

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