# Key Considerations for Enhancing the Partial Discharge Capability of High Voltage Power Semiconductor Modules

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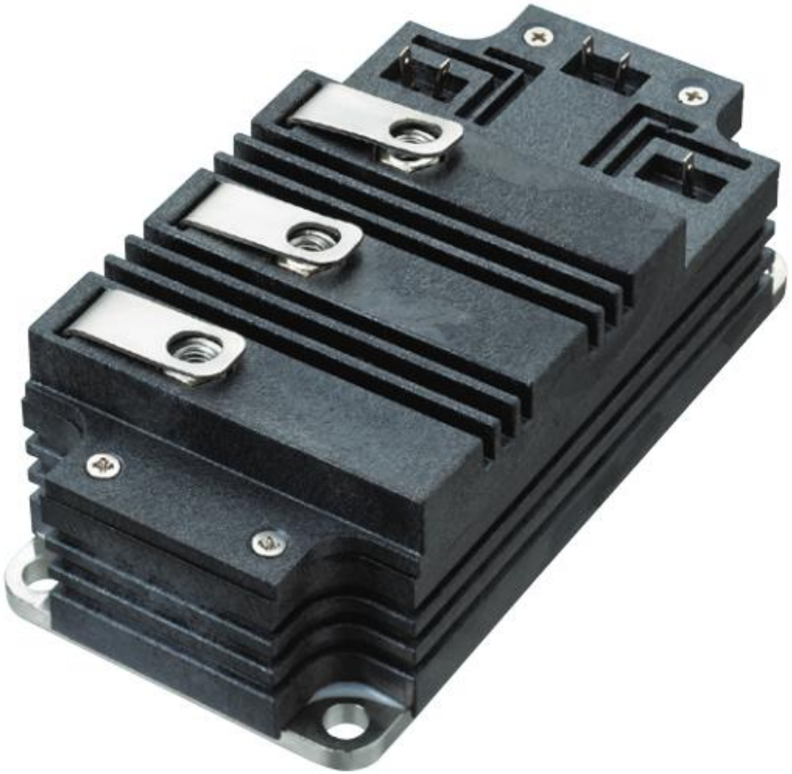
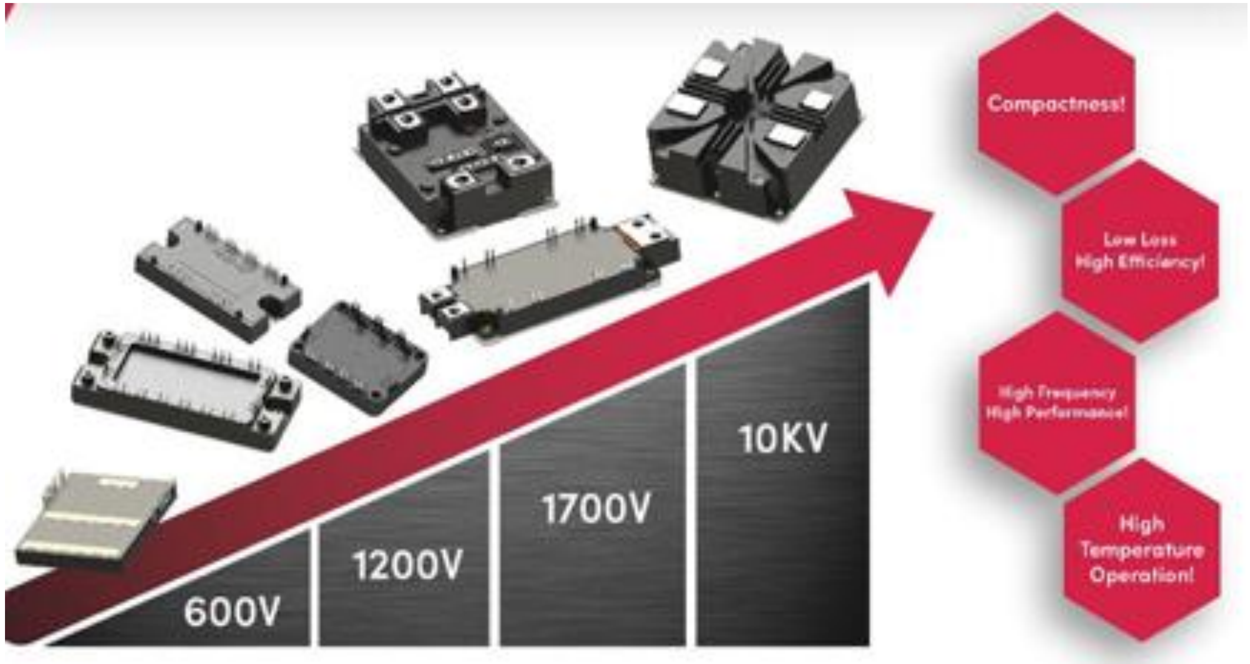
# Overview

- **Partial Discharge**
  - Defining partial discharge and how to minimize its occurrence
- **Material Selection:**
  - Use of high-quality insulation materials with high dielectric strength to withstand high voltage stress and minimize discharge.
- **Design of Insulation System:**
  - Optimizing the geometry and thickness of insulation layers to reduce the likelihood of partial discharge formation.



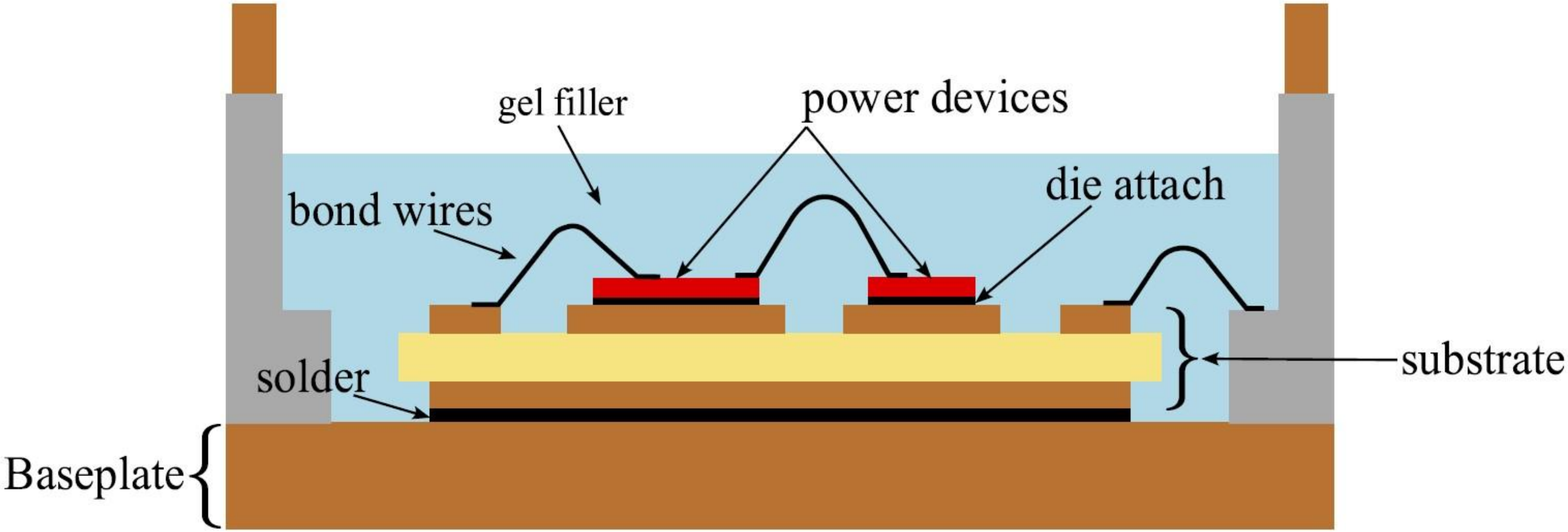
# Benefit and Challenges of High Voltage Semiconductor Power Modules

- What are the benefits of utilizing HV (High-Voltage) power modules?
  - System efficiency through reduction of power losses and energy savings
    - Reduction in size of inverters or power system
    - Use of HV WBG (wide-bandgap) devices enables use in high frequency and high temperature applications.



- What are the design and manufacturing challenges of HV power modules?
  - Increasing partial discharge capability from electrical fields produced by HV.
  - Reduction and balance of power loop inductance when utilizing MCMs(multi-chip modules)
  - Reduction and balance of gate loop inductance when utilizing MCMs(multi-chip modules)

# Standard Power Semiconductor Module



# Definition and Significance of Partial Discharge

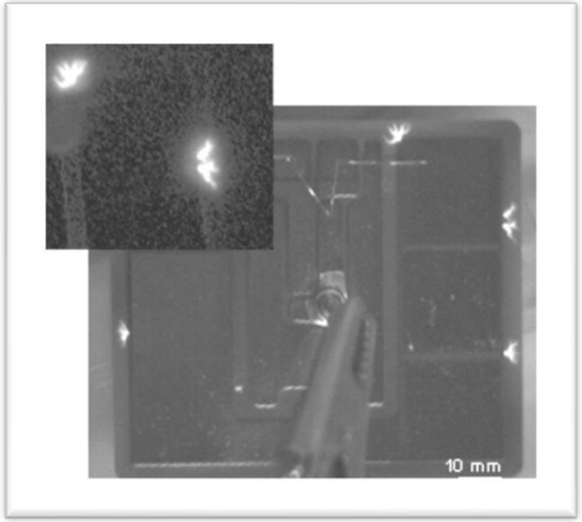
*What is partial discharge (PD)?*

Localized dielectric breakdown when the electric field strength exceeds that of the material’s dielectric strength

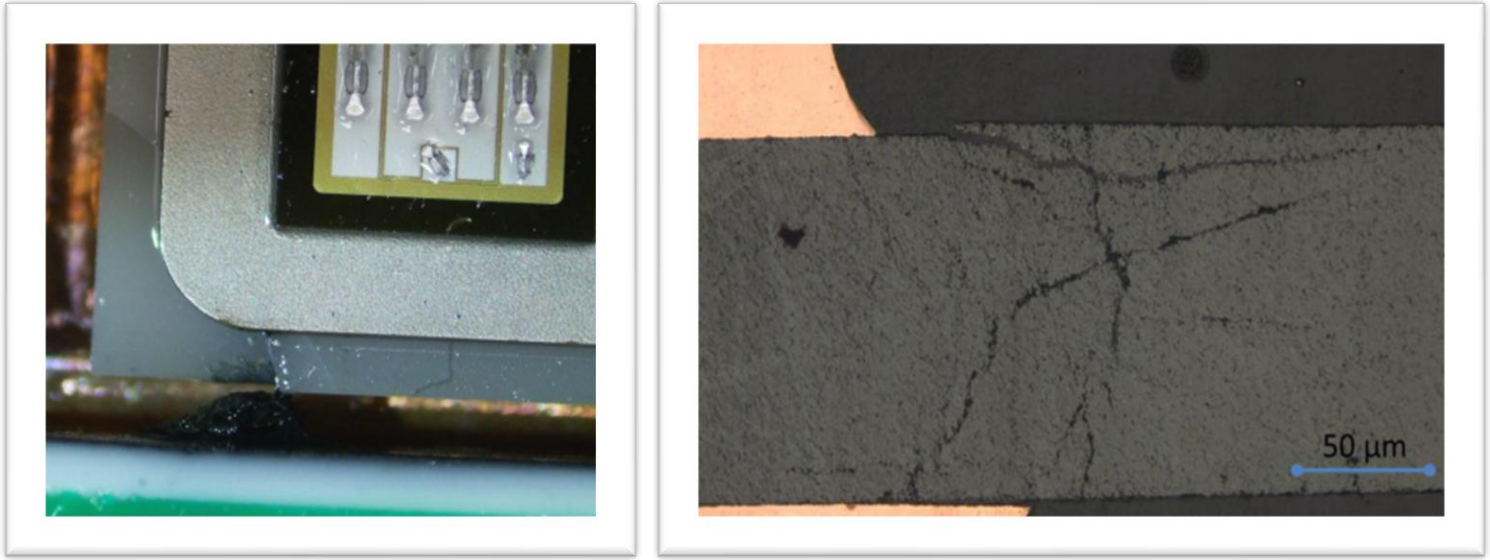
  - Partial discharge inception voltage (PDIV) is the operating voltage at which PD occurs

- Repeated partial discharge (PD) degrades the material in which it occurs and can lead to device failure within the module

Active PD Events



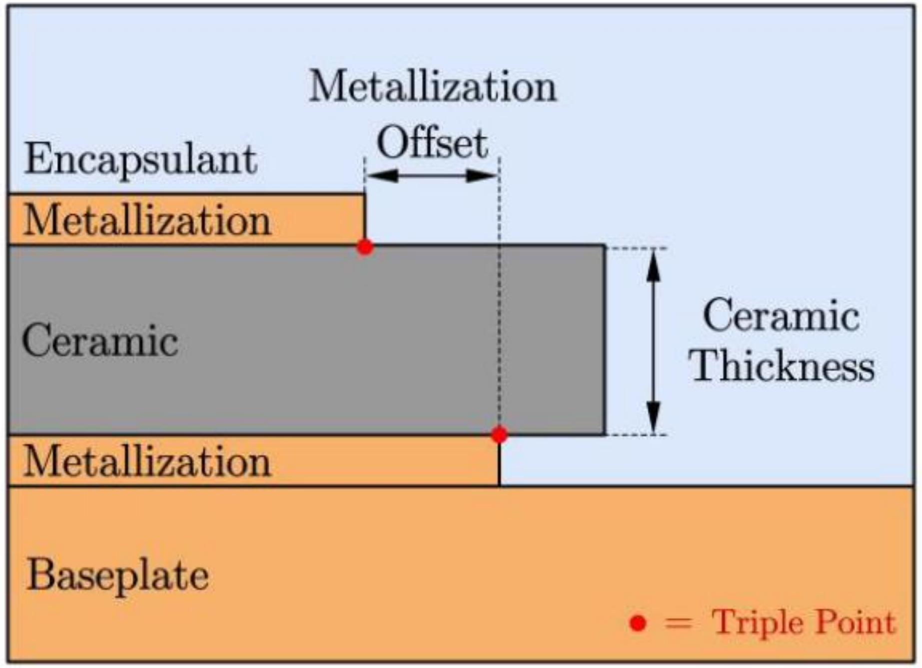
Result of PD Events

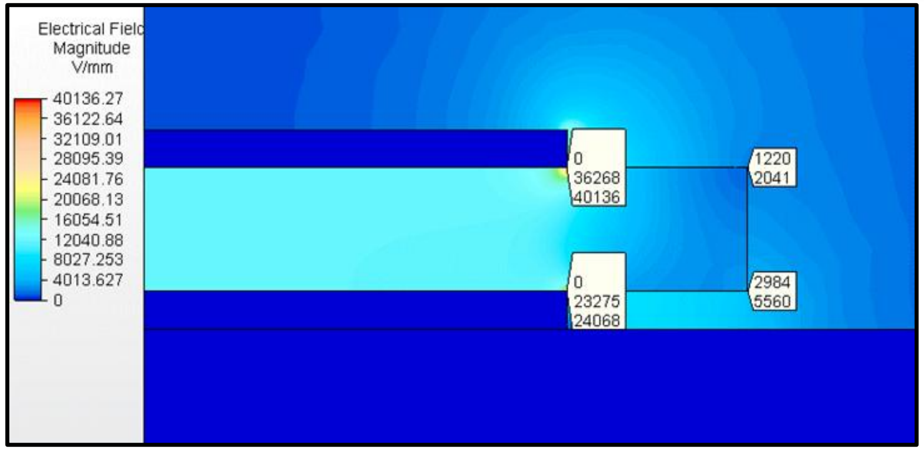


# Occurrence of Partial Discharge

- PD most frequently occurs at the triple point junction and within voids
- The triple point junction is where the ceramic substrate, metallization, and gel meet.
  - *Electric field is significantly enhanced at the triple point*
- Voids can be those within the gel, ceramic, or in the lamination between ceramic and its metallization
- PD frequency increases with operating temperature, voltage amplitude, and operating frequency

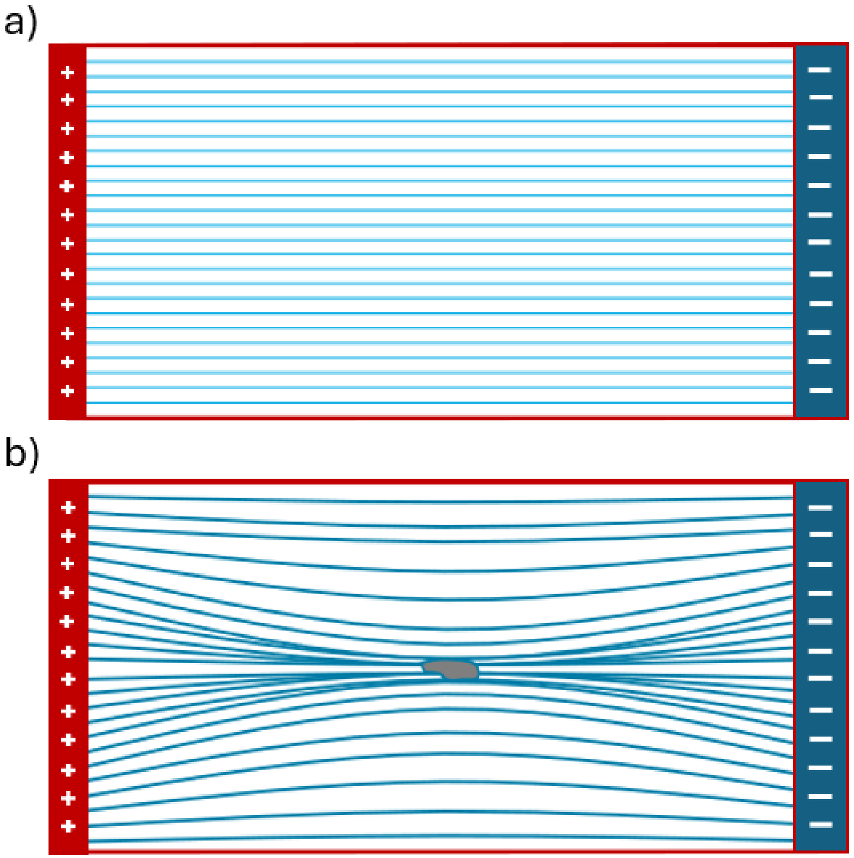
*PD Frequency* $\propto$ *Temperature, Frequency, Voltage*



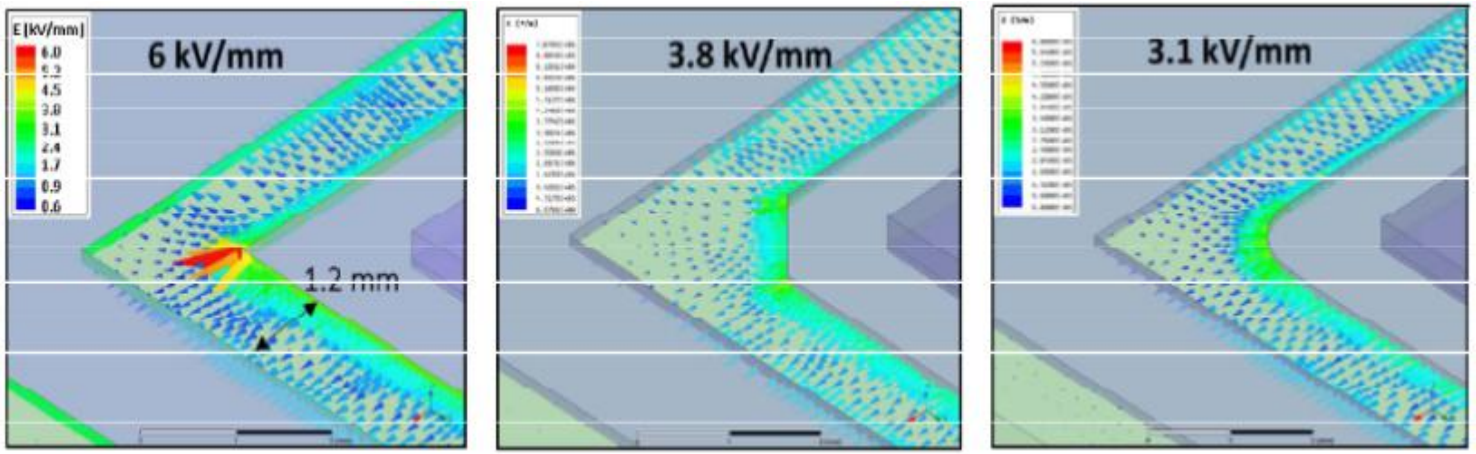


# Electric Field Concentration

- Concentration of equipotential electric field lines occurs at:
  - Voids
  - Non-uniform metal edges
  - Sharp corners

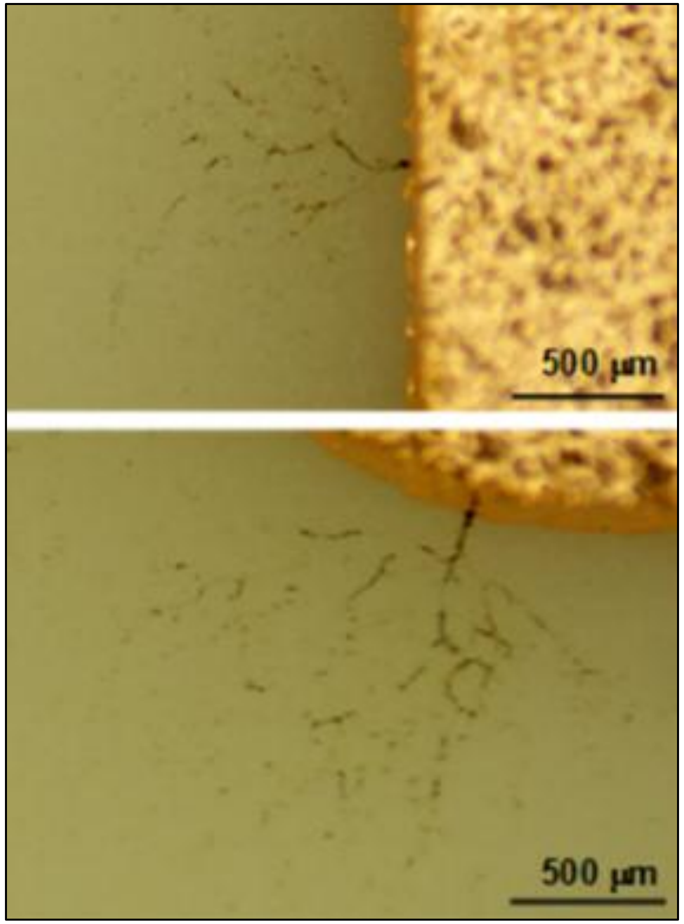


*Lower dielectric strength of void media concentrates E-field*



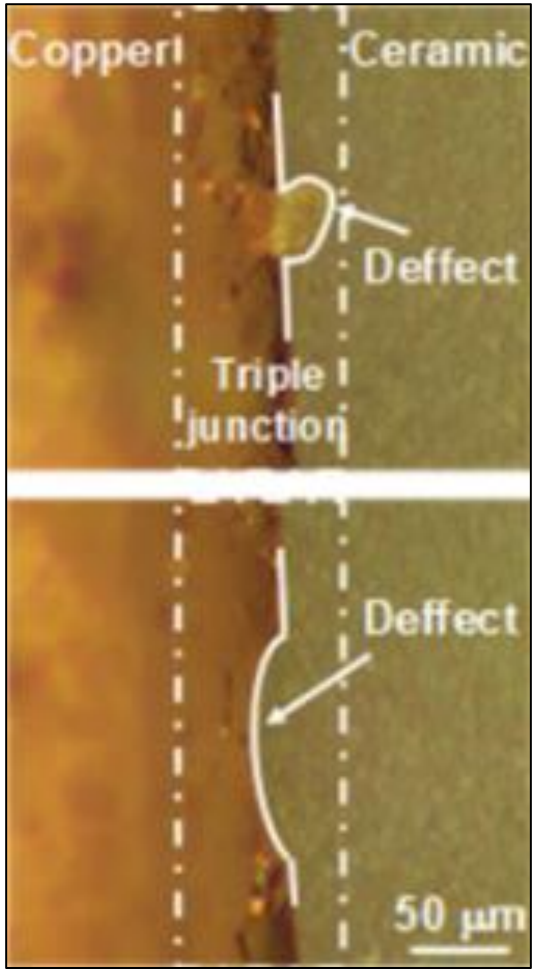
# Electrical Trees

- **Definition:** a pre-breakdown phenomenon which progresses through repeated partial discharges
- Electrical trees begin at the electrode and end at a void
- Ultraviolet light and gaseous products resulting from the PD degrade the dielectric materials
- Repeated PD can grow the tree until it branches from one electrode to another resulting in catastrophic failure.



# Choosing the Right Ceramic Material

- Powerex utilizes aluminum nitride (AlN)
  - High dielectric strength (20 kV/mm)
  - Good thermal conductivity (230 W/mK)
- Quality is key
  - Voids within ceramic or under metallization will result in PD
  - Poor etching uniformity is the seed of electric trees
  - Diamond saw to avoid conductive slag produced during laser scribing



**Voids under the metallization lead to delamination and decrease module lifetime*

# Impact of Silicone Gel on Partial Discharge

**Dielectric Properties**:

- Silicone gel enhances the dielectric strength of the insulation, reducing the likelihood of partial discharge formation.

**Gap Filling and Stress Relief**:

- Silicone gel fills gaps and voids in the module, providing uniform insulation and reducing localized stress that can lead to partial discharges.

**Moisture and Contaminant Protection**:

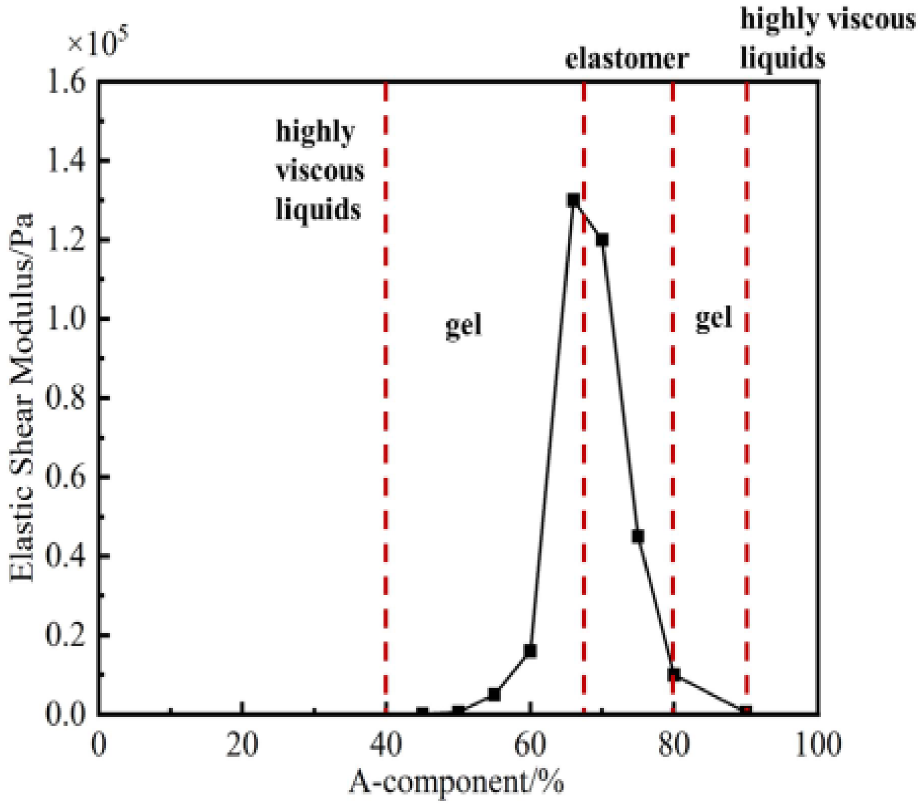
- Silicone gel acts as a barrier against moisture, dust, and contaminants, which can lower the risk of partial discharge by maintaining the integrity of insulation materials.

**Cure Time and Consistency**:

- Proper curing of silicone gel ensures consistent coverage and minimal voids, optimizing the partial discharge resistance in high-voltage environments.

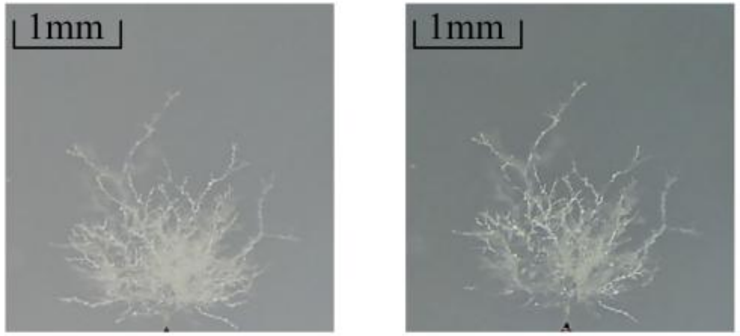
**Aging and Degradation Resistance**:

- Silicone gel is resistant to aging and degradation over time, maintaining its performance and insulating properties under high voltage conditions.

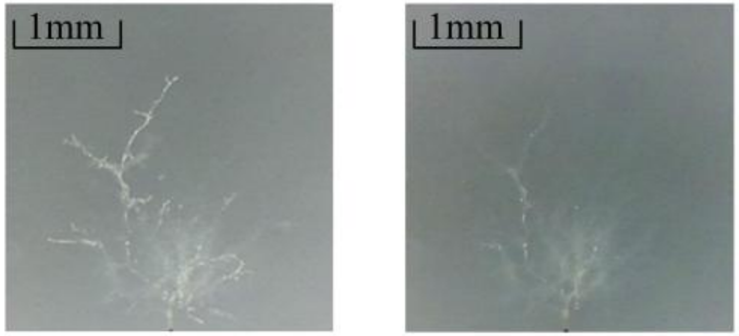


# Self-Healing in Silicone Gel

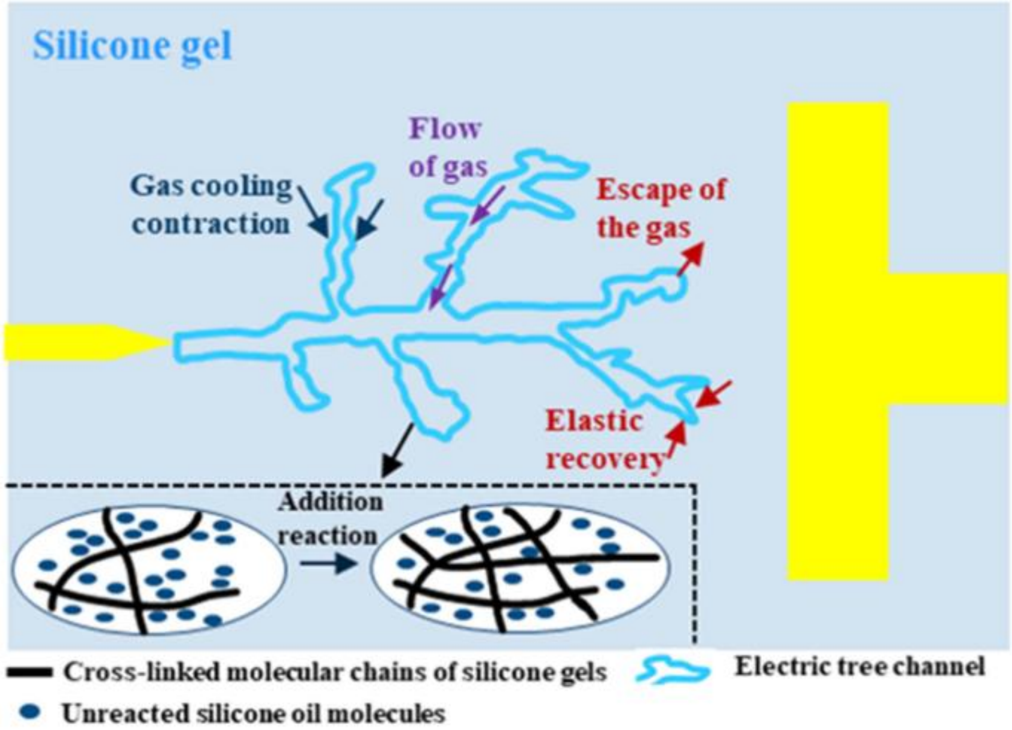
- Silicone gel exhibits the ability to heal from PD, mitigating the extent of electrical trees
- Two types of self-healing
    - Type 1: Occurs during tree propagation
        - Physical mechanism based on elastic modulus (lower = better)
    - Type 2: Occurs after PD event
        - Physical and chemical mechanism
- Gel mixtures with lower elastic modulus and higher silicone oil content exhibit more advanced healing



(a) 0min (b) 30min



(c) 60min (d) 6h



# Substrate Geometry

- Critical Area of focus for increasing partial discharge capability:
  - Incorporate fillets with a radius > 2mm on corners of metallization
  - Minimize planar area of substrate
  - Employ equal pullback of top and bottom metallization
  - Thicker ceramics improve PDIV at the cost of thermal performance
  - Stack substrates vertically

**Metallization Corner Radius**

- Utilize large radii
- Reduces charge density accumulation

**Ceramic Thickness**

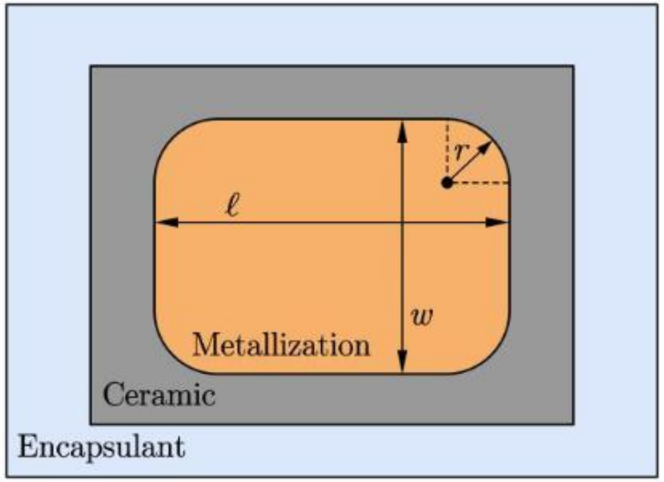
- Dielectric strength is a function of thickness (kV/mm)
- Balance thermal and dielectric requirements

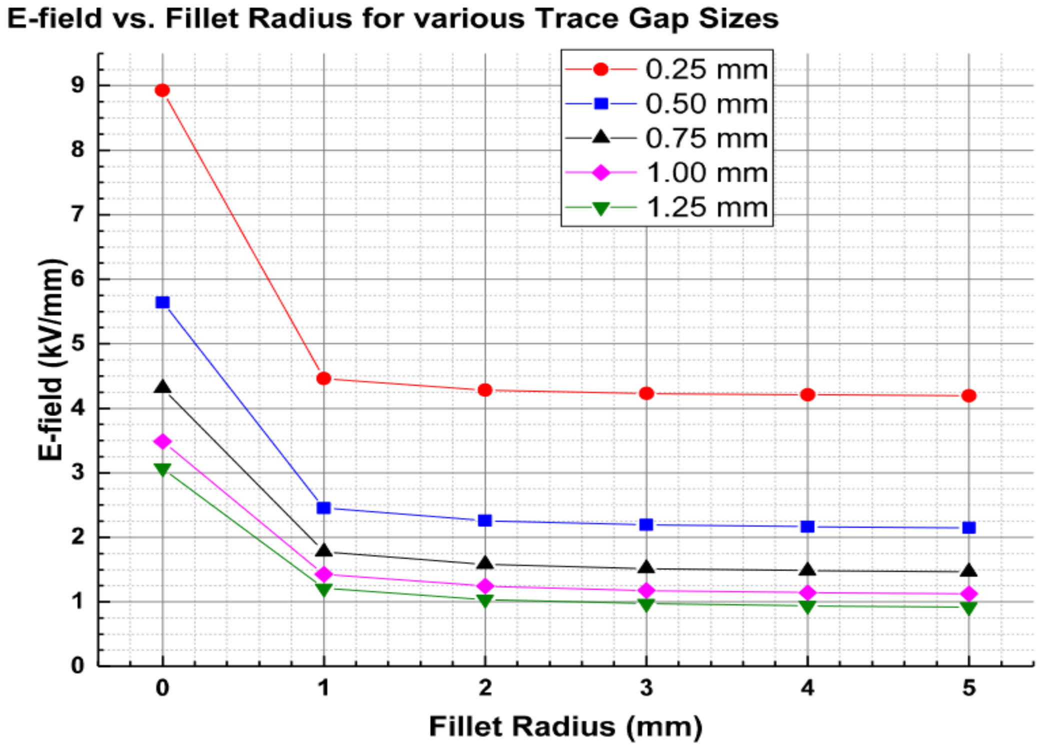
**Metallization Offset**

- Equal pullback
- 1-2mm from ceramic edge

# Substrate Metallization Radius

- Increasing the metallization corner fillet radius dramatically reduces frequency and intensity of PD events
    - 0mm to 20mm reduced frequency 96%
    - *Minimum of 1mm filet is critical*





# Substrate Metallization Pullback

- Substrates designed for low-voltage applications typically employ an offset in the pullback between top and bottom electrodes.
- Reducing the offset from 2mm to 0mm can increase PDIV up to 30%
- Powerex utilizes 0mm offset with equal 1.5mm pullback on high-voltage substrate designs

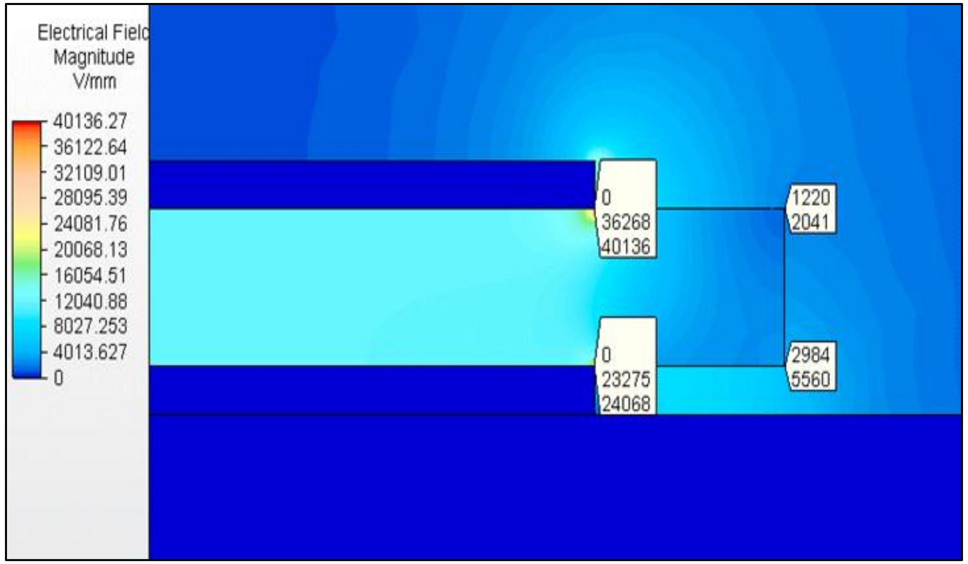
15% lower electric field at equal Cu pullbacks

Uniform electric field distribution at equal Cu pullbacks

# Overcoming Triple Point Field Enhancement for 20 kV

- Based solely on dielectric strength rating, 1 mm thick AlN should theoretically withstand 20 kV applied bias
  - Triple point field enhancement (TPFE) *in excess of 35 kV*

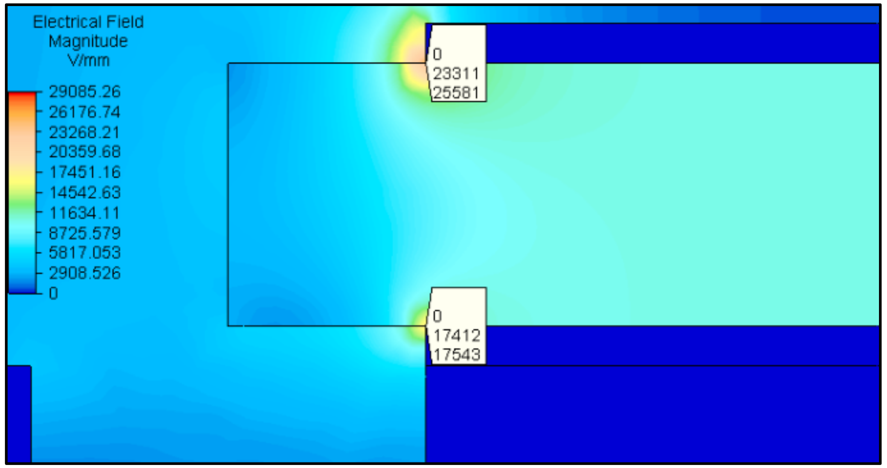
- Options to achieve 20 kV PDIV:
  - Increase ceramic thickness > 1 mm
  - Stack multiple substrates vertically

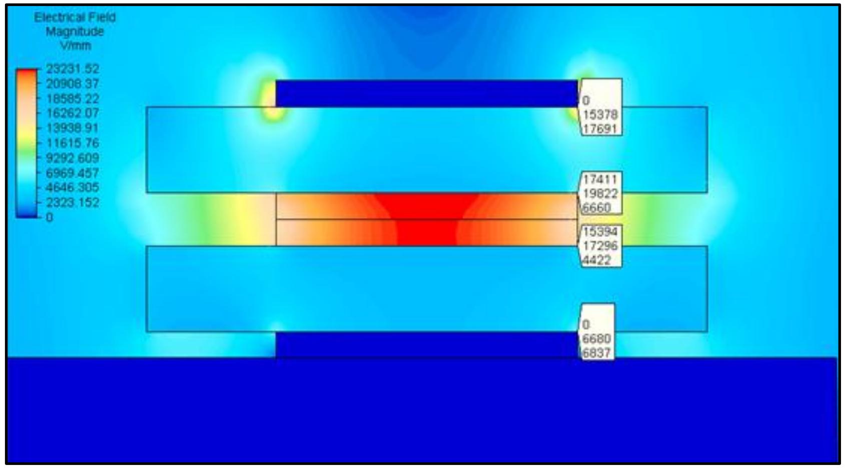


# Options for 20 kV PDIV

Single 2 mm AlN substrate:
- TPFE > 23 kV/mm
- Prone to voids within the ceramic

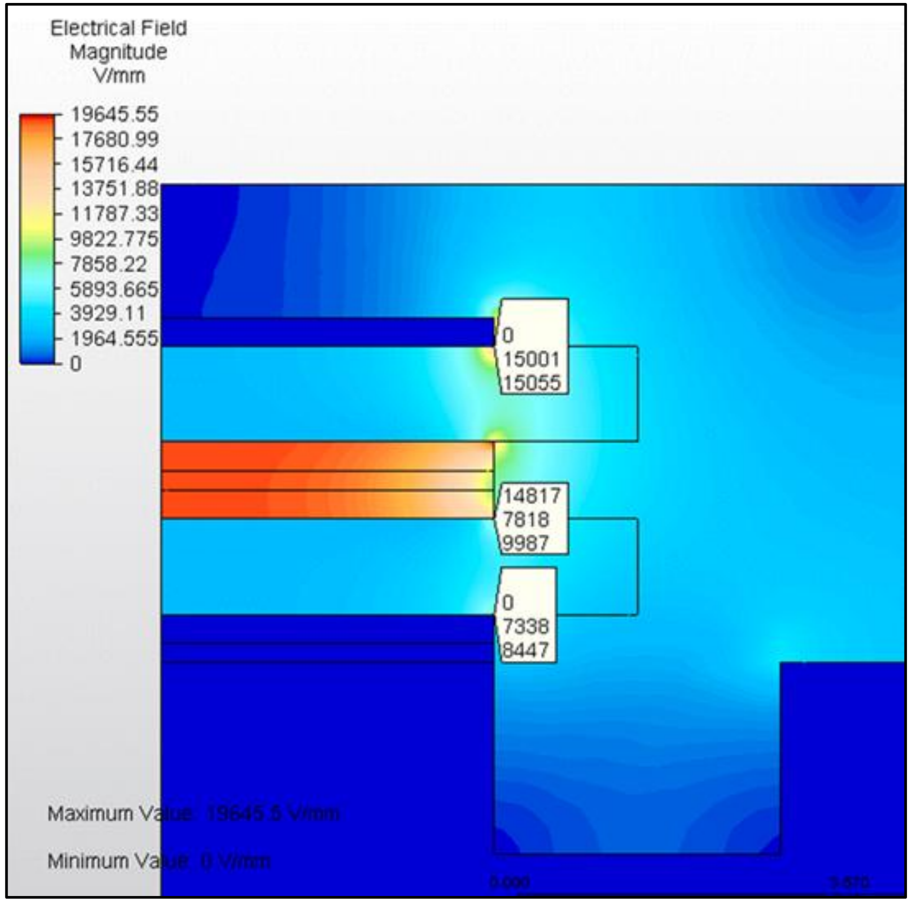
Double stacked 1 mm AlN substrates:
- TPFE < 20 kV/mm
- Increases difficulty in production





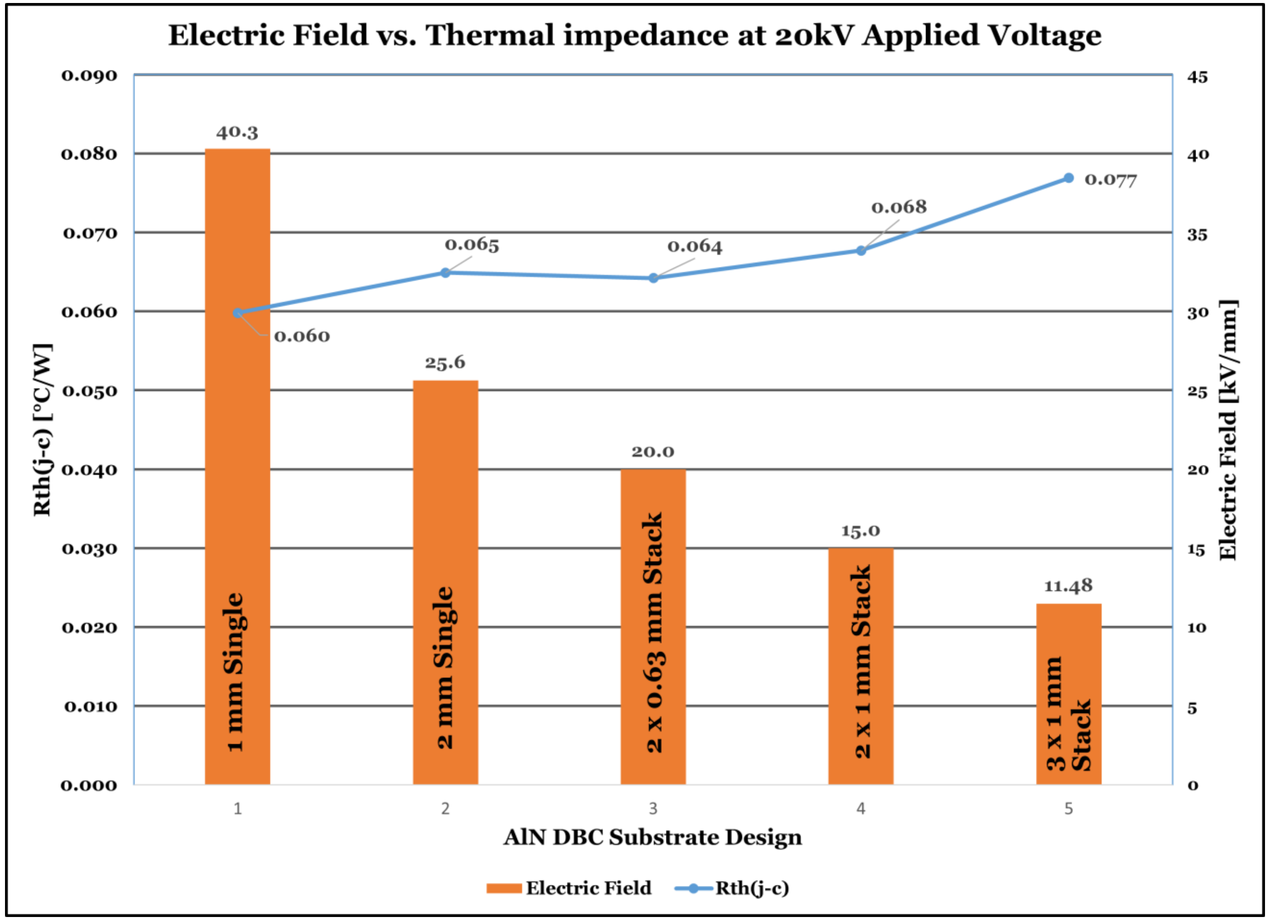
# Improvement in Stacked Design

The addition of a square 2 mm groove in the baseplate around the bottom metallization further reduces the TPFE by 15%!



# Tradeoff- Thermal vs Partial Discharge

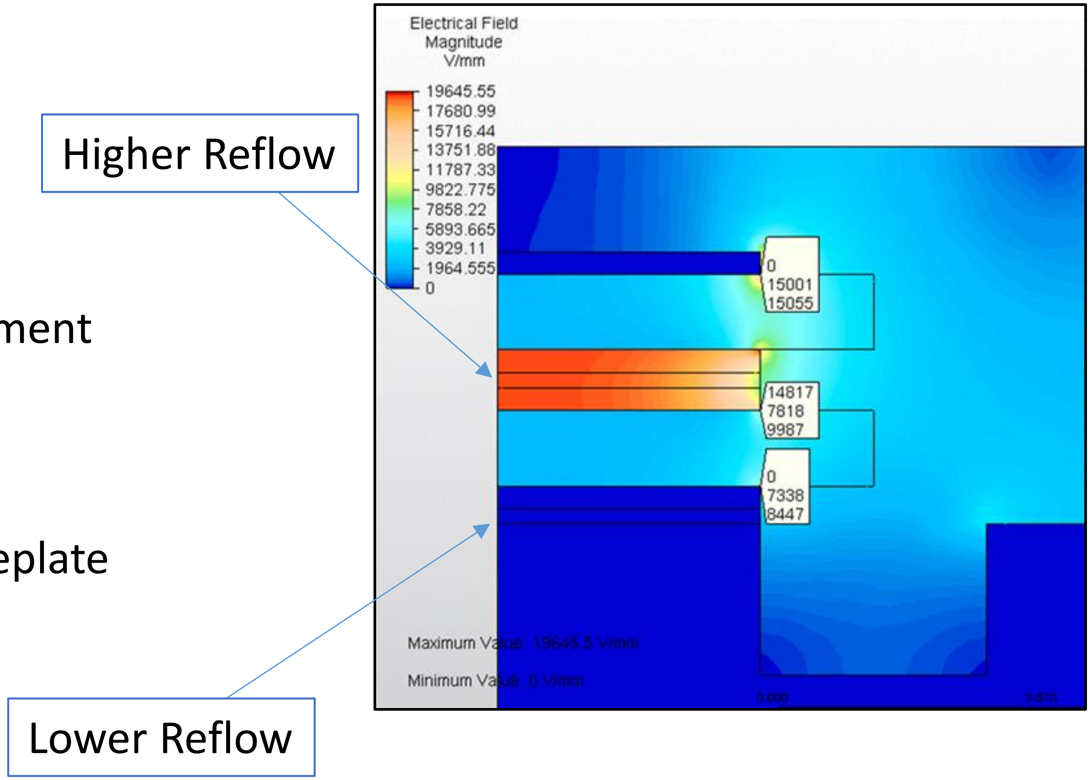
- Difference in Rth between options 2, 3, and 4 is negligible
- Options 3, 4, and 5 meet the TPFE requirement
- Option 4 is the best combination of thermal performance and TPFE reduction
- *The sacrifice in Rth of 5 is not necessary for 20 kV PDIV*



# Manufacturing Tips

## ➢*Design means nothing if your manufacturing technique is poor*

- Substrates and baseplates must be clean from ionic contamination
  - Scrub surface with mild abrasive and/or run through a plasma cleaner
  - Store in an inert atmosphere until ready for use
- Solder joints must contain less than 5% voiding
  - Reflow in vacuum oven
  - Check joints with acoustic microscopy or x-ray imaging
- Stacked substrates must be perfectly aligned
  - Surface tension is not always enough to guarantee alignment
  - Employ fixturing to maintain alignment during reflow
- Construct stacked assembly in multiple steps if necessary
  - Higher reflow solder between substrates
  - Lower reflow solder between bottom substrate and baseplate
- Flux contamination must be removed
  - Ionic contamination will poison gel and kill your module
  - Certain geometries may require extra attention
  - Ionograph testing to validate cleaning



# Conclusion

- Partial discharge most frequently occurs at the triple point
  - Repeated PD forms electrical trees
- Vertically stacked substrates provides the most significant reduction in triple point field enhancement
- Substrates must be free from edge imperfections, voids in metallization, and conductive slag
- Manufacturing techniques are critical to prevent ionic contamination, voids, and substrate misalignment