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Extending Board Level Reliability(BLR) of a Wafer Level Fanout 4D Digital Radar Chiplet Package

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Presentation Outline

Extending BLR of a Wafer Level Fanout 4D Digital Radar Chiplet Package

- Package
- Test Method
- System Considerations and Test Board Design
- BLR Results
- BLR Results with Edge Bond Materials
- Where do failures occur?
- Conclusions

The First Digital Automotive Radar

"If it moves, it will be automated -- and it must be safe. The time is now to make a fundamental paradigm shift away from legacy, analog radar, toward digital radar systems that provide the much more accurate information needed for sophisticated algorithms to save lives."

Manju Hegde, CEO and Cofounder
Uhnder, Inc.

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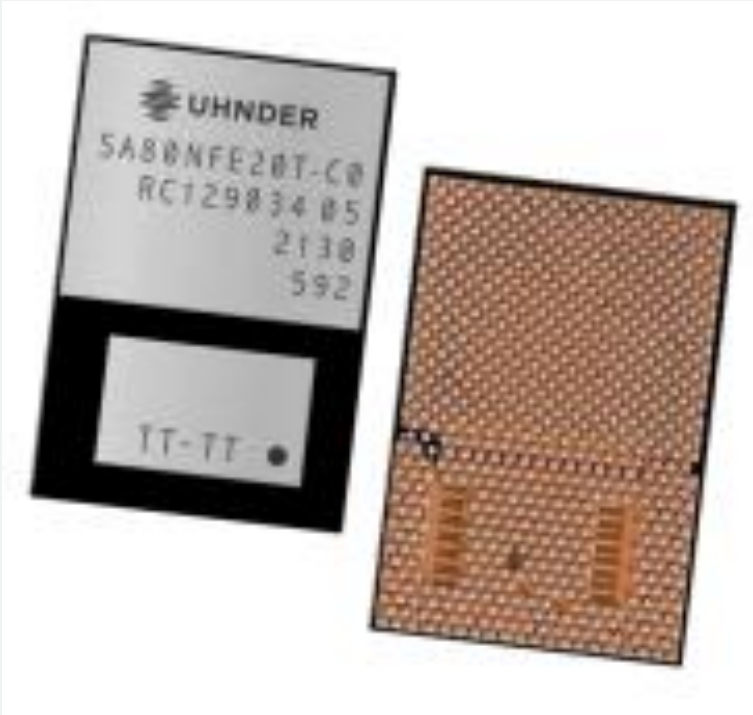
4D FO-WLP Radar Package

- Two Die
- Two FAB Technology Nodes
- Split by Function
  - Large die
    - Compute
    - CSP construction
    - Minimum die to pkg edge
  - Small die
    - Analog
    - FO-WLP construction
- Back of Die exposed
  - Provides Thermal path



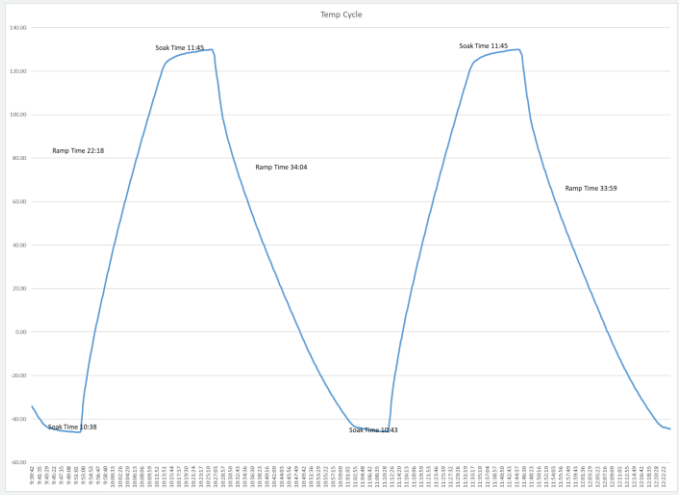
- Package Size
  - 8.2 x 12.8 mm
- Construction
  - 2 RDL layers +UBM
  - 717 IO
- Pitch
  - Minimum pitch 0.35mm
  - Custom pattern
  - Sections of package are on different ball pitch coordinates

Test Method

Test Method
Our TC-Test SPECS

IPC9701A test parameters
- Single chamber
- -40°C to 125°C
- Soak Time is 10-11 minutes
- Cycle time ~78 minutes
  - Cold to hot 22 minutes (7.5°C/min) (using heating assist)
  - Hot to Cold 34 minutes (4.9°C/min)
  - 18.5 cycles per day
- With increased chamber loading cycle
  - 90-96 minutes
  - ~15 cycles/day

Failure is 1000 Ohm over T0 room resistance.
- Resistivity increases by 40% room to hot
- Resistivity decreases by 25% room to cold



IPC 9701A Test Spec

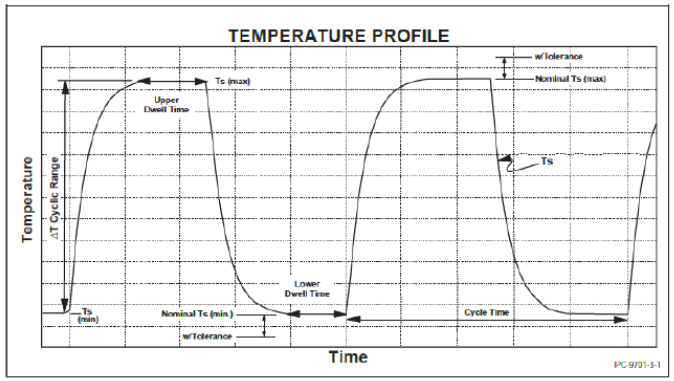


Figure 3-1 Representative Temperature Profile for Thermal Cycle Test Conditions (Figure 3-1 based upon Figure 1, Annex A of JESD22-A104-B)

Table 4-1 Temperature Cycling Requirements, Mandated and Preferred Test Parameters Within Mandated Conditions

Test Condition	Mandated Condition
Cycle (TC) Condition:	
TC1	*0°C ⟷ +100°C (Preferred Reference)*
TC2	-25°C ⟷ +100°C
TC3	-40°C ⟷ +125°C
TC4	-55°C ⟷ +125°C
TC5	-55°C ⟷ 100°
Test Duration	Whichever condition occurs FIRST: 50% *(Preferred 63.2%)* cumulative failure (Preferred Reference Test Duration) or
Number of Thermal Cycle (NTC) Requirement:	
NTC-A	200 cycles
NTC-B	500 cycles
NTC-C	1,000 cycles (Preferred for TC2, TC3, and TC4)
NTC-D	3,000 cycles
NTC-E	*6,000 cycles (Preferred Reference TC1)*
Low Temperature Dwell Temperature Tolerance (preferred)	10 minutes +0/-10°C (+0/-5°C) [+0/-18°F (+0/-9°F)]
High Temperature Dwell Temperature Tolerance (preferred)	10 minutes +10/-0°C (+5/-0°C) [+18/-0°F(+9/-0°F)]
Temperature Ramp Rate	≤20°C [36°F]/minute
Full Production Sample Size	33 component samples (32 test samples plus one for cross-section, add additional 10 samples for rework, if applicable)
Printed Wiring (Circuit) Board (PWB/PCB) Thickness	2.35 mm [0.093 in]
Package/Die Condition	Daisy-Chain Die/Package (see Table 4-2)
Test Monitoring	Continuous Monitoring (see Table 4-4, Preferred Reference-Event Detector)

System Considerations and Test Board Design

System Considerations

4D Digital Imaging Radar-on-Chip operating in the 76-81 GHz

- Board Materials friendly to RF Routing
  - Low Loss (Df)
  - Low Dk
- Low CTE
  - Minimize board to package CTE mismatch
- Smoothness of Cu foil
  - Minimize RF signal Loss
- Number of board layers required for escape routing
- Escape Routing friendly to RF
- RF friendly Pad finish –OSP or Immersion Ag

Test boards designed to match likely system construction

BLR Test Board Designs

Test Boards designed to more closely match use case.

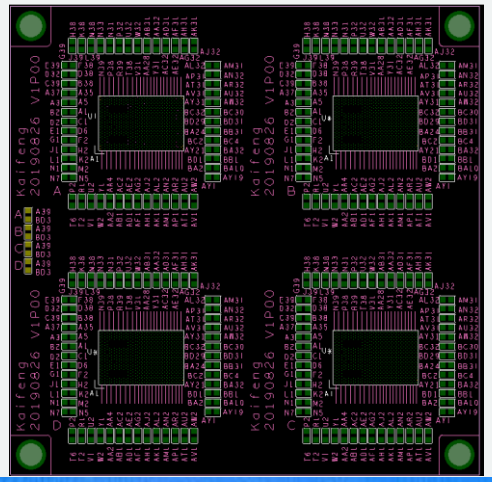
Board A

- Initial board
- 70mm board 4 device board
- One chain containing die, package and corners (~750 ohms)
- Hand wiring required for test setup
- NSMD

Board B

- Each device has 3 chains (die, package, corners)
- Package and corners continuously monitored (20-24 ohms and 1-4 ohms)
- B1 devices split between SMD and NSMD pads
- B2 all device pads were NSMD
- Fabricated with various RF material stacks

Board A

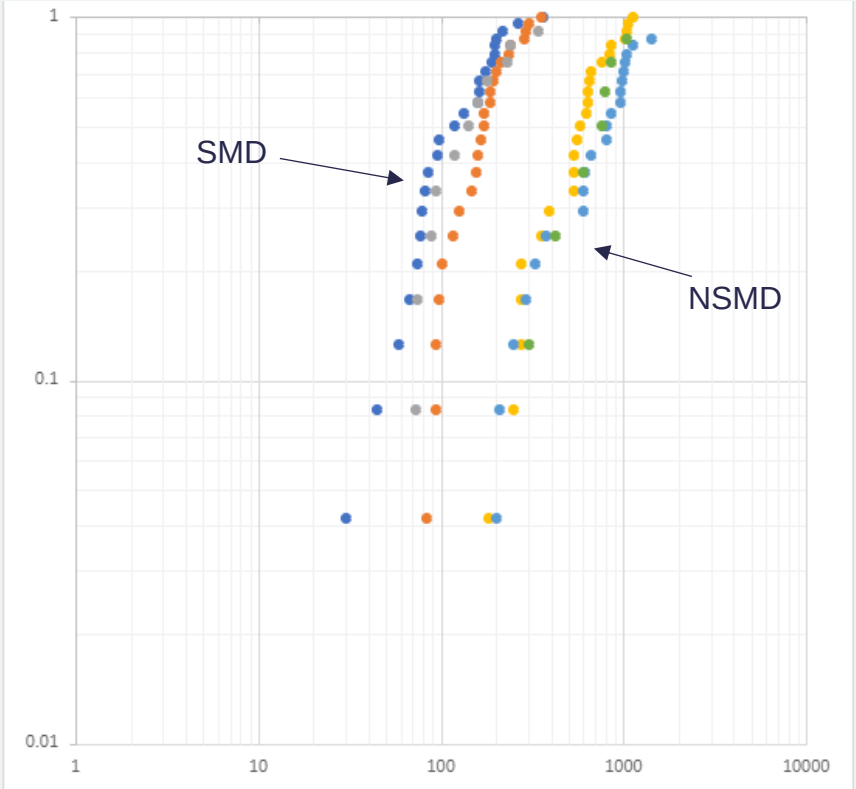


Board B1 and B2

SMD vs NSMD pads

Test Board B1

- Initial limited sample with Board A showed promising results
- Board B1 vs Board A
  - Thicker board – 2X dielectric
  - Thicker Copper – 30% metal
  - Contained both SMD and NSMD pads
- Very Poor Results
- Allowed for quick data collection to assess:
  - Pad Geometry Impact
    - NSMD pads showed significant improvement
  - Solder Volume Optimization
    - 100%, 130%, 160% of initial volume tested
    - Solder volume chosen was Nominal tested
- Optimizations used on all further tests



BLR Test Data cycled -40C to 125C

BLR Test Board Designs

Test Board B2

- 8 devices per board
- All use NSMD pad
- Pad finish immersion Ag
- Each device has 3 chains (die, package, corners)
- Package and corners continuously monitored (20-24 ohms and 1-4 ohms)
- Fabricated with various stacks

Board B2

PCB Board Materials Properties

Key Properties of Primary materials used for test boards

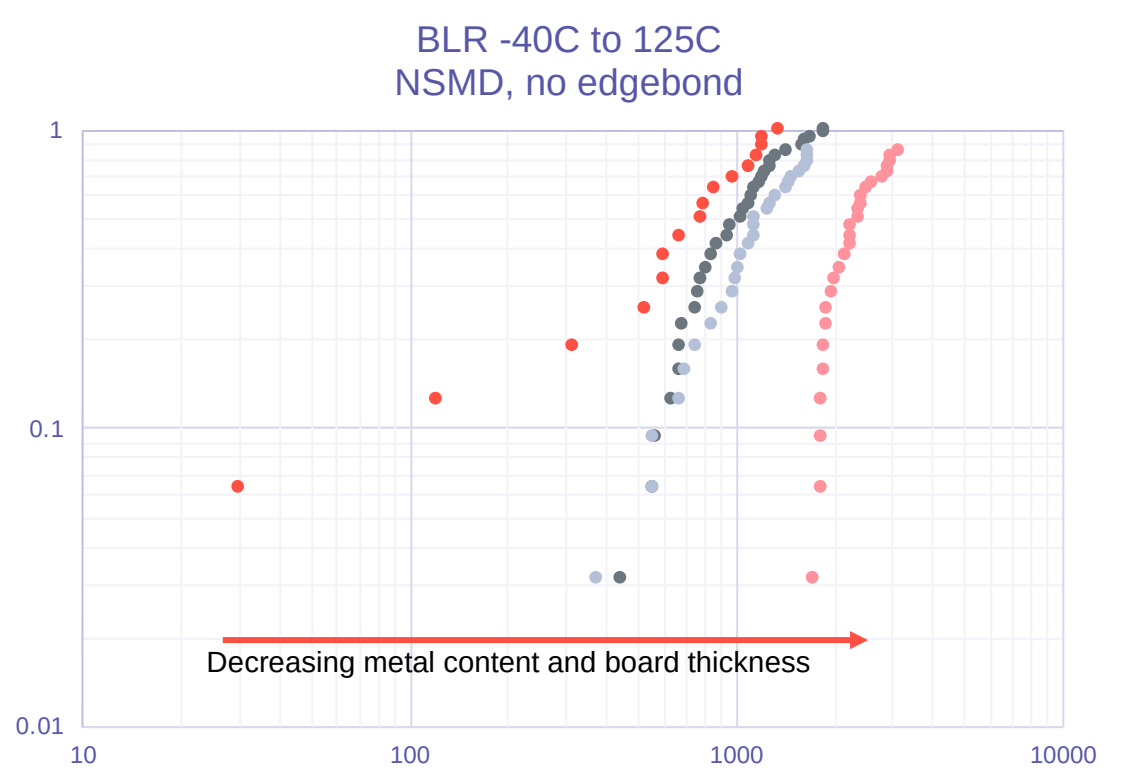
	Dk	Df	CTE (x, y) ppm/℃	CTE (z) ppm/℃	Elastic Modulus GPa	Tg ℃
Material A	3.5	0.002	14-16	42		200
Material B	3.5	0.003	6-8	20-30		240-260
Material C	3.3	0.002	5-10	35-55	7-11	180-240

- Most testing used Material B
- CTE given is for dielectric material
- Fabrication construction influences CTE of the final board

BLR Results

BLR Data

Effect of varying board and metal thickness on BLR using PCB Material B



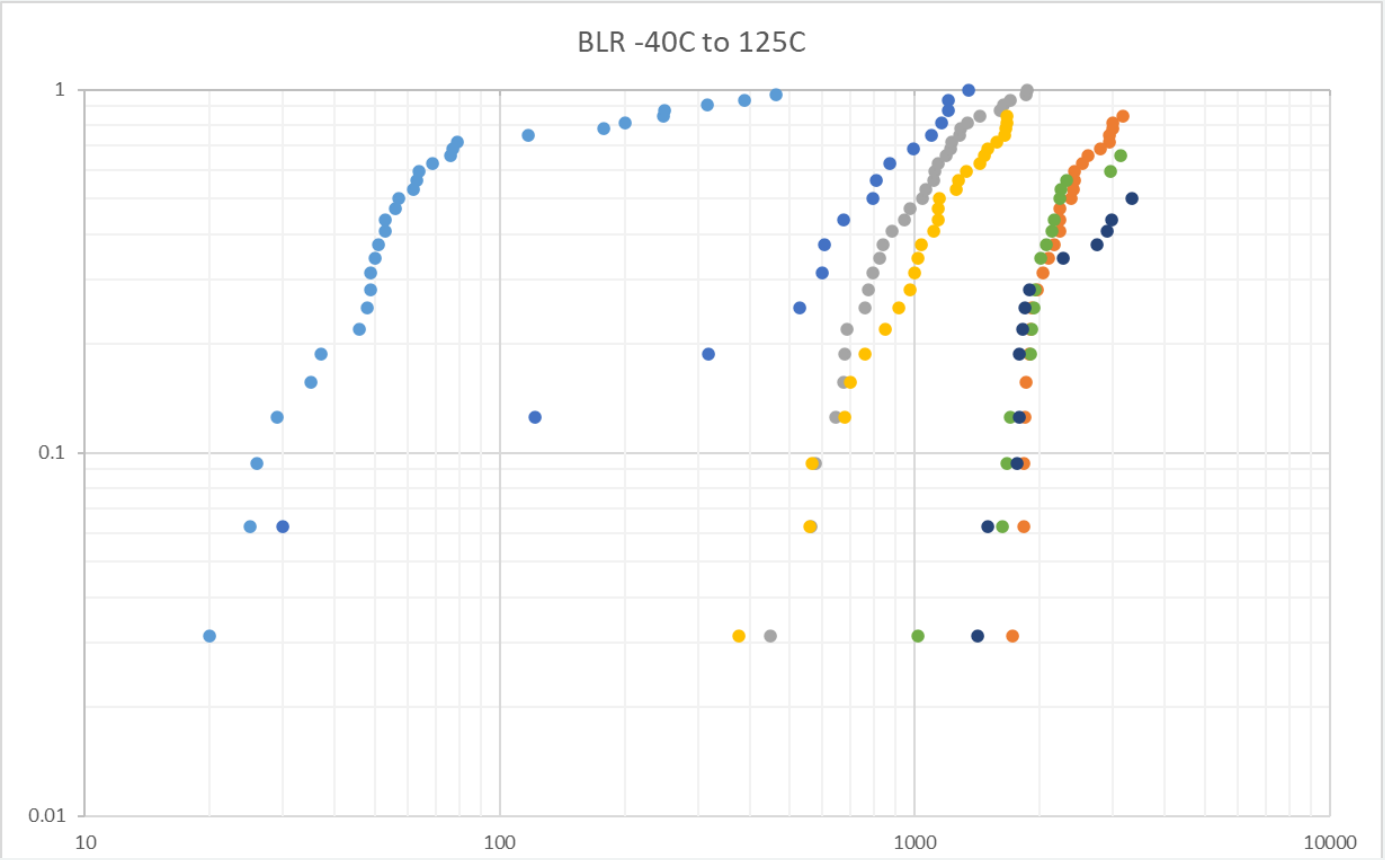
units µm	Board B	Board B	Board B	Board A
Total Metal	326	197	196	194
Total Dielectric	647	585	382	378
Sum	973	782	578	572
Actual Bd Thickness	983-1016	871-887	679-715	635-649
Design Bd Thickness	1000	830	650	690

Data taken from PCB fabrication compliance reports
Columns are listed from left to right on chart

- Metal content dominate factor.
- Dielectric thickness secondary factor

BLR Summary of Construction Tested

Materials: Material A, Material B, and Material C



	Thickness from Compliance Reports		Cycles to fail	
	Metal (µm)	Board (µm)	1st	63%
Material A	293	939-966	20	69
Material B	326	982-1016	30	870
Material B	197	871-887	450	1141
Material B	196	679-715	377	1431
Material C	217	936-964	1015	2323
Material C	218	703-747	1414	2911
Material B	194	635-649	1725	2529

Note: List is in order of data from left to right on chart

BLR Edgebond Results

Material B Board CTE and Edgebond Materials

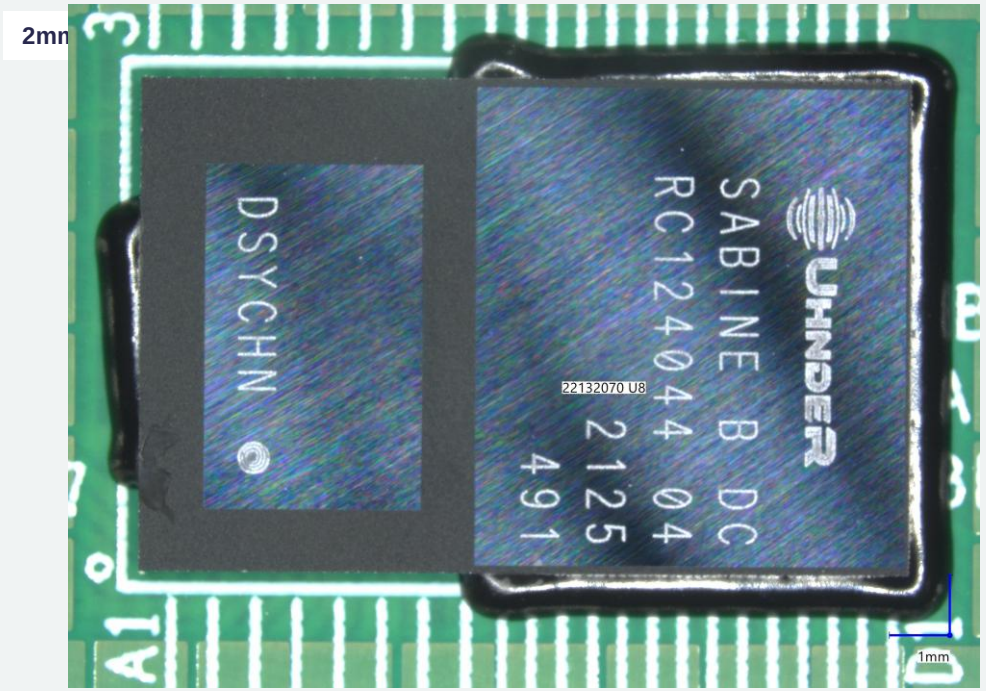
A custom formulation and a standard formulation Edge Bond were tested.

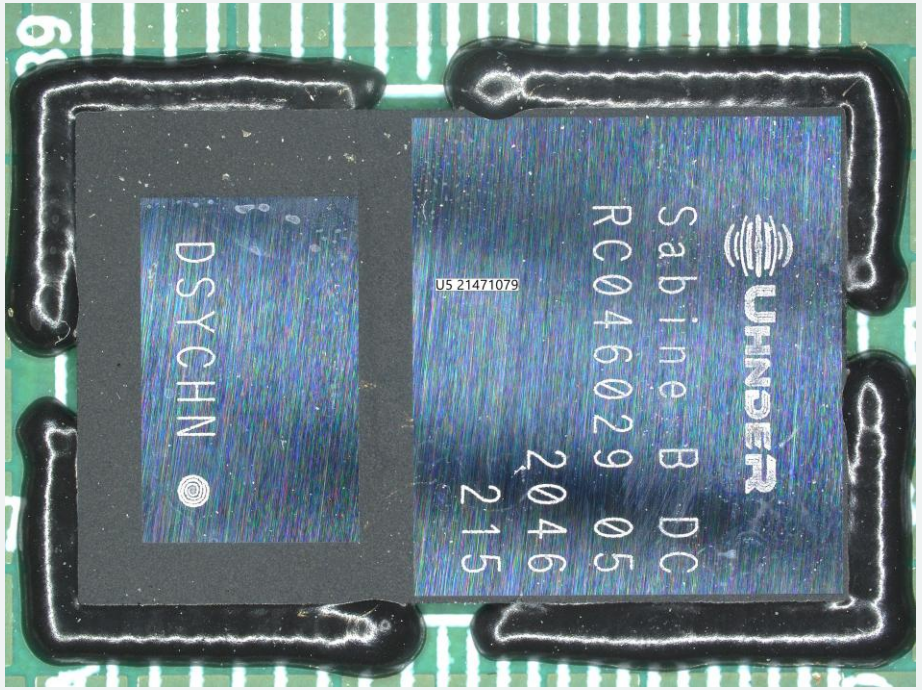
- PCB Composite CTE on Material B Designs:
  - Measured to be 15-15.5 ppm/°C range.
- Edgebond materials:
  - Targeted between the CTE of the device and the board.
    - CTE of the silicon die ~3.0 ppm/°C
    - CTE of the FO-WLP mold compound ~7.5 ppm/°C.
  - Partnered with two Edge Bond Suppliers
  - EB1 standard commercially available material with a CTE of 15 ppm/°C matching board.
  - EB2 custom material with CTE of 10 ppm/°C.
  - Data was taken on both materials.

Properties	unit	Edge Bond 1 (Standard)	Edge Bond 2 (Custom)
Color		Black	Black
Tg	deg C	150	150
Onset of Transition	deg C		110
CTE Alpha 1	ppm/deg C	15	10
CTE Alpha 2	ppm/deg C	56	37
Pot life	days @25C	7	3
Shelf life	months/temp	6 @ -5C	6 @ 2-8C
Cure Condition	time/temp	5 min@130C 15 min @120C	8 min @130C
Specific Gravity	g/cc	1.8	2.1*
Elongation	%	1.76	2.3*
Hardness	Shore D	95	>90
Dk	at 10GHz	3.4	
Df	at 10GHz	0.013	

Edgebond Dispense Patterns

A custom and standard dispense pattern were tested.





Custom pattern –

- designed to avoid top layer RF escape paths

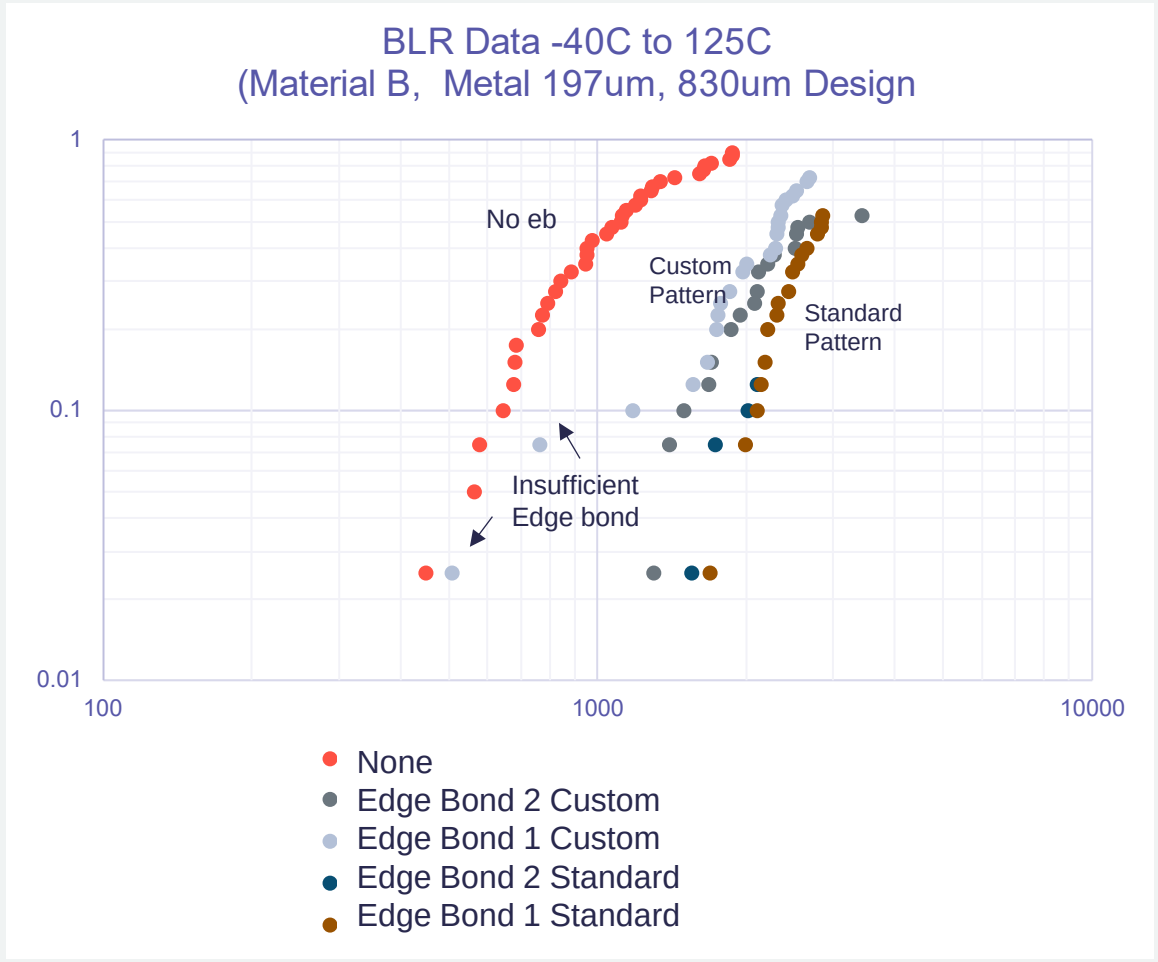
Standard pattern –

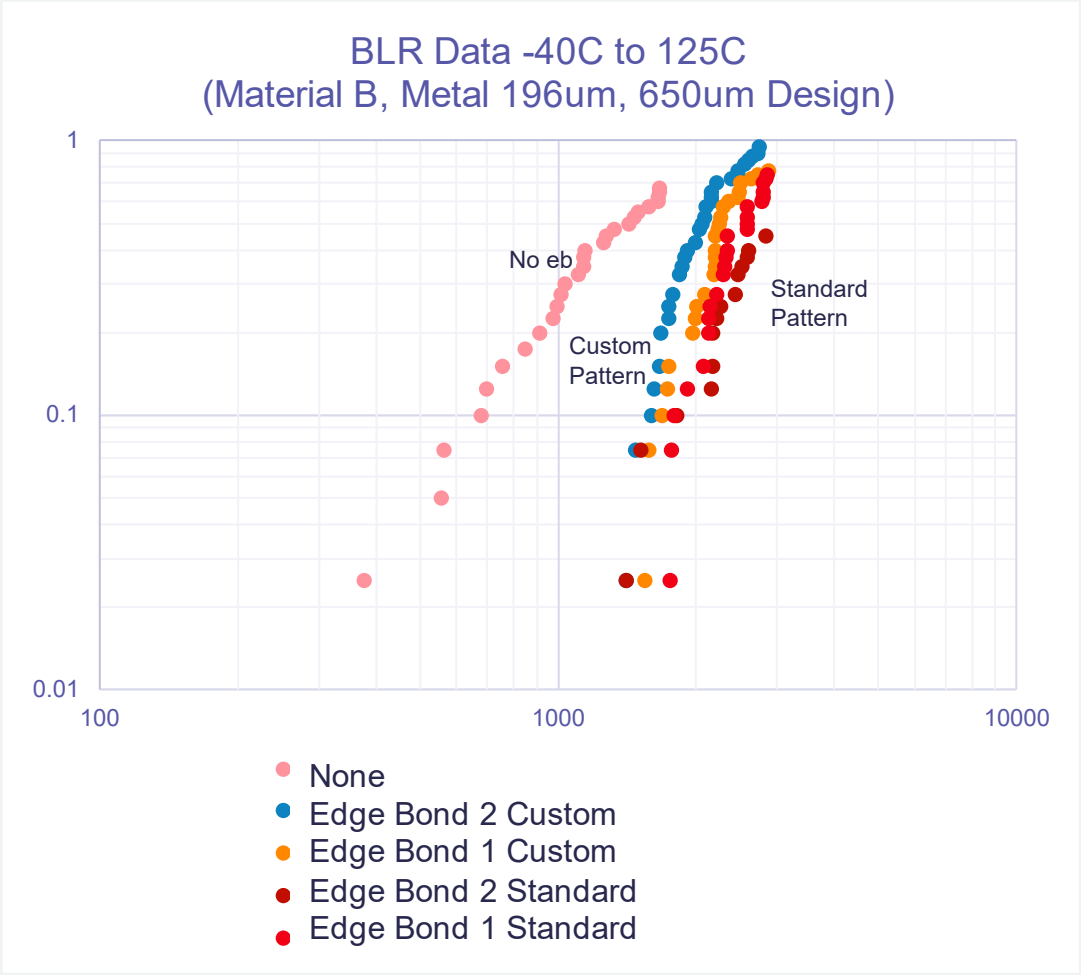
- Covers all 4 corners with outgas hole on each side

Both patterns use boards designed with 2mm keepout zone around device.
Edgebond material goes 50% or greater up the side of device with width of 70µm or greater.
No edgebond on top of device.

Edge Bond Results

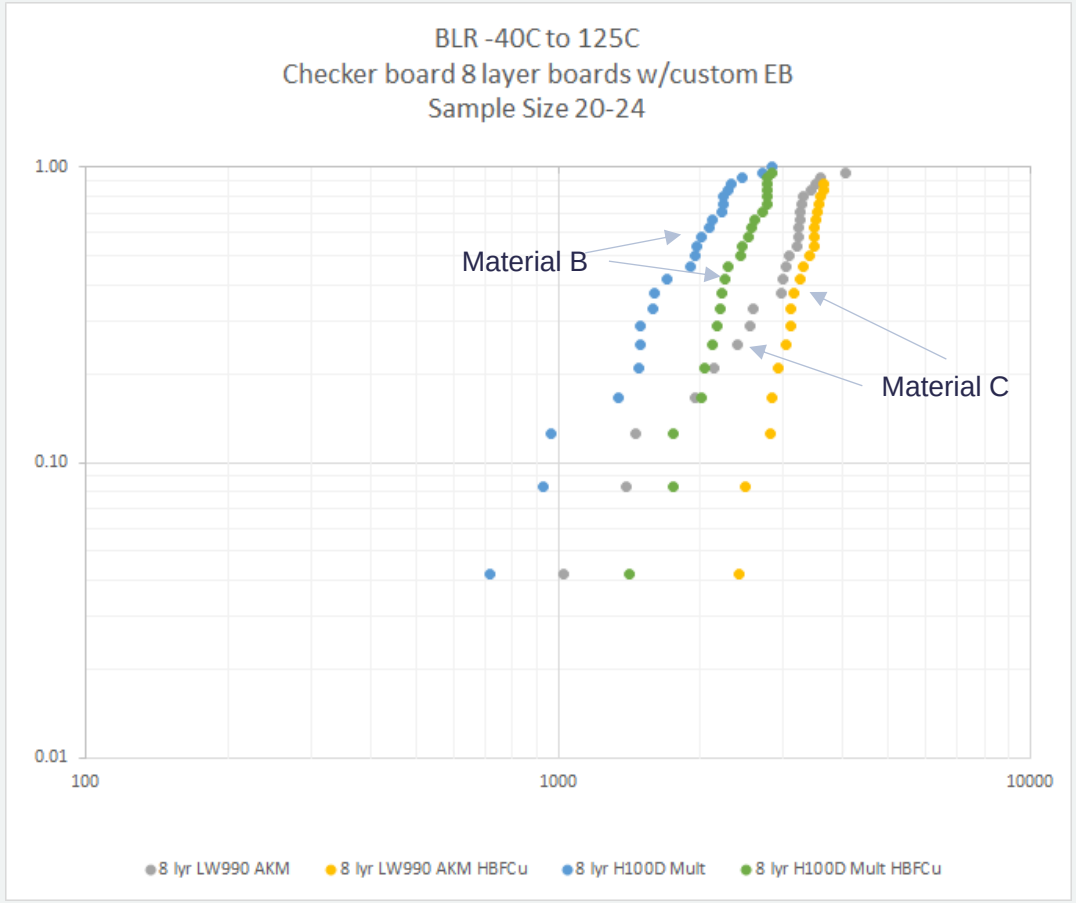
Board design comparison data – No edgebond, custom and standard pattern edge bond dispense.





Edge Bond BLR Custom Pattern

Material B and Material C with and without edge bond custom pattern.



Experiment used Edge Bond 2 material custom pattern

units µm	Board B None Material B	Board B Custom EB2 Material B	Board B None Material C	Board B Custom EB2 Material C
Total Metal	165		192	
Actual Bd Thickness	617-692		741-755	
Design Bd Thickness	650		700	
1st Fail	718	1418	1030	2421
Characteristic Life	2080	2597	3229	3490

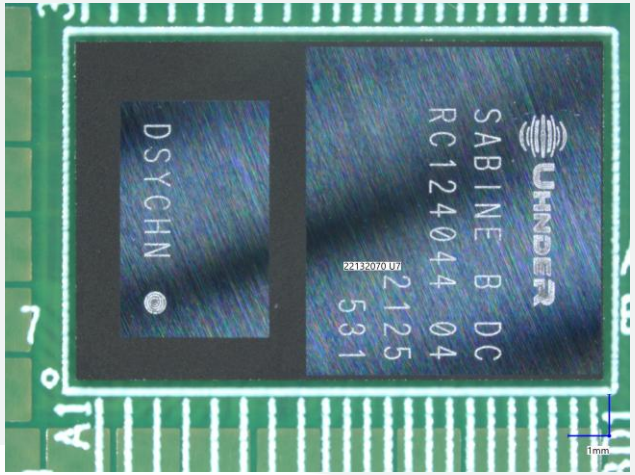
Material C achieved better BLR life than Material B in this case

- With and without EB material
- Despite having thicker metal and thicker dielectric

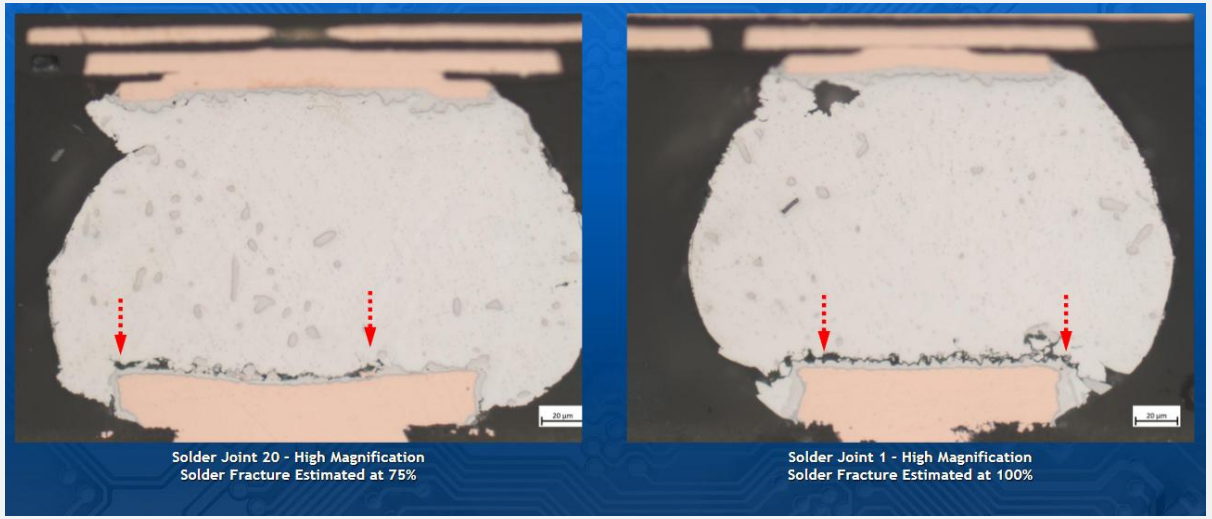
Where do Failures Occur?

Typical Failure point – Device without Edge Bond Material

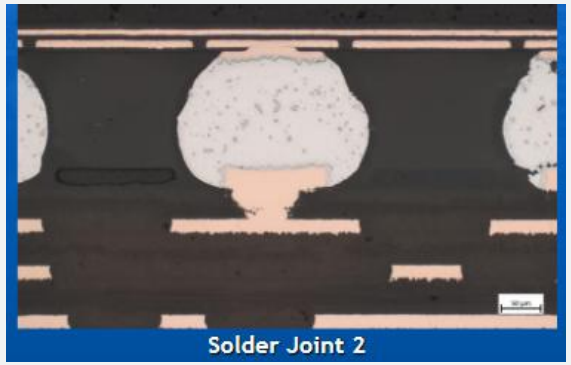
Biggest CTE mis-match is in the CSP package area and PCB board



1st fail
Row



Next balls
No damage found



Conclusions

Conclusions

- Significant contributors to BLR
  - Pad Geometry – NSMD
  - Metal Content of Board
  - Thickness of Board
  - Material of Board – (example: Material B vs Material C)
- CTE of board material does not tell the whole story
- Don’t trust design target thicknesses always confirm with compliance reports from board manufacturer
- Edge bond materials are an effective way of increasing BLR life
- Having a custom edge bond pattern decreased BLR slightly compared to a standard dispense pattern

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