Panel Level Package: Reliability evaluation of double-sided direct copper plated interconnects on embedded power chips by thermal and electrical stress test

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Outline

1. Background
2. Our Previous Technical Developments
3. Newly Updated Our Technical Developments

   Power Cycling Tests for direct Cu plated interconnect

   - Prototyping
   - Power cycling test
4. Summary

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Background

■ Applications : Power Supply Systems

Source : NTT Corporation

Source : TOYOTA corporation

- ✓ Recently, with the growth of various power-consuming devices such as motors, Inverters and data center servers, the amount of electricity consumed is increasing year by year.
- ✓ Power systems for AI data centers are moving toward vertical power architectures that increasingly require reduced wiring resistance and inductance.
- ✓ Placing the power supply near the processor (CPU/GPU/HBM) will be an important for power integrity.
- ✓ Chip-embedded packages (3D-like) can shrink size and increase current density.
- ✓ And, the use of wide bandgap power semiconductors such as GaN and SiC devices is also very effective in reducing switching losses, improving heat dissipation, and miniaturizing passive components.

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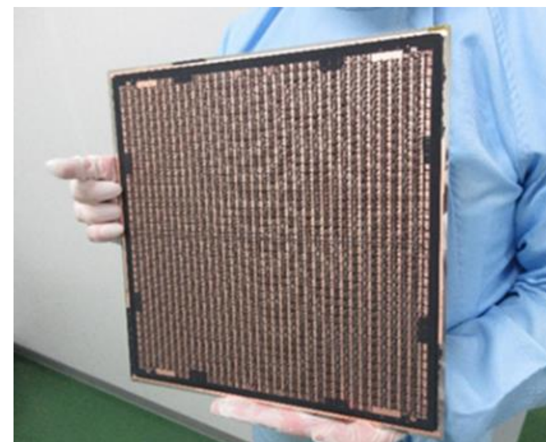
Previous Technical Developments

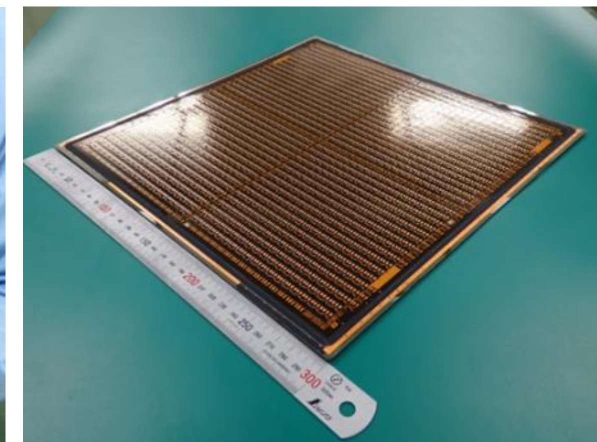
■ Power Module Packaging Technologies

We focus on power module packages using chip-embedded technology in a panel-level process

Benefits of chip embedded for power module

- *Higher power (current) density*
- *Low parasitic resistance and inductance*
- *Miniaturization and Thinner*
- *Excellent double-sided cooling concept*
- *Robust all Cu plated interconnection technology*
- *Higher scalable integration*

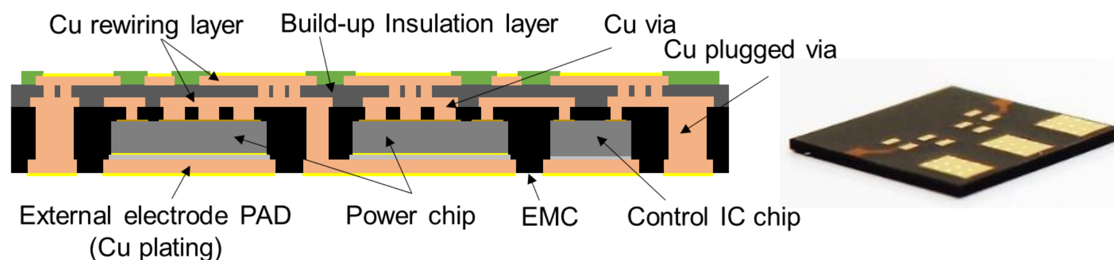




Previous Presentations

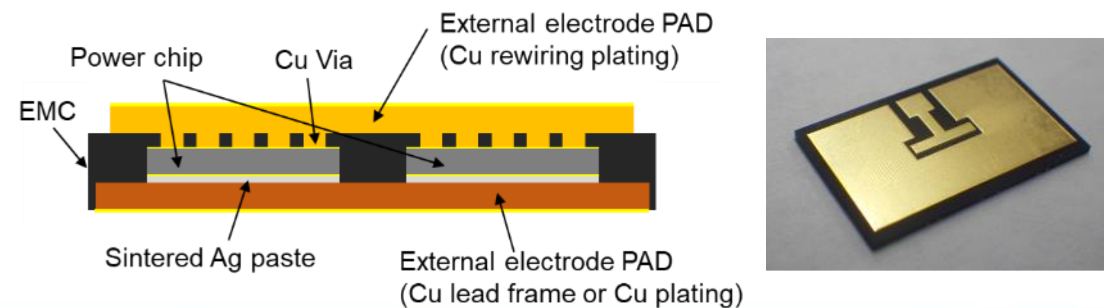
✓ ***IMAPS DPC2023***

DC-DC half-bridge application(GaN HEMT module)



✓ ***IMAPS DPC2024 and IMAPS power electronics 2024***

Inverter application(SiC core module)



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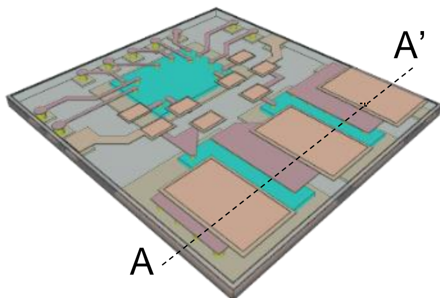
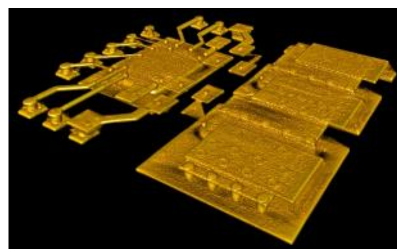
Previous Technical Developments

✓ ***IMAPS DPC2023***

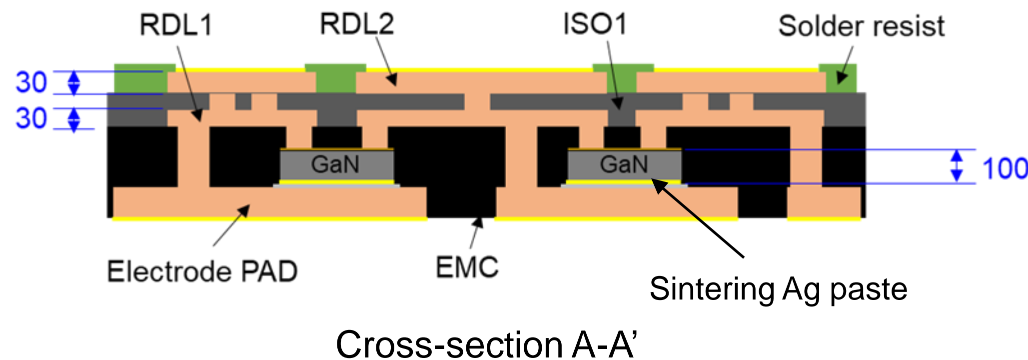
DC-DC half-bridge application(GaN HEMT module)
Extreme Thin multi-chip module (350um)





X-ray CT 3D image

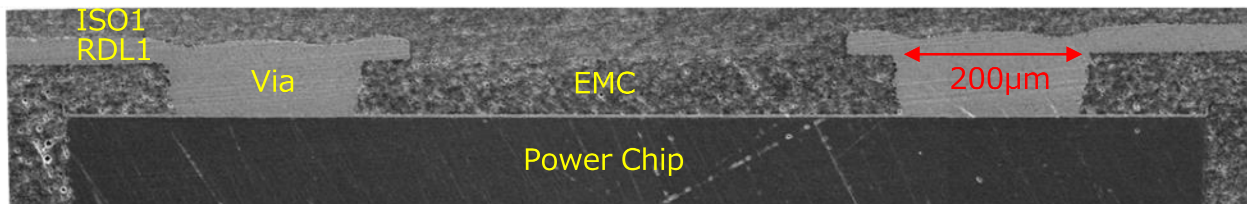
Package size :7.5×7.0mm



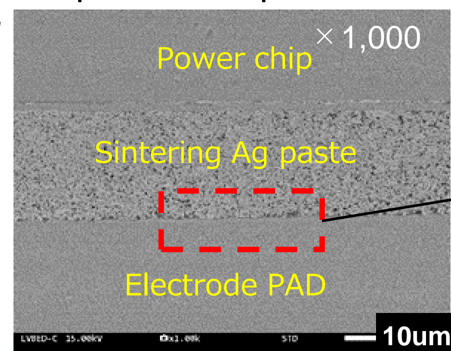
Cross-section A-A'

Cross-section image

Direct Cu plating connection of power chips



Chip attached paste



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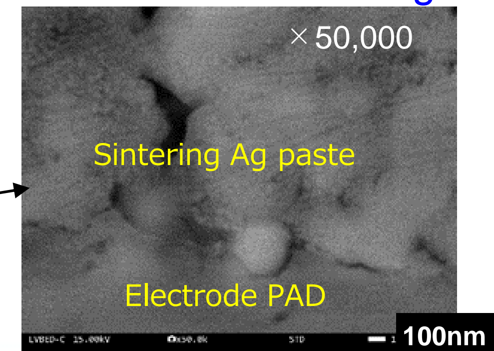

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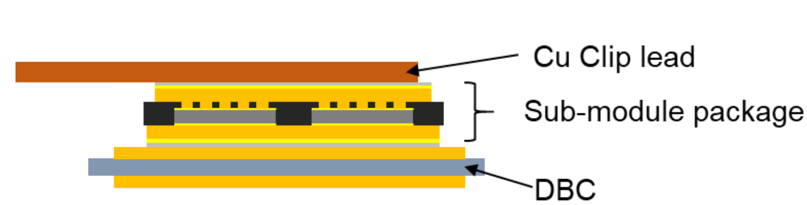
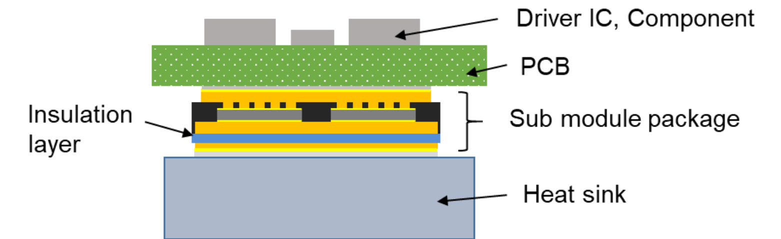
Previous Technical Developments

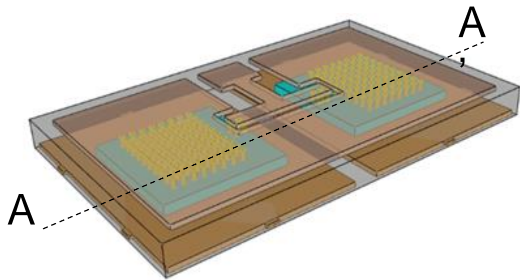
✓ ***IMAPS DPC2024***

SiC Sub-module
for Inverter application



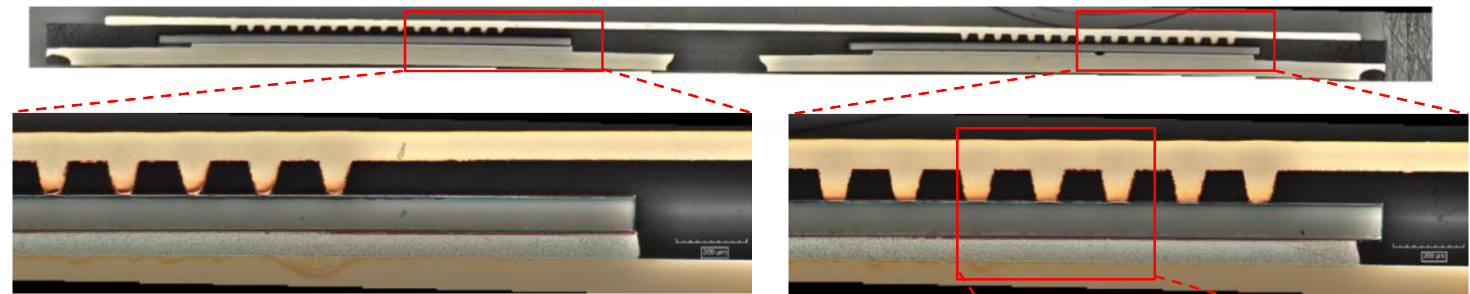


Package size :16 × 10mm



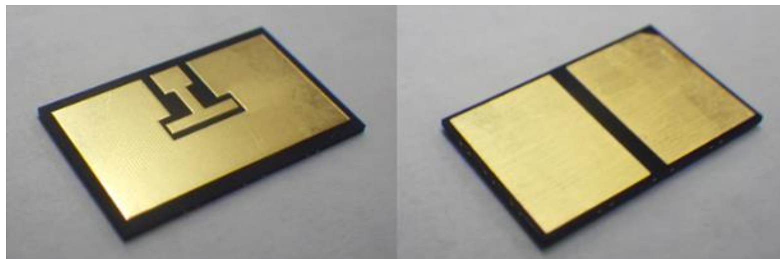
Cross-section image

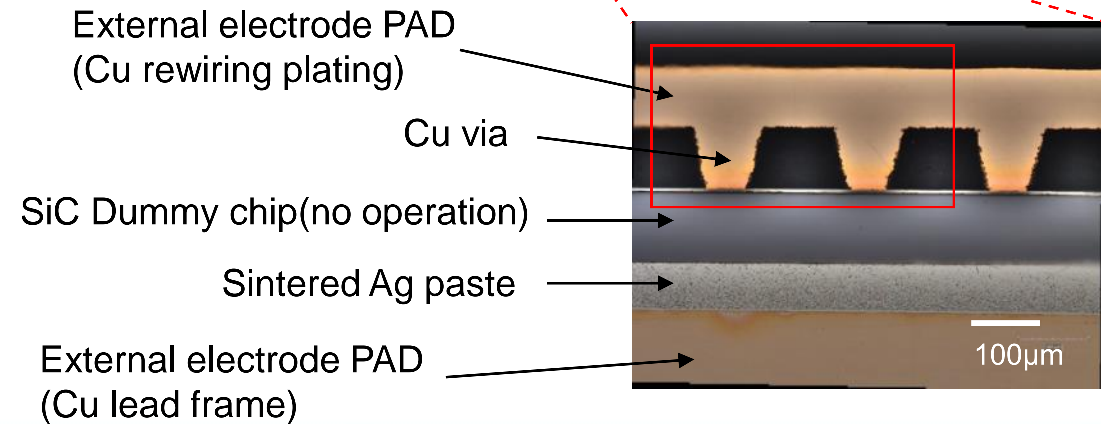
Very low resistance and inductance structure



Top

Bottom





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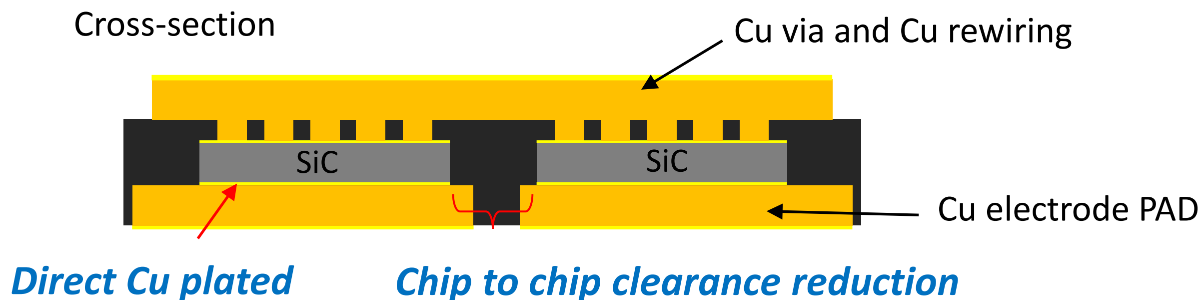
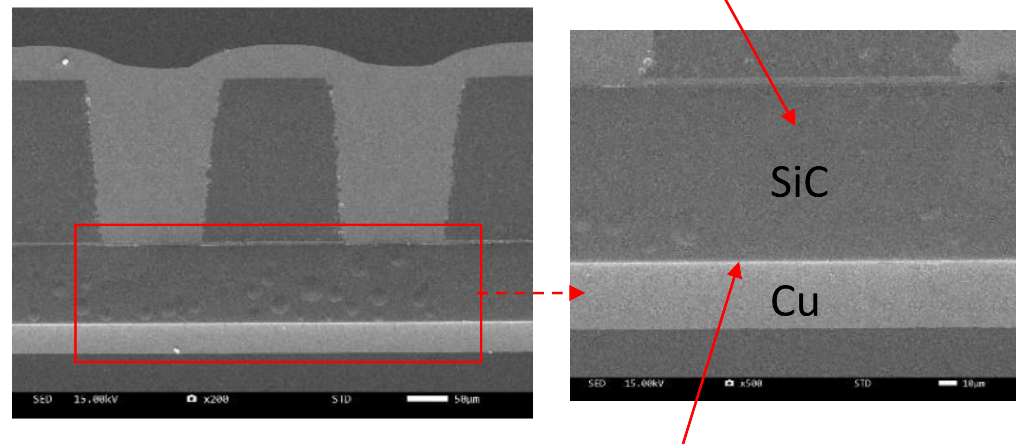
Previous Technical Developments

✓ ***IMAPS Power Electronics2024***

SiC Sub-module for Inverter application

✓ SiC chip Direct Cu plated





<Motivations>

- **Lower resistance and higher heat dissipation**
- High Reliability Bonding with power chips
- No need for high temperature bonding process (reduced Cu surface oxidation)
- **Miniaturization through chip-to-chip clearance reduction**
- **Improved BLT, spread, fillet and void control issues (without die attach materials)**

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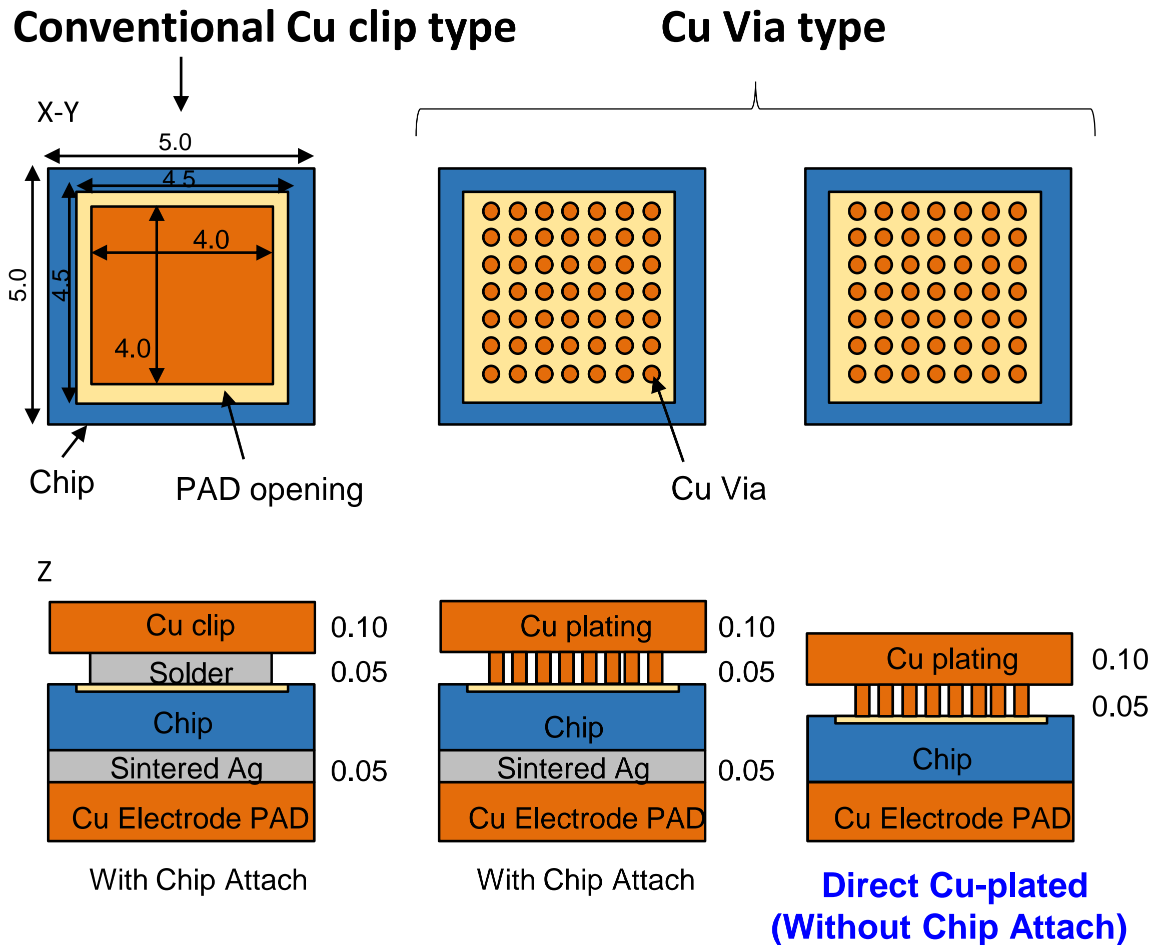
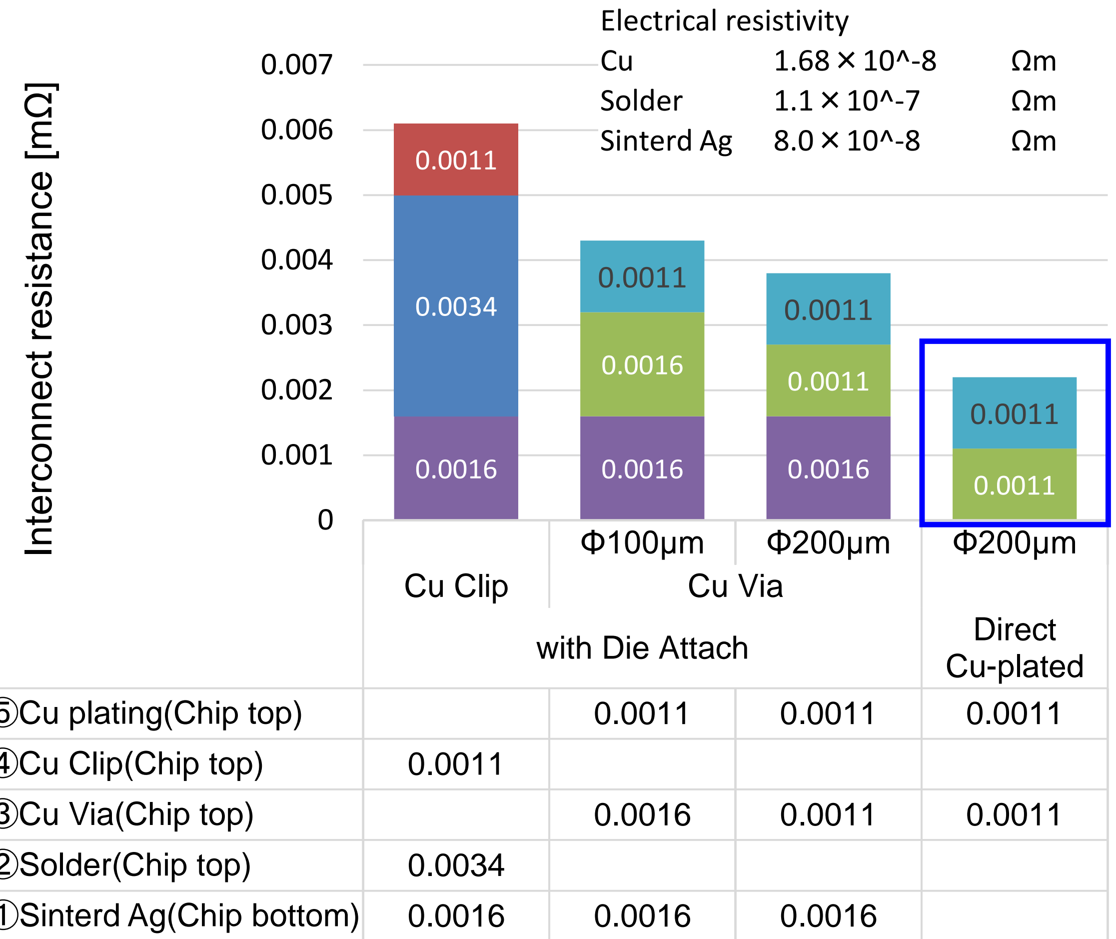
Previous Technical Developments

✓ ***Advantages of direct Cu plated: Low resistance characteristics (theoretical calculation)***





	Cu Clip (with Die Attach)	Cu Via Φ100μm (with Die Attach)	Cu Via Φ200μm (with Die Attach)	Direct Cu-plated Φ200μm
⑤Cu plating(Chip top)		0.0011	0.0011	0.0011
④Cu Clip(Chip top)	0.0011			
③Cu Via(Chip top)		0.0016	0.0011	0.0011
②Solder(Chip top)	0.0034			
①Sinterd Ag(Chip bottom)	0.0016	0.0016	0.0016	

Chip and Cu Electrode PAD are not included.

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Previous Technical Developments

✓ ***TCT results for Direct Cu plated***

Reliability test conditions（CLR: Component Level Reliability）

Test Items	Condition
Pre-Condition	The baking condition is 125 ℃ 24h. MSL = LEVEL1 Ta=85℃, RH=85%, storage=168h Reflow soldering heat stress (3times)
Thermal Cycle Test (TCT)	Ta= -65℃⇔150℃

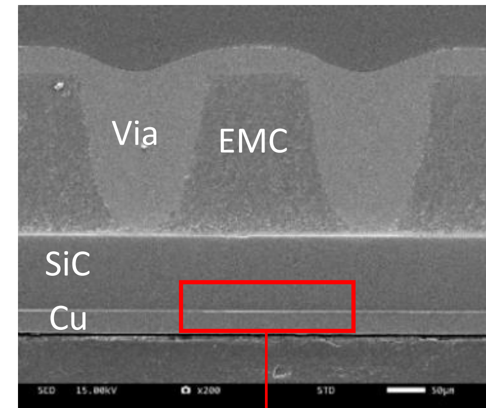
Reliability test results

TCT	n=22	Time	100 cycles	300 cycles	500 cycles	1,000 cycles
		Result (Failure rate)	0/3	0/3	0/3	0/3

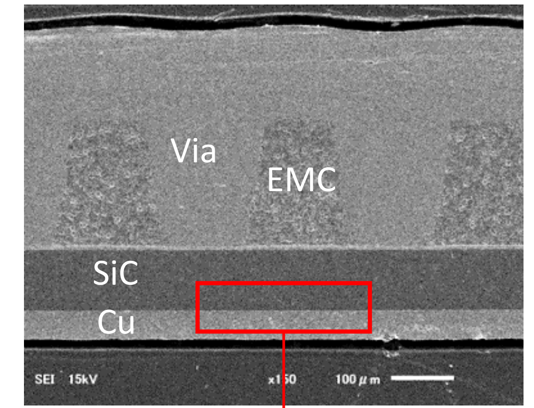
※Result :Cross-sectional SEM check by sampling

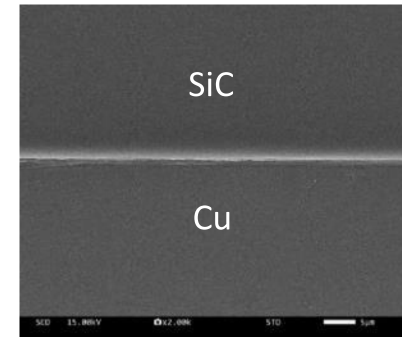
Cross-sectional SEM after each cycle

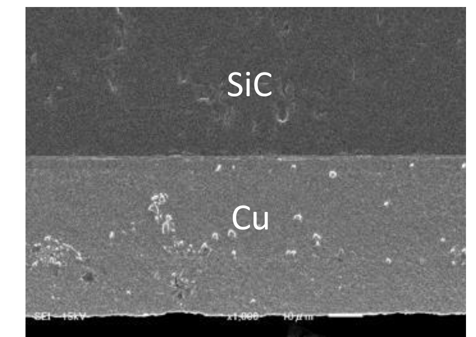
After 100cyc



After 300cyc







No delamination and cracking

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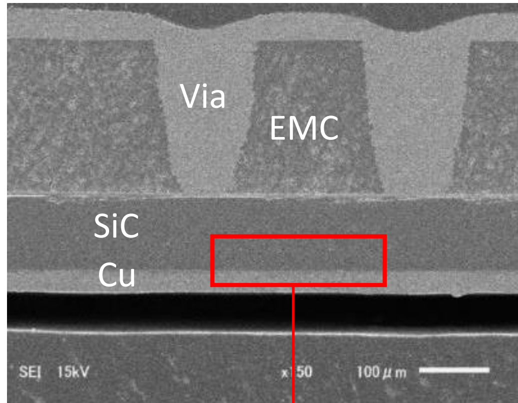
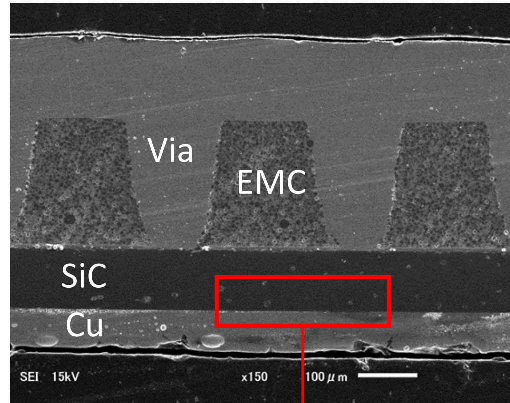
Previous Technical Developments

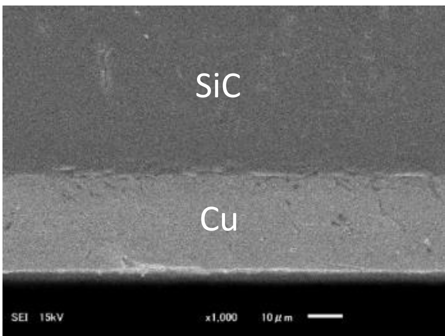
✓ ***TCT results for Direct Cu plated***

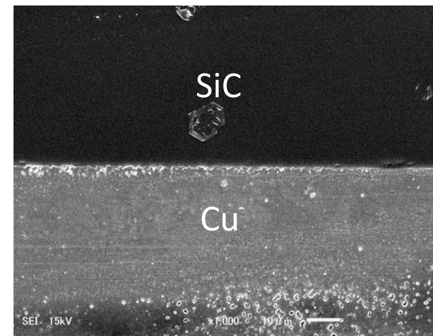
After 500cyc

After 1,000cyc







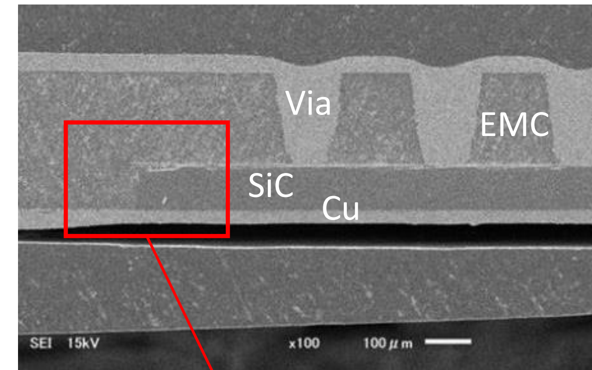


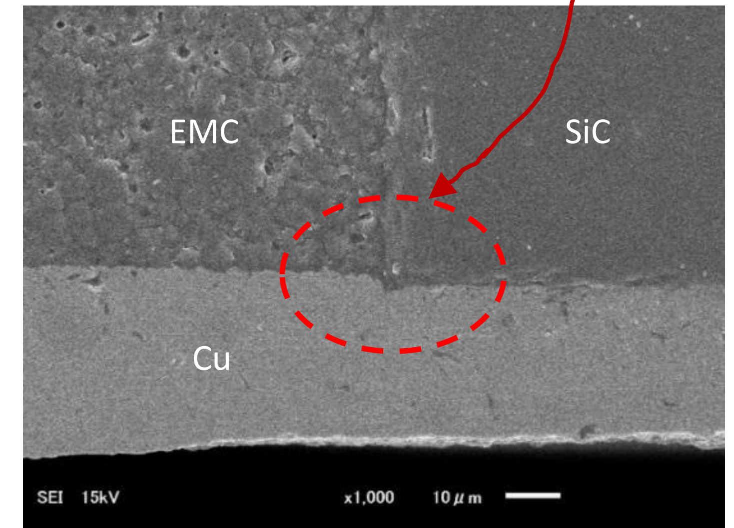
No delamination and cracking

More details analysis

Cross-sectional SEM after TCT 500cyc;

SiC chip-edge position (Highest stress area)





No delamination and cracking

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Newly Updated Our Technical Developments

Power Cycling Tests for direct Cu plated interconnect

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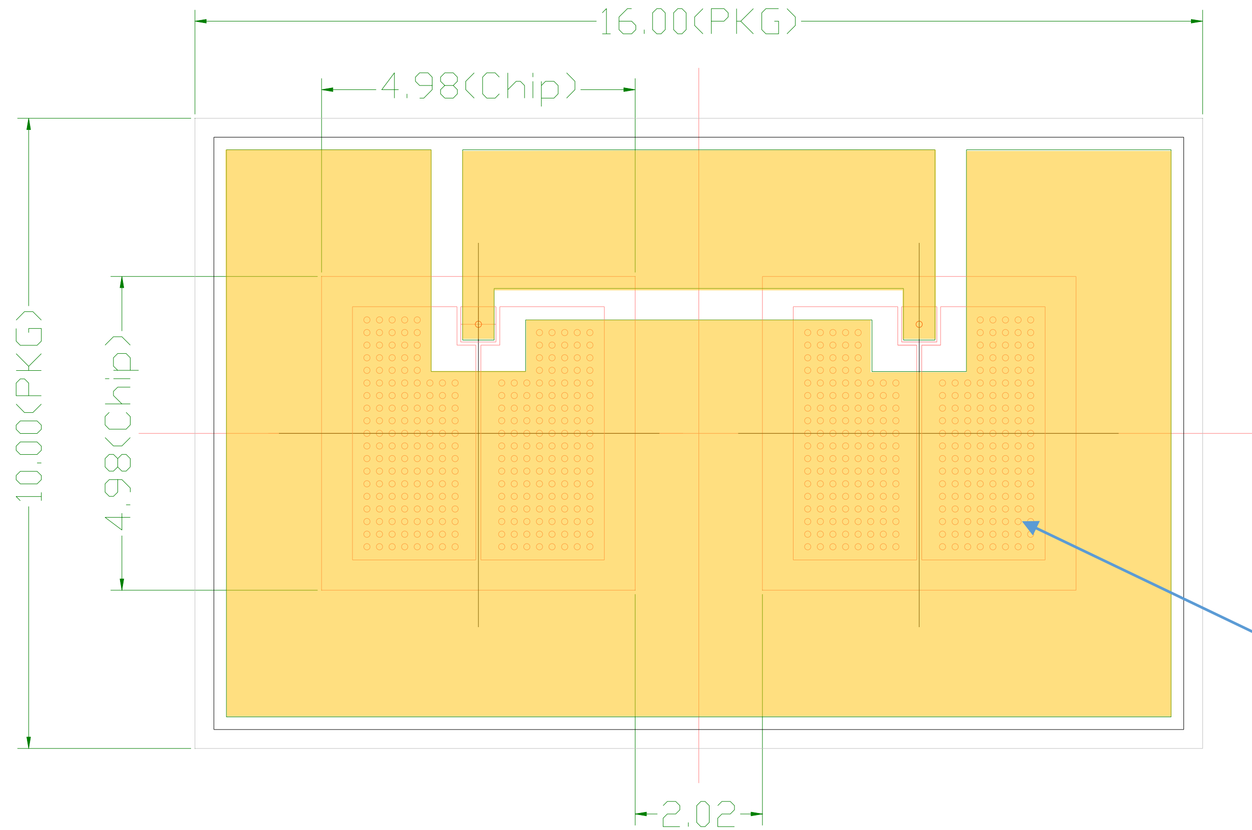
Prototyping

✓ ***Package design***



Si – IGBT
650V, 45A

Chip size
4.98×4.98mm

Chip thickness
90μm

2 chips in parallel

Via diameter 100μm

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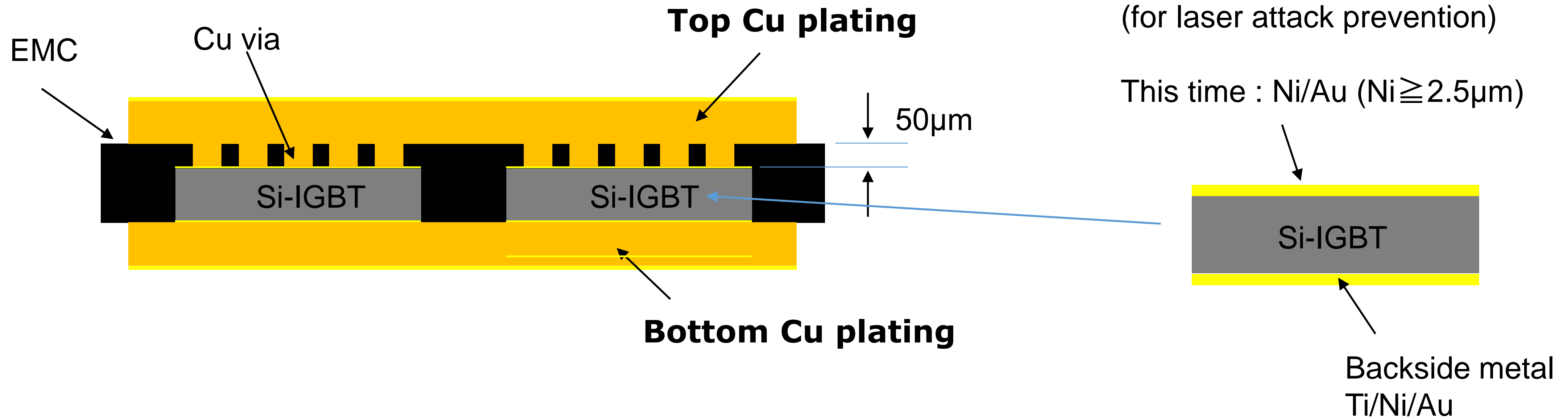
Prototyping

✓ ***Package vertical structure and dimensions***



Level No.	Cu plating thickness(μm)	
	Top Cu	Bottom Cu
A	100	100
B	200	200

※Trial level

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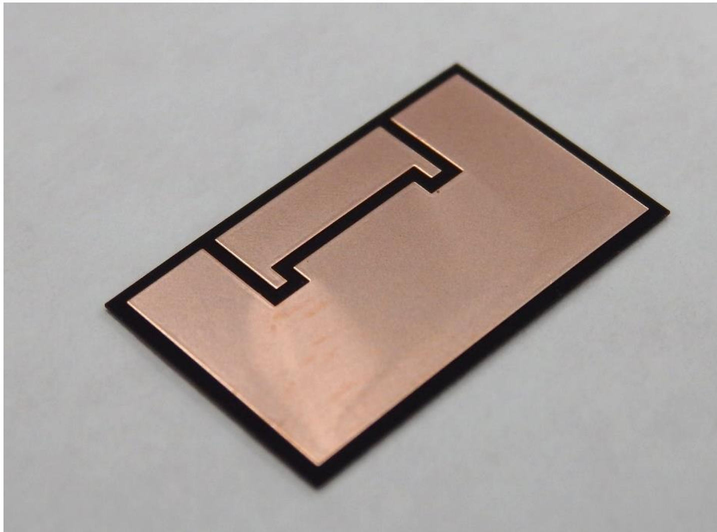
Prototyping

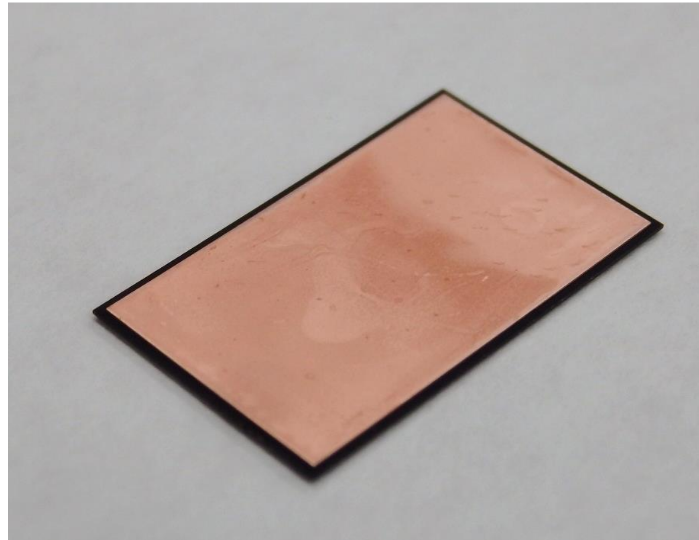
✓ ***Finished Prototype***

Package external image

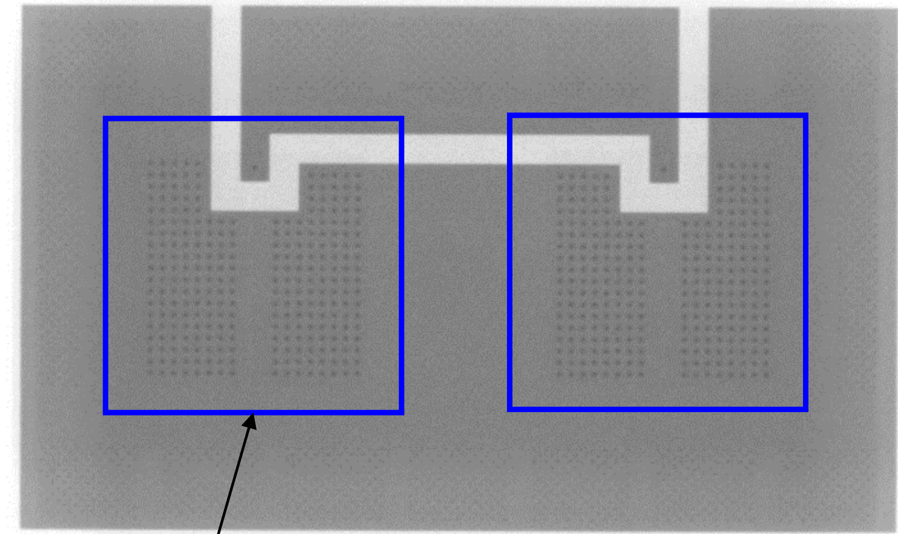
Top



Bottom



X-ray image



IGBT chip

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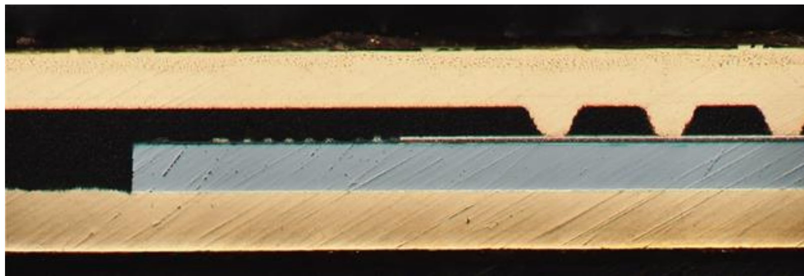
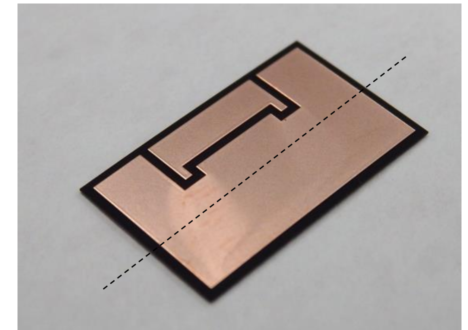
Prototyping

✓ ***Finished Prototype***

Cross-section image by microscope





Level No.	Cu plating thickness(μm)	
	Top Cu	Bottom Cu
A	100	100

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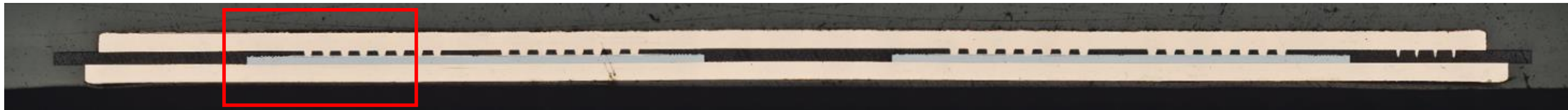
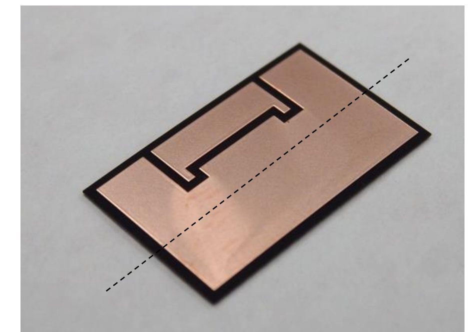
Prototyping

✓ ***Finished Prototype***

Cross-section image by microscope





Level No.	Cu plating thickness(μm)	
	Top Cu	Bottom Cu
B	200	200

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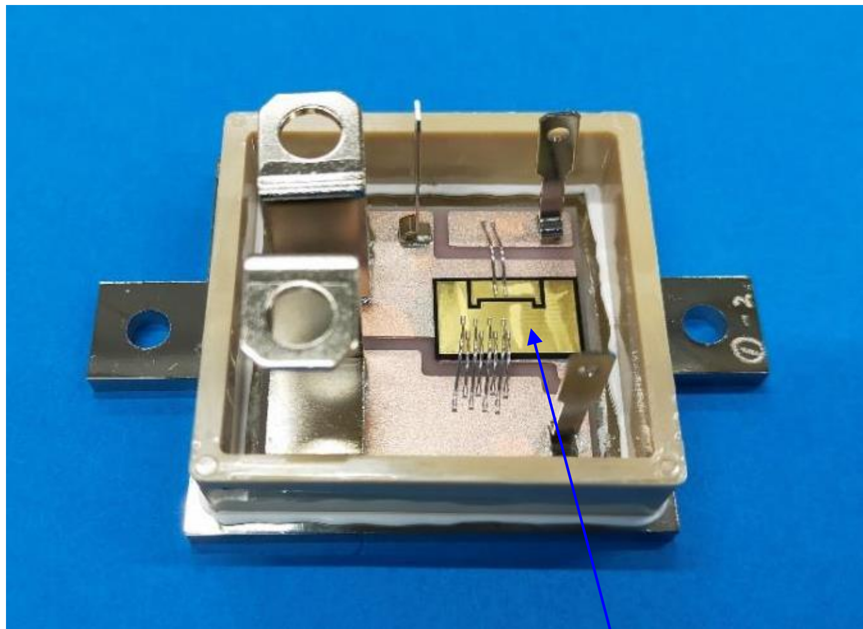
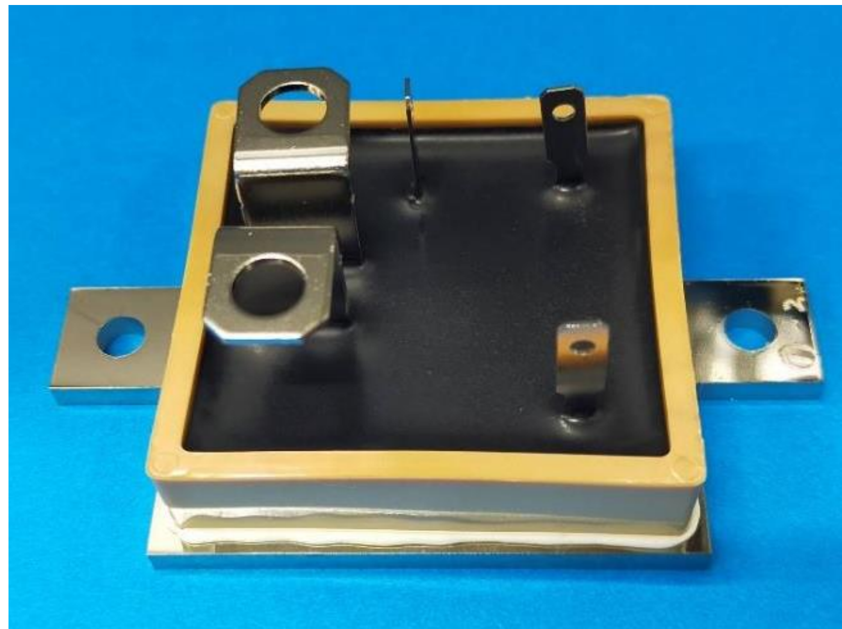
Power Cycling Test

✓ ***Power cycling test sample***

Before resin sealing

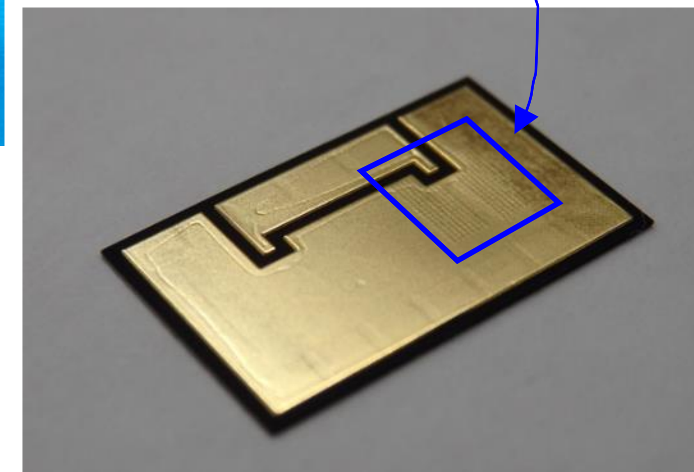


After resin sealing



Our sub-module in power module housing

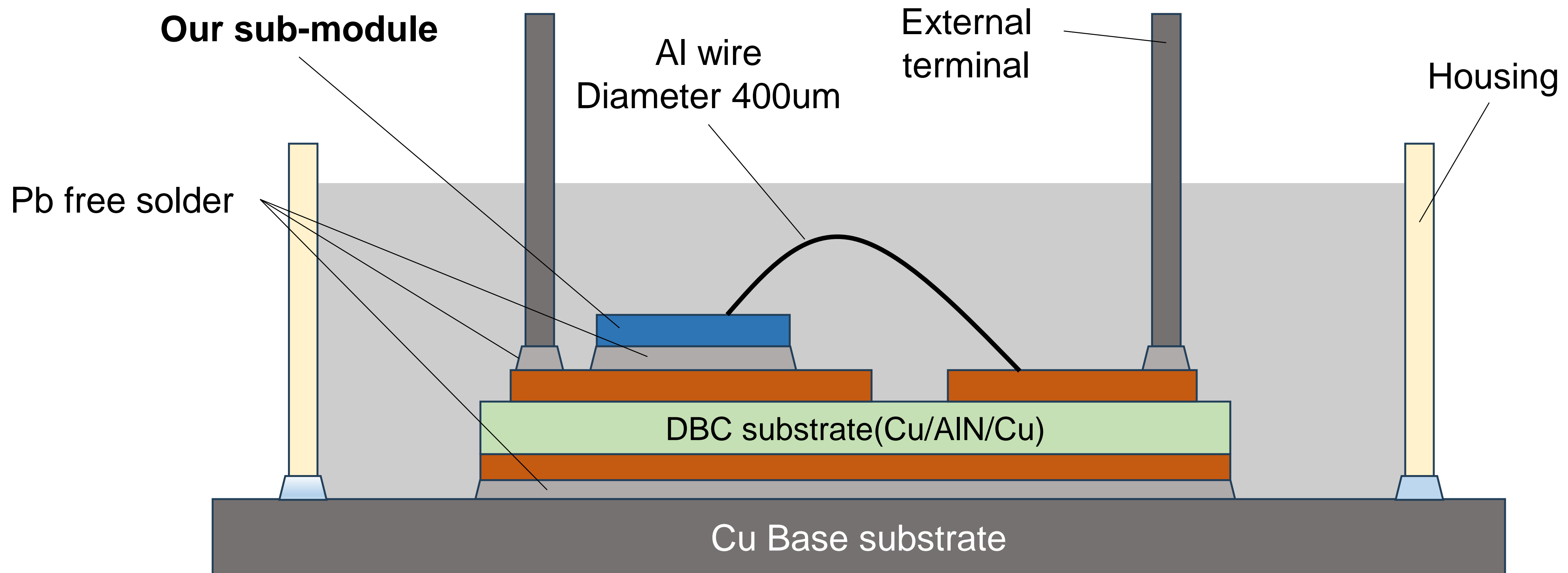
Using 1-chip sample



Power Cycling Test

- ✓ ***Power cycling test sample***

Cross-section structure



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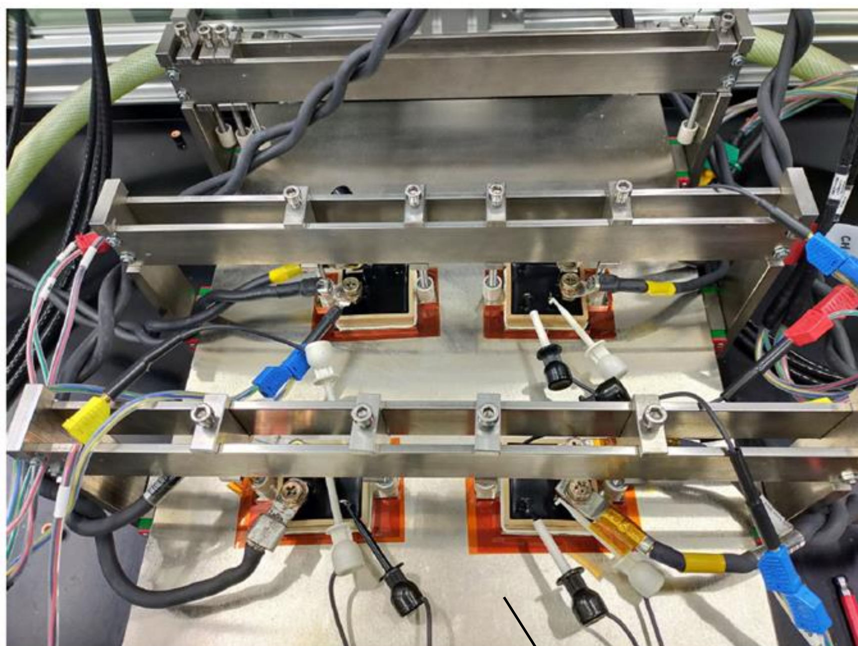
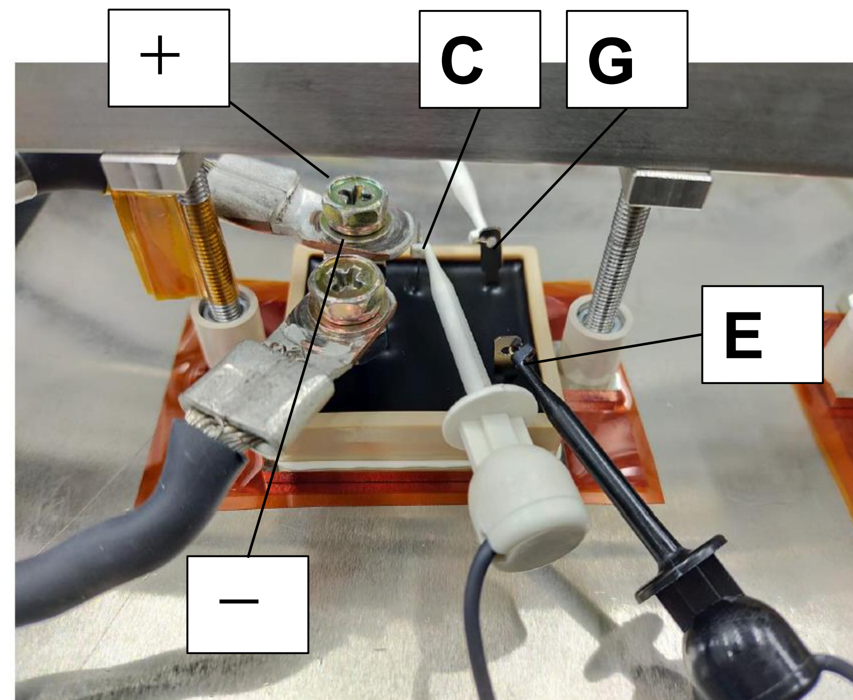
Power Cycling Test

✓ ***Power cycling test setup***



Cold plate



＋ : Input current
－ : Output current
C : Collector
E : Emitter
G :Gate

Outsourcing is used for testing (Chemitox, Japan)

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Power Cycling Test

✓ ***Test conditions***

Items	Conditions
Test mode	Current constant mode : 45A(Between C-E terminal)
Cold plate temperature	25℃
Number of Si-IGBT chips	1 chip
ΔTj	A sample : 75℃ B sample : 65℃
ON/OFF time	ON=10sec OFF=20sec
Number of cycles	13,000 cyc

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Power Cycling Test

✓ ***Judgment items***

Items	Remarks(means)
Tjmax	Maximum temperature of chip when ON
Tjmin	Minimum temperature of chip when OFF
ΔTj	Tjmax-Tjmin
Von	On-voltage at input current(45A)

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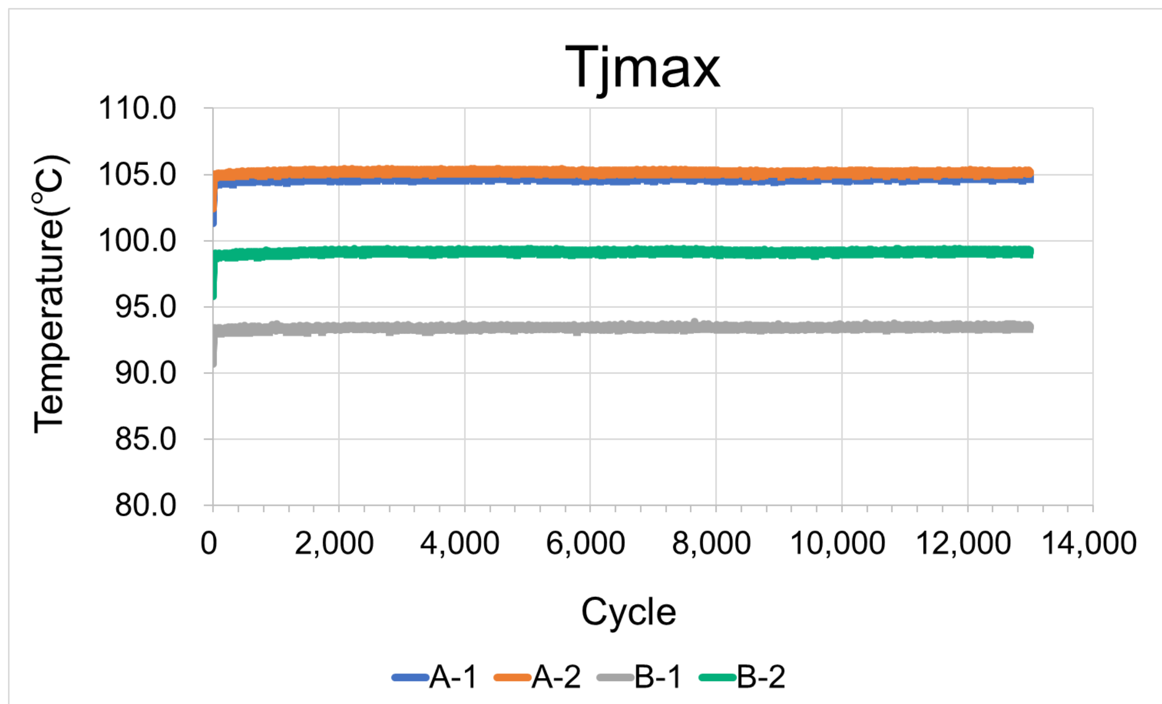
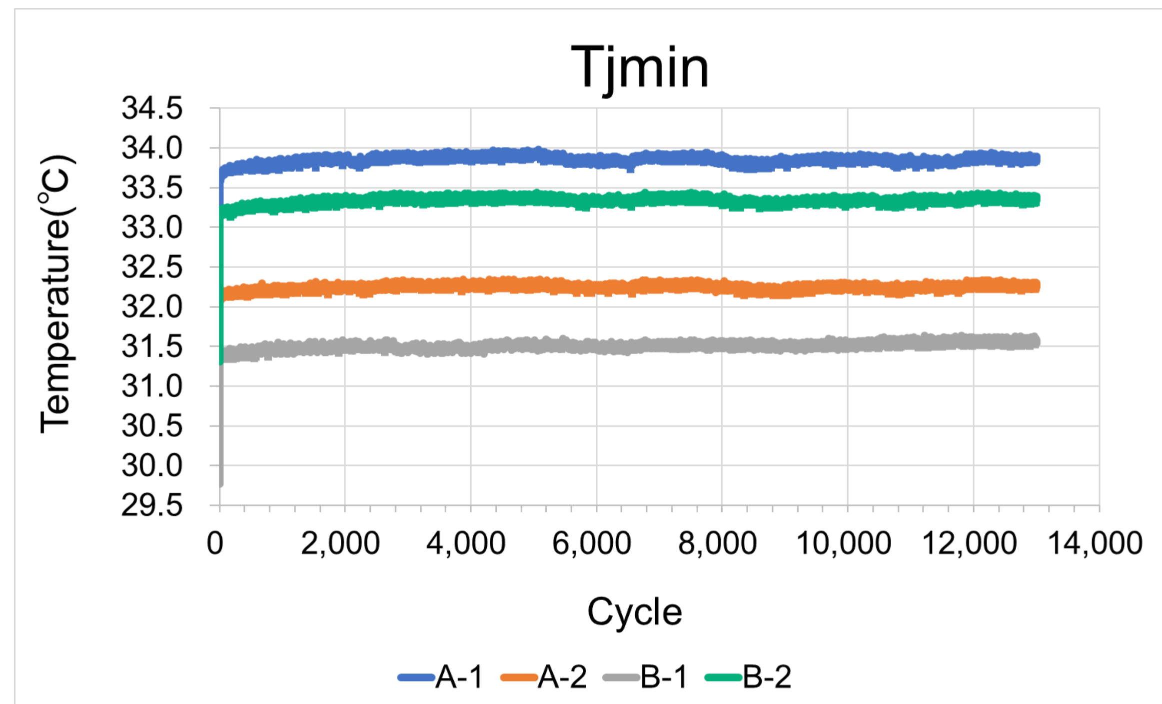
Power Cycling Test

✓ ***Power cycling test results***

Sample A:Cu thickness 100μm
Sample B:Cu thickness 200μm





No characteristic change after 13,000 cycles

Good results

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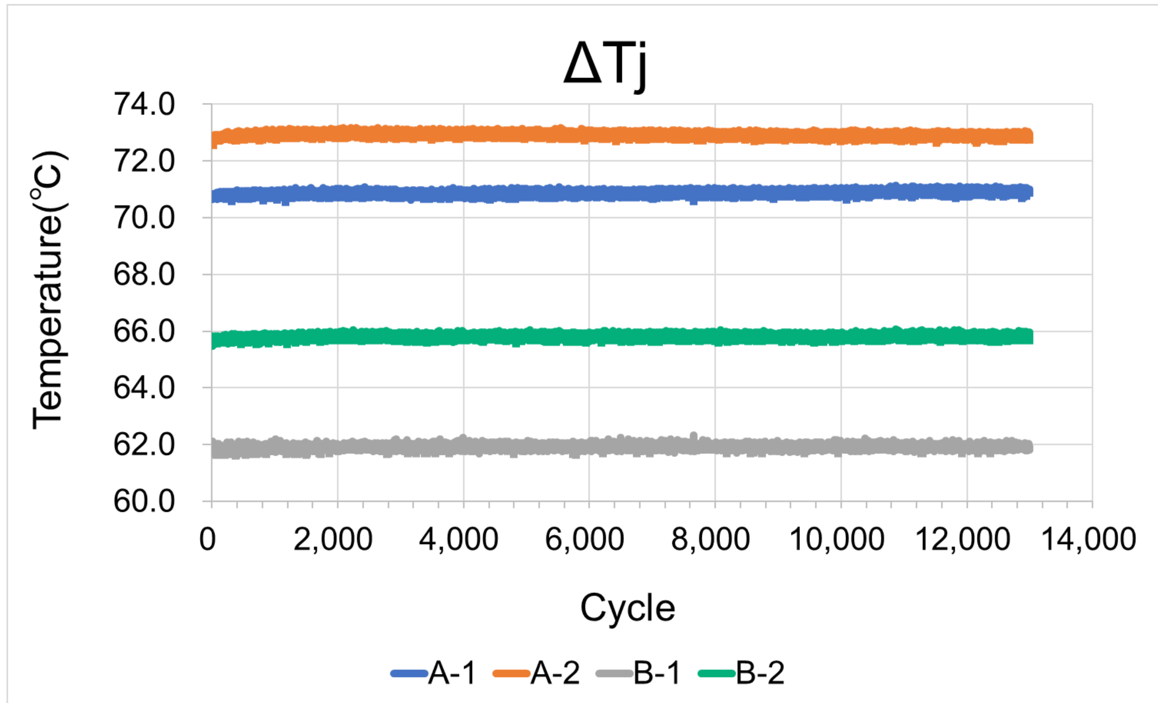
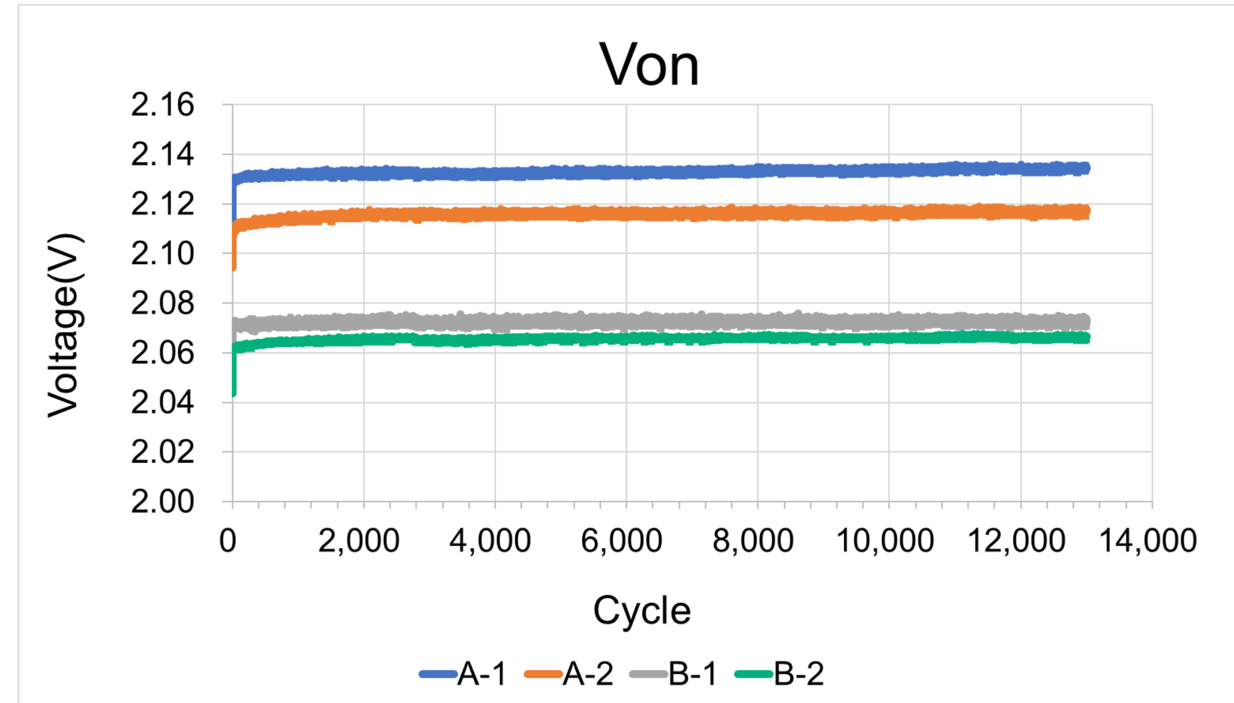
Power Cycling Test

✓ ***Power cycling test results***

Sample A:Cu thickness 100µm
Sample B:Cu thickness 200µm





No characteristic change after 13,000 cycles

Good results

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Summary

- ✓ We performed power cycling tests on Cu direct plated interconnections fabricated by a fan-out panel-level process.
- ✓ In this study, we examined the effect on connection reliability of different Cu thicknesses on the top and bottom of the chip.
- ✓ As a result of the power cycling test, we obtained good results with no change in any of the characteristics such as Tjmax, Tjmin and Von.
- ✓ In this study, we have obtained the possibility of direct connection with thick Cu to power chips.
  (100μm and 200μm thick Cu)
- ✓ As a next step, we plan to perform power cycling tests under higher current conditions (2-chip parallel Si-IGBTs).
- ✓ We also would like to evaluate TCT reliability testing at the board level(BLR).

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