M-Series™ Fan-out Interposer Technology (MFIT™)

with vertical interconnect blocks

Robin Davis – Sr. Director of Business Development

Benedict San Jose – Principal Materials, Process, & Integration Engineer

Outline

- Introduction
- MFIT Process Flow Overview
- MFIT Process Flow Details
- Conclusion

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Introduction

Why fanout interposers?

AI & HPC Driving Multi-Chip Integration

- AI & HPC require multiple processors & HBM for high-speed computing
- Fine-line RDL enables chiplet architectures but increases defect risk
- Fan-out interposers provide scalable, cost-effective integration

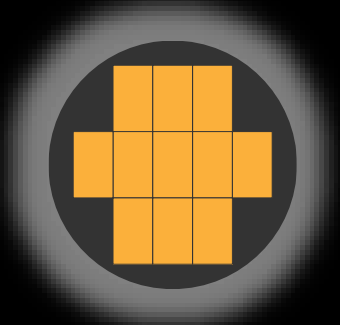
Fan-out vs. Si Interposers

- No TSVs required ⟶ Lower cost, simpler manufacturing
- RDL with polyimide (PI) improves signal integrity over silicon passivation
- HVM in 300mm wafer today - ⟶ roadmap to 600mm large panels

Reducing Defect Risk & Improving Yield

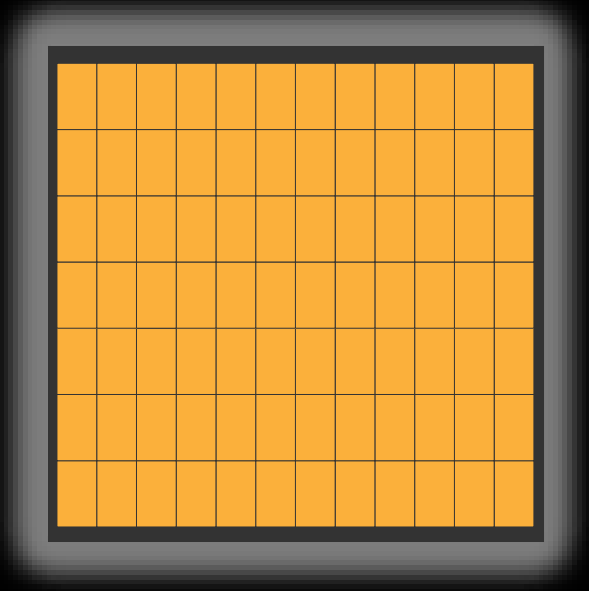
- Fine-line, high-density RDL requirements (UCIe, HBM3 & 4) increase yield risk
- Chip-first RDL embeds expensive processors too early ⟶ High risk
- Fan-out interposers enable known-good RDL bridge dies ⟶ Higher yield, lower risk

48mm x 80mm interposer
on 300mm wafer



60% area efficiency*
11 packages

on 600mm panel



90% area efficiency*
84 packages

*Ratio of total package area ÷ total panel area

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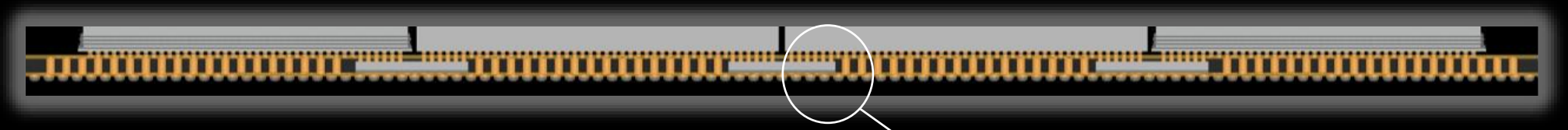
Introduction

What is M-Series Fan-out Interposer (MFIT) Technology?



Molded fan-out interposer with embedded components

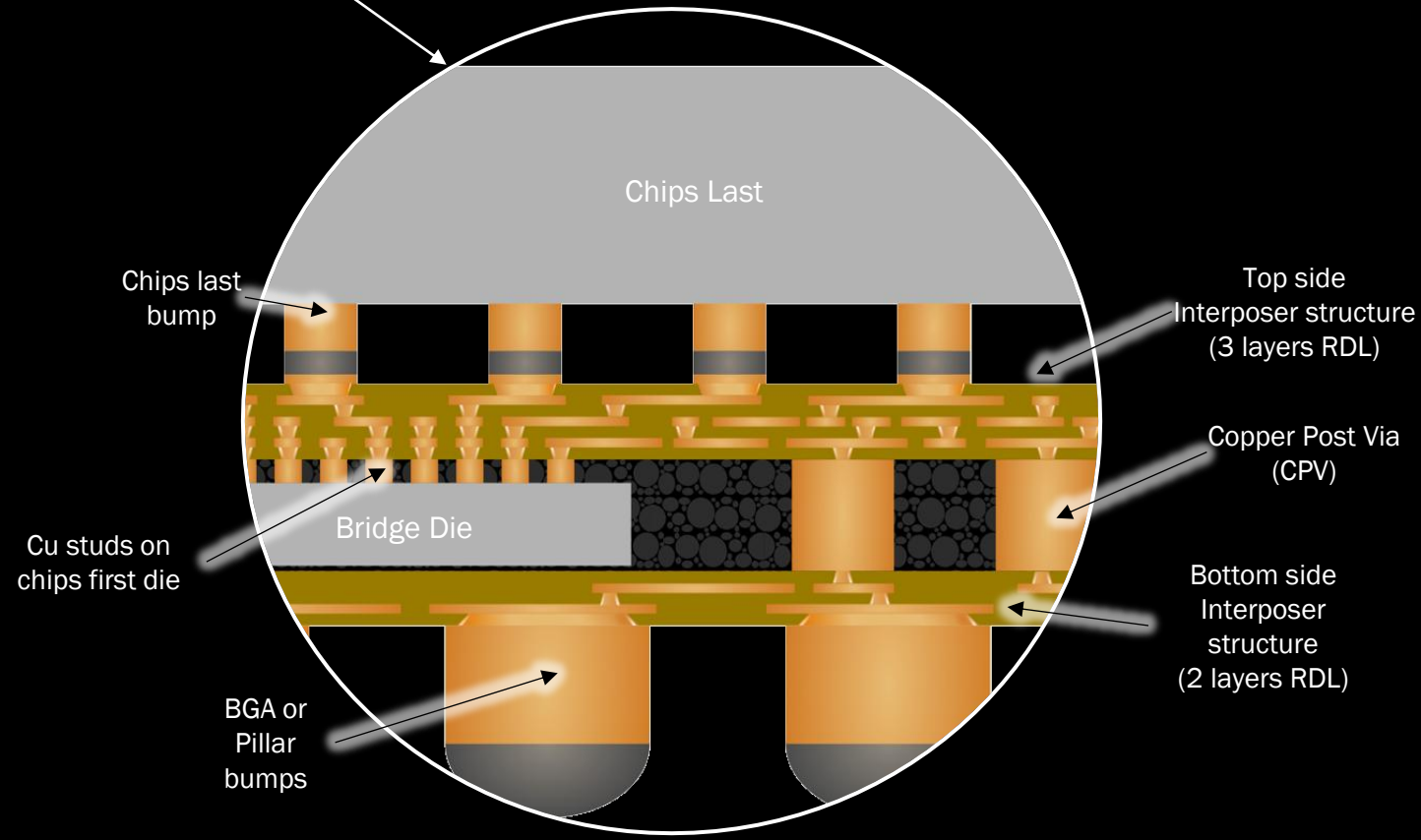
- Bridge die
- IPDs *(such as DTCs)*
- Active devices

Through Mold Interconnects

- Molded copper vias (MCVs)

  - OR -

- Vertical interconnect blocks (pre-fabricated and placed like other components)



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Multiple patents issued and pending

Outline

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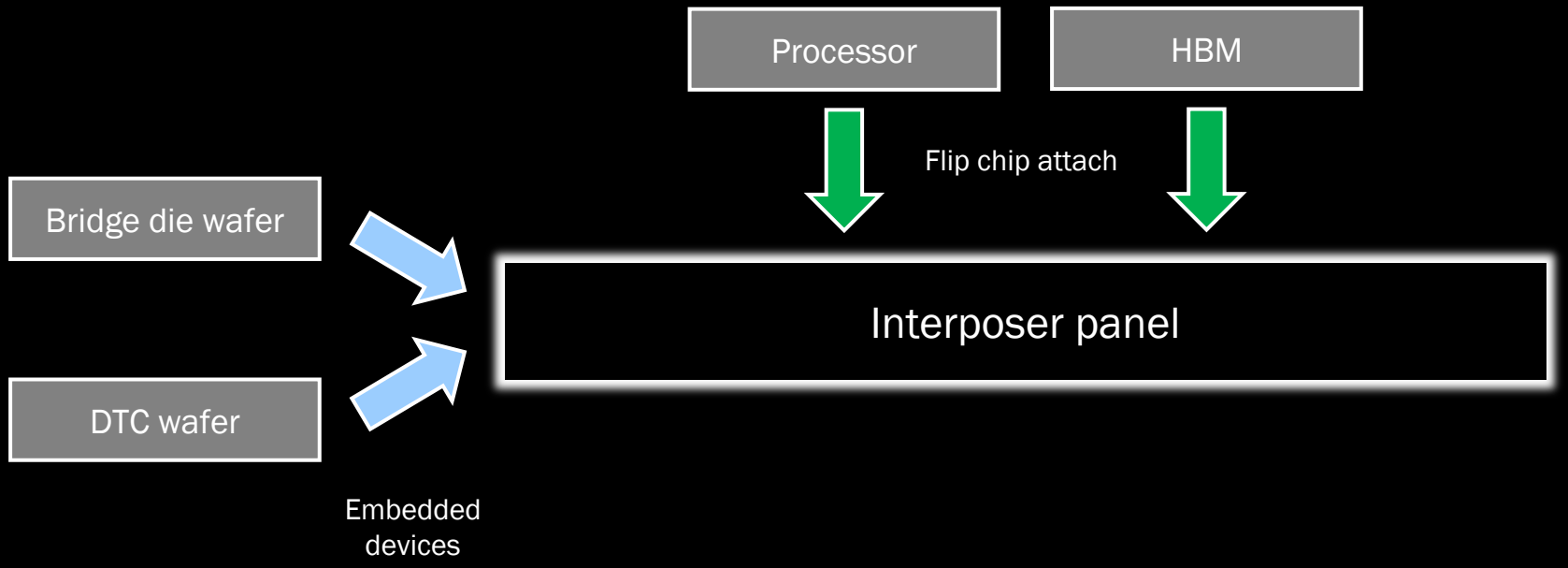
MFIT Process Flow Overview

Simple Schematic Overview



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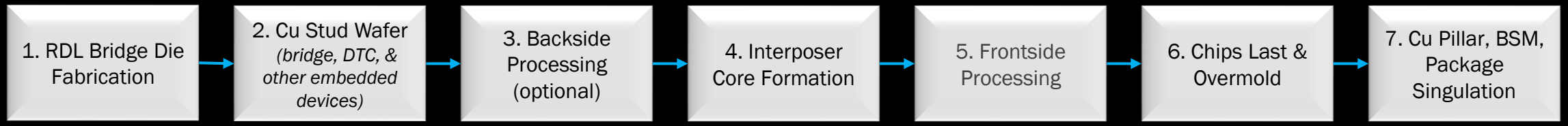
MFIT Process Flow

High Level Flow



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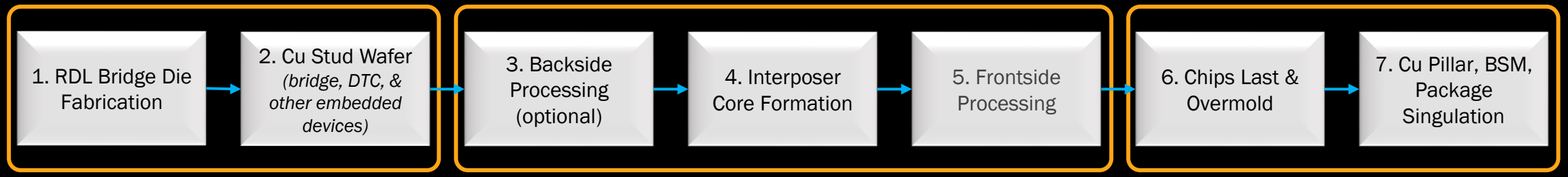
MFIT Process Flow

High Level Flow



Embedded components

Interposer

Chips last and finishing

Two process flows:

1. Glass carrier flow
2. Full thickness flow

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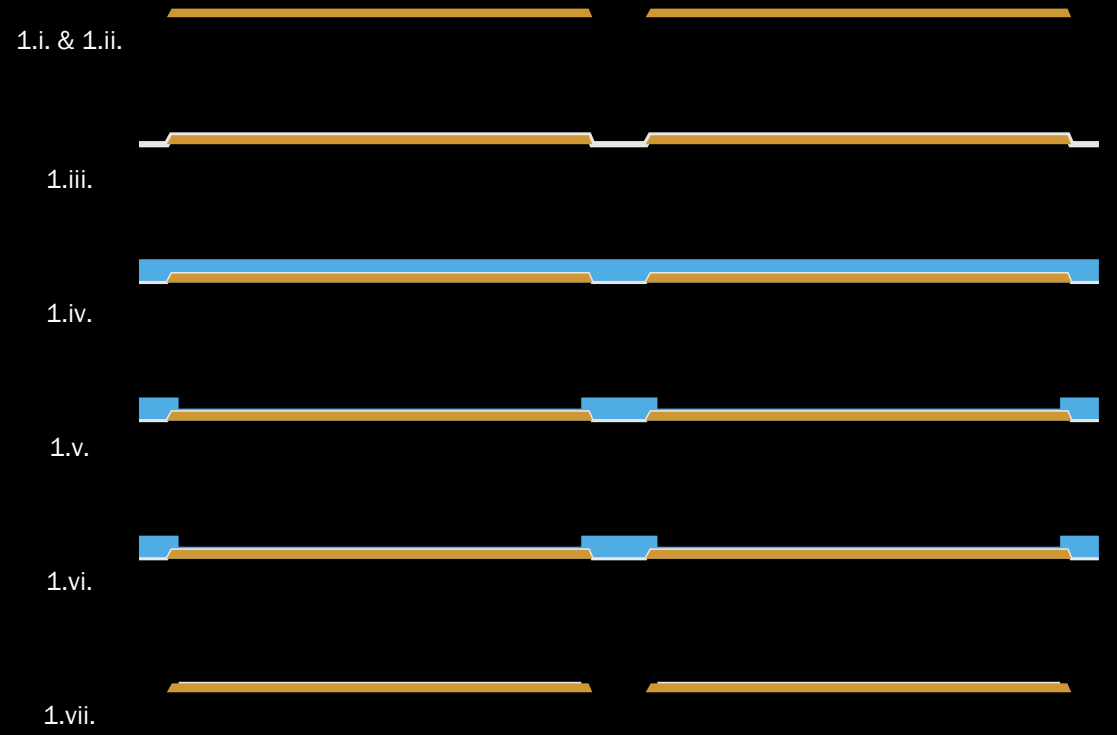
MFIT Process Flow

Embedded Components

1. RDL Bridge Die Fabrication → 2. Cu Stud Wafer (bridge, DTC, & other embedded devices) → 3. Backside Processing (optional) → 4. Interposer Core Formation → 5. Frontside Processing → 6. Chips Last & Overmold → 7. Cu Pillar, BSM, Package Singulation

1.

- i. PI Coat, Expose & Develop
- ii. Cure & Descum
- iii. Seed PVD
- iv. RDL Photoresist
- v. PR Expose & Dev
- vi. RDL Cu Plating
- vii. PR Strip & Etch
- viii. PCM Test
- ix. 100% AOI - RDL



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MFIT Process Flow

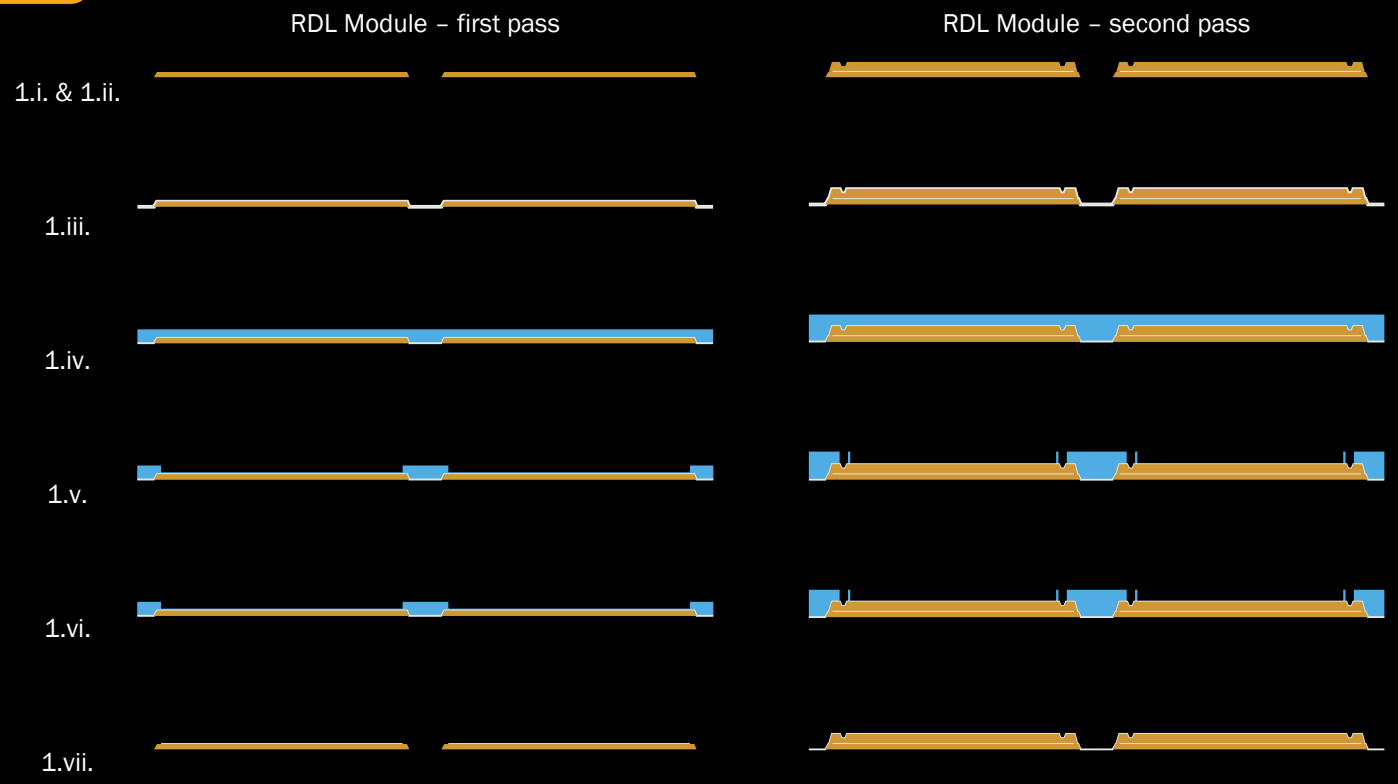
Embedded Components

1. RDL Bridge Die Fabrication → 2. Cu Stud Wafer (bridge, DTC, & other embedded devices) → 3. Backside Processing (optional) → 4. Interposer Core Formation → 5. Frontside Processing → 6. Chips Last, Overmold, Glass Carrier 2 → 7. Cu Pillar, BSM, Package Singulation

1.

RDL Module
repeat for all RDL layers

- i. PI Coat, Expose & Develop
- ii. Cure & Descum
- iii. Seed PVD
- iv. RDL Photoresist
- v. PR Expose & Dev
- vi. RDL Cu Plating
- vii. PR Strip & Etch
- viii. PCM Test
- ix. 100% AOI - RDL



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MFIT Process Flow

Embedded Components

1. RDL Bridge Die Fabrication
2. Cu Stud Wafer (bridge, DTC, & other embedded devices)
3. Backside Processing (optional)
4. Interposer Core Formation
5. Frontside Processing
6. Chips Last & Overmold
7. Cu Pillar, BSM, Package Singulation

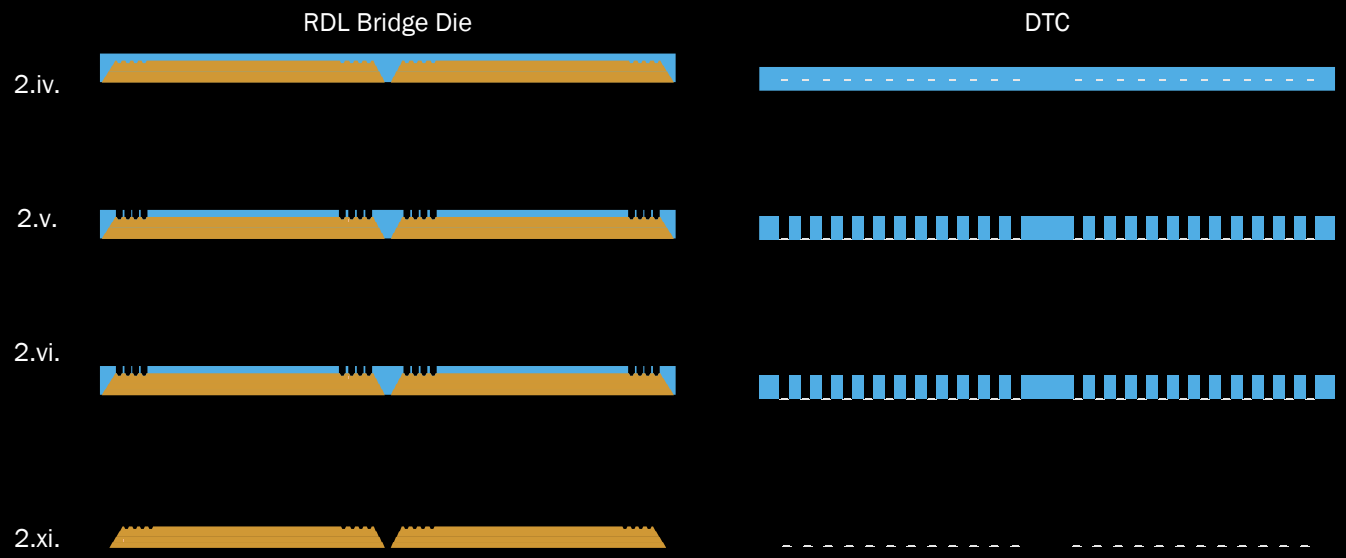
1.

RDL Module
repeat for all RDL layers

- i. PI Coat, Expose & Develop
- ii. Cure & Descum
- iii. Seed PVD
- iv. RDL Photoresist
- v. PR Expose & Dev
- vi. RDL Cu Plating
- vii. PR Strip & Etch
- viii. PCM Test
- ix. 100% AOI - RDL

2.

- i. PI Coat, Expose & Develop
- ii. Cure & Descum
- iii. Seed PVD
- iv. Thick Photoresist
- v. Expose & Develop
- vi. Cu Stud Plating
- vii. Strip & Etch
- viii. Electrical Continuity Test
- ix. 100% AOI - RDL + Cu Stud
- x. Wafer Backgrind
- xi. Wafer Saw



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MFIT Process Flow

Embedded Components

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repeat for all RDL layers

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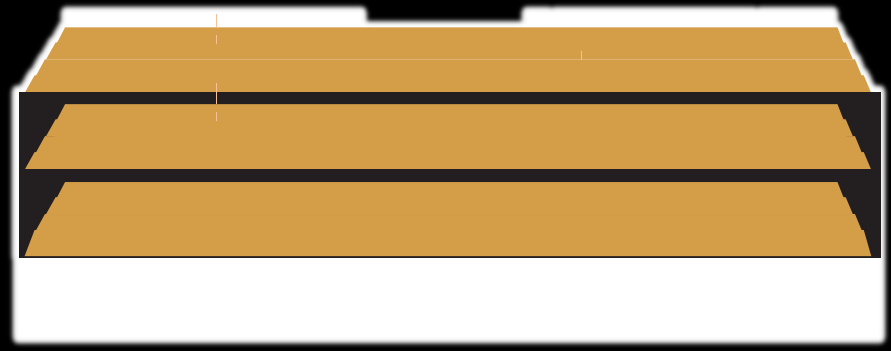
- ii. Cure & Descum
- iii. Seed PVD
- iv. RDL Photoresist
- v. PR Expose & Dev
- vi. RDL Cu Plating
- vii. PR Strip & Etch
- viii. PCM Test
- ix. 100% AOI - RDL

MDx Planarization Layer (optional)

2.

- i. PI Coat, Expose & Develop
- ii. Cure & Descum
- iii. Seed PVD
- iv. Thick Photoresist
- v. Expose & Develop
- vi. Cu Stud Plating
- vii. Strip & Etch
- viii. Electrical Continuity Test
- ix. 100% AOI - RDL + Cu Stud
- x. Wafer Backgrind
- xi. Wafer Saw

RDL Bridge Die



RDL Bridge Die
(with optional MDx layers)

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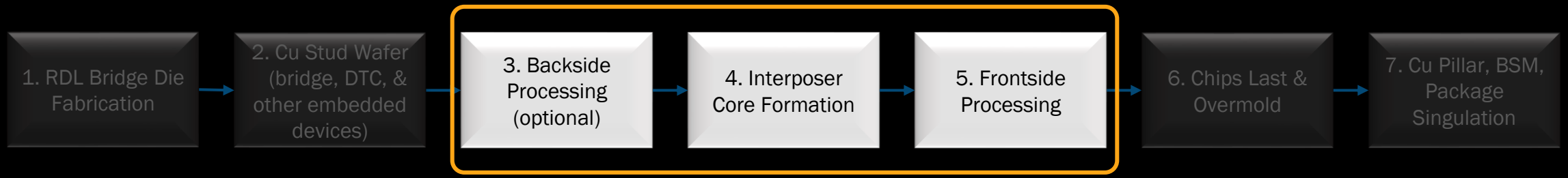
MFIT Process Flow

Interposer



Interposer

Two process flows:

1. Glass carrier flow
2. Full thickness flow

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MFIT Process Flow - #1 Glass Carrier

Interposer

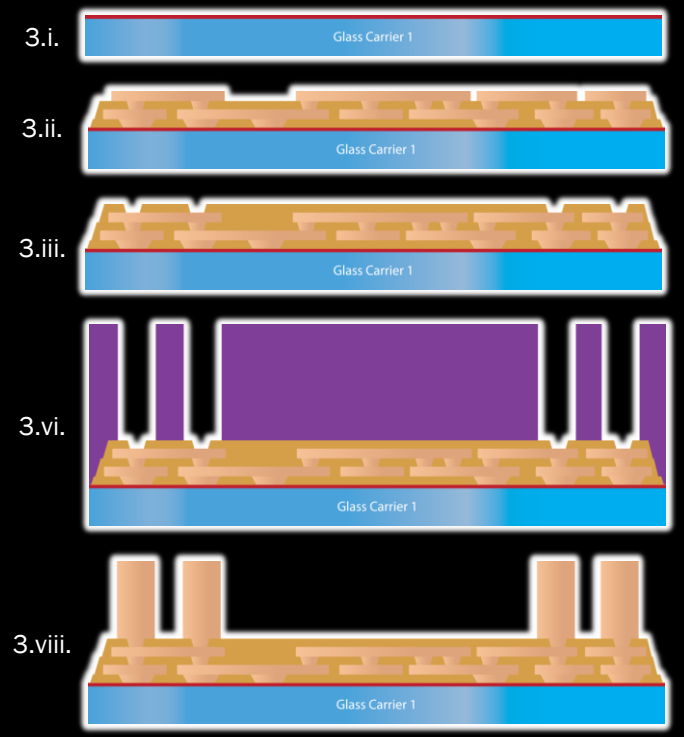
1. RDL Bridge Die Fabrication → 2. Cu Stud Wafer (bridge, DTC, & other embedded devices) → **3. Backside Processing (optional)** → 4. Interposer Core Formation → 5. Frontside Processing → 6. Chips Last & Overmold → 7. Cu Pillar, BSM, Package Singulation

RDL Module
repeat for all RDL layers

- PI Coat, Expose & Develop
- Cure & Descum
- Seed PVD
- RDL Photoresist
- PR Expose & Dev
- RDL Cu Plating
- PR Strip & Etch
- PCM Test
- AOI - RDL

3.

- i. Glass Carrier 1 + LRL
- **ii. RDL Module** repeat for all RDL layers
- iii. PI Coat, Expose, Develop, Descum, Cure
- iv. CPV Seed PVD
- v. CPV Photoresist
- vi. CPV Expose & Dev
- vii. CPV Plating
- viii. CPV PR Strip & Etch
- ix. PCM Test
- x. AOI – CPV



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MFIT Process Flow - #1 Glass Carrier

Interposer

1. RDL Bridge Die Fabrication → 2. Cu Stud Wafer (bridge, DTC, & other embedded devices) → 3. Backside Processing (optional) → 4. Interposer Core Formation → 5. Frontside Processing → 6. Chips Last & Overmold → 7. Cu Pillar, BSM, Package Singulation

RDL Module
repeat for all RDL layers

- PI Coat, Expose & Develop
- Cure & Descum
- Seed PVD
- RDL Photoresist
- PR Expose & Dev
- RDL Cu Plating
- PR Strip & Etch
- PCM Test
- AOI - RDL

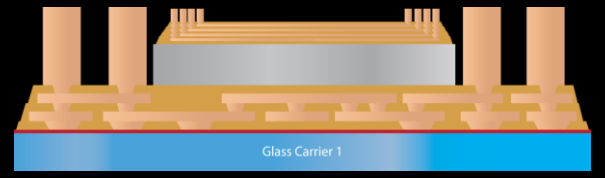
3.

- i. Glass Carrier 1 + LRL
- **ii. RDL Module** repeat for all RDL layers
- iii. PI Coat, Expose, Develop, Descum, Cure
- iv. CPV Seed PVD
- v. CPV Photoresist
- vi. CPV Expose & Dev
- vii. CPV Plating
- viii. CPV PR Strip & Etch
- ix. PCM Test
- x. AOI – CPV

4.

- i. Die Attach (bridge & DTC)
- ii. Cure
- iii. Molding
- iv. Post Mold Cure
- v. Front Planarization
- vi. Cu Clean
- vii. AOI
- Die Measurement
- GDS File Creation

4.i.



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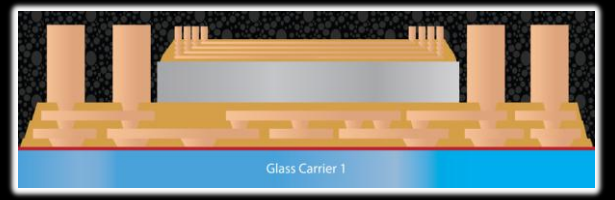

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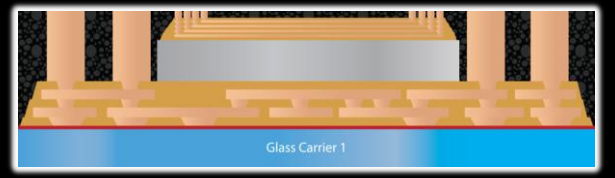

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MFIT Process Flow - #1 Glass Carrier

Interposer

1. RDL Bridge Die Fabrication → 2. Cu Stud Wafer (bridge, DTC, & other embedded devices) → 3. Backside Processing (optional) → 4. Interposer Core Formation → 5. Frontside Processing → 6. Chips Last & Overmold → 7. Cu Pillar, BSM, Package Singulation

RDL Module
repeat for all RDL layers

- PI Coat, Expose & Develop
- Cure & Descum
- Seed PVD
- RDL Photoresist
- PR Expose & Dev
- RDL Cu Plating
- PR Strip & Etch
- PCM Test
- AOI - RDL

3.

- i. Glass Carrier 1 + LRL
- **ii. RDL Module** repeat for all RDL layers
- iii. PI Coat, Expose, Develop, Descum, Cure
- iv. CPV Seed PVD
- v. CPV Photoresist
- vi. CPV Expose & Dev
- vii. CPV Plating
- viii. CPV PR Strip & Etch
- ix. PCM Test
- x. AOI – CPV

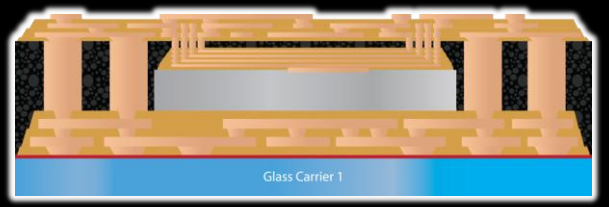
4.

- i. Die Attach (bridge & DTC)
- ii. Cure
- iii. Molding
- iv. Post Mold Cure
- v. Front Planarization
- vi. Cu Clean
- vii. AOI
- Die Measurement
- GDS File Creation

5.

- **i. RDL Module** repeat for all RDL layers
- ii. PI Coat, Expose, Develop, Descum, Cure
- iii. Seed PVD
- iv. µpad PR Lamination
- v. PR Expose & Dev
- vi. µpad Plating
- vii. PR Strip & Etch
- viii. Daisy chain test
- ix. AOI - µpad

5.i.



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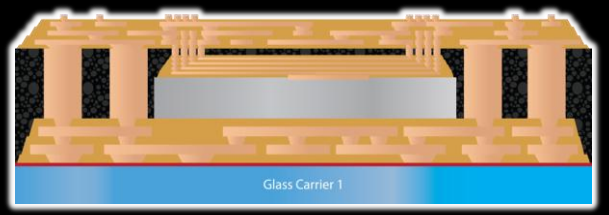

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MFIT Process Flow - #2 Full Thickness

Interposer

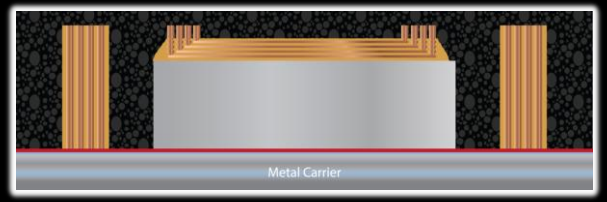
1. RDL Bridge Die Fabrication → 2. Cu Stud Wafer (bridge, DTC, & other embedded devices) → 3. Backside Processing (optional) → **4. Interposer Core Formation** → 5. Frontside Processing → 6. Chips Last & Overmold → 7. Cu Pillar, BSM, Package Singulation

4.

- i. Die Attach (bridge, DTC, VIB)
- ii. Molding
- iii. Post Mold Cure
- iv. Carrier debond
- v. Front Planarization
- vi. Cu Clean
- vii. AOI
- Die Measurement
- GDS File Creation

4.i.

4.iii.



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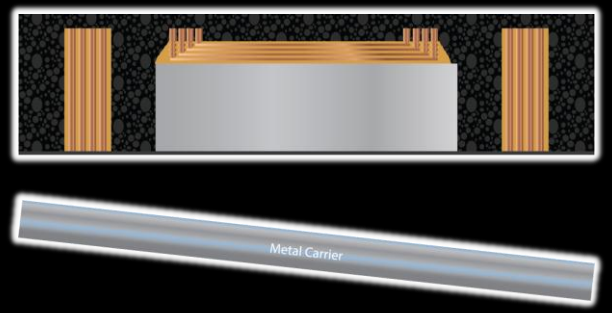

4.v.

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MFIT Process Flow - #2 Full Thickness

Interposer

1. RDL Bridge Die Fabrication → 2. Cu Stud Wafer (bridge, DTC, & other embedded devices) → 3. Backside Processing (optional) → 4. Interposer Core Formation → 5. Frontside Processing → 6. Chips Last & Overmold → 7. Cu Pillar, BSM, Package Singulation

RDL Module
repeat for all RDL layers

- PI Coat, Expose & Develop
- Cure & Descum
- Seed PVD
- RDL Photoresist
- PR Expose & Dev
- RDL Cu Plating
- PR Strip & Etch
- PCM Test
- AOI - RDL

4.

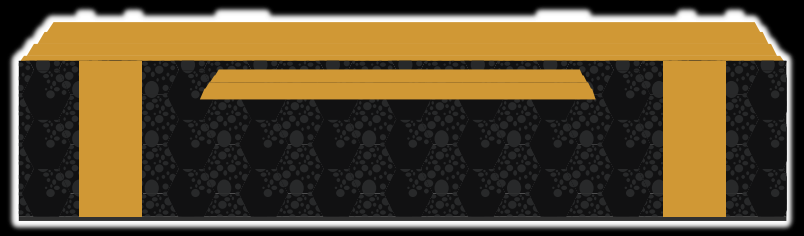
- i. Die Attach (bridge, DTC, VIB)
- ii. Molding
- iii. Post Mold Cure
- iv. Carrier debond
- v. Front Planarization
- vi. Cu Clean
- vii. AOI
- Die Measurement
- GDS File Creation

5.

i. RDL Module
repeat for all RDL layers

- ii. PI Coat, Expose, Develop, Descum, Cure
- iii. Seed PVD
- iv. µpad PR Lamination
- v. PR Expose & Dev
- vi. µpad Plating
- vii. PR Strip & Etch
- viii. Daisy chain test
- ix. AOI - µpad

5.vii.



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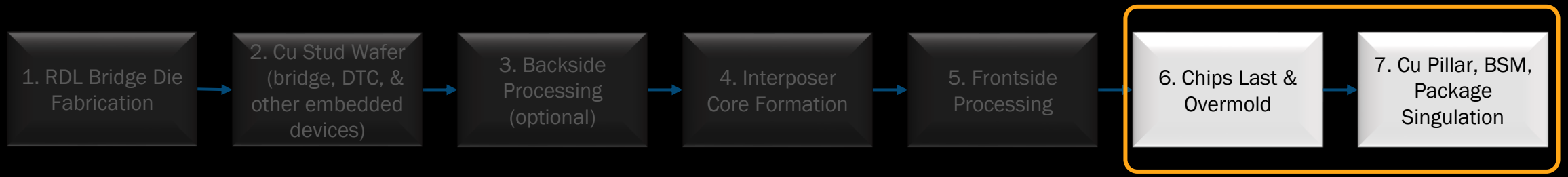
MFIT Process Flow

Chips Last & Finishing



Chips last and finishing

Two process flows:

1. Glass carrier flow
2. Full thickness flow

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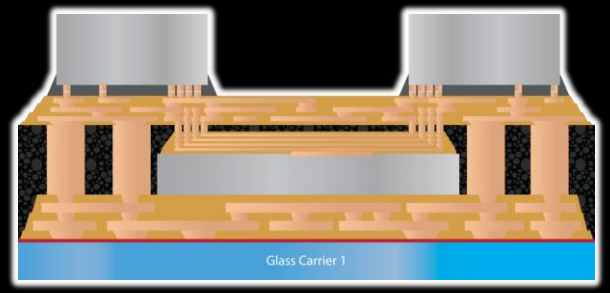
Multiple patents issued and pending

MFIT Process Flow - #1 Glass Carrier

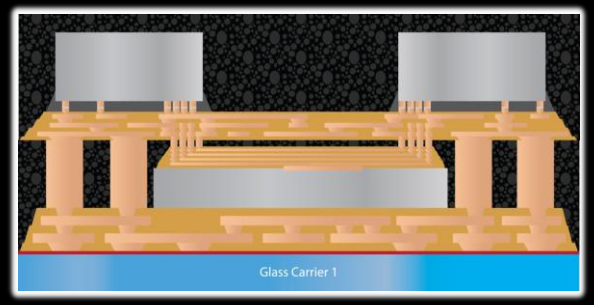
Chips Last & Finishing

1. RDL Bridge Die Fabrication → 2. Cu Stud Wafer (bridge, DTC, & other embedded devices) → 3. Backside Processing (optional) → 4. Interposer Core Formation → 5. Frontside Processing → **6. Chips Last & Overmold** → 7. Cu Pillar, BSM, Package Singulation

6.iii.



6.v.



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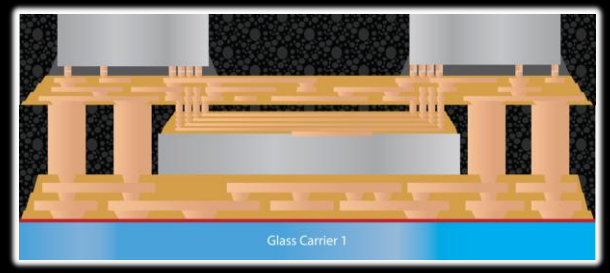

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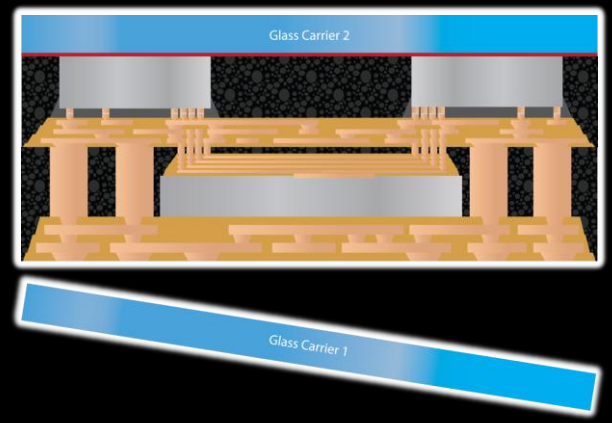

6.

- i. Chips Last FC bonding
- ii. Module level test
- iii. Die Underfill
- iv. Cure
- v. Mold
- vi. Cure
- vii. Backgrind
- viii. Marking
- ix. AOI
- x. Glass Carrier 2 Bond
- xi. Glass Carrier 1 Debond
- xii. Clean

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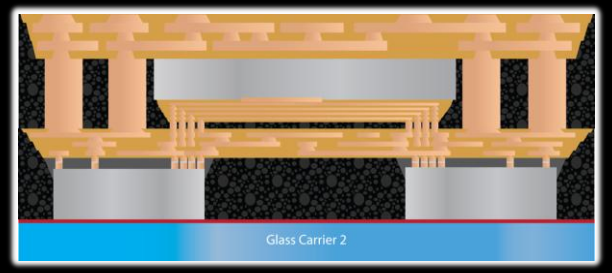
MFIT Process Flow - #1 Glass Carrier

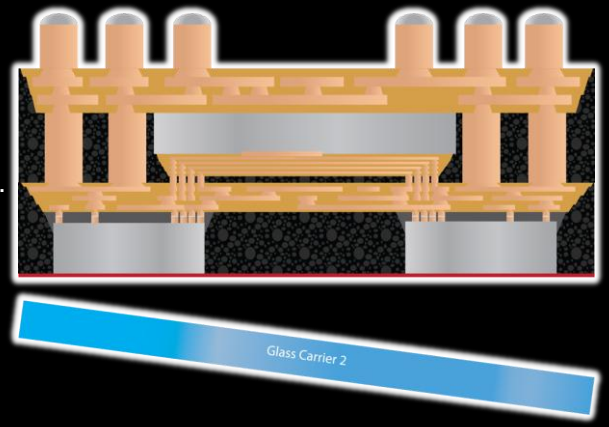
Chips Last & Finishing

1. RDL Bridge Die Fabrication → 2. Cu Stud Wafer (bridge, DTC, & other embedded devices) → 3. Backside Processing (optional) → 4. Interposer Core Formation → 5. Frontside Processing → 6. Chips Last & Overmold → 7. Cu Pillar, BSM, Package Singulation

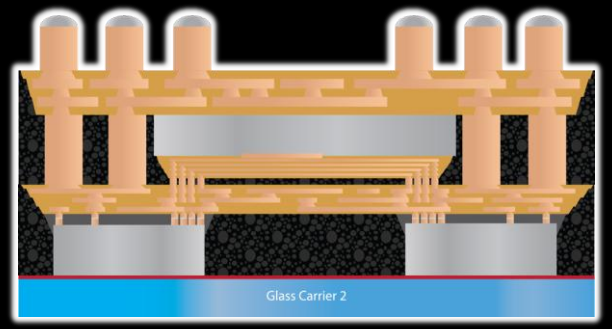
6.xi.



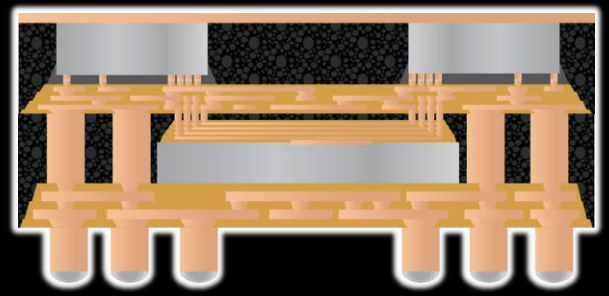
7.viii.



7.vi.



7.ix.



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- i. Chips Last FC bonding
- ii. Module level test
- iii. Die Underfill
- iv. Cure
- v. Mold
- vi. Cure
- vii. Backgrind
- viii. Marking
- ix. AOI
- x. Glass Carrier 2 Bond
- xi. Glass Carrier 1 Debond
- xii. Clean

7.
- i. UBM Seed PVD
- ii. UBM Photoresist
- iii. Expose & Dev
- iv. Cu Pillar Plating
- v. Strip & Etch
- vi. Reflow
- vii. AOI
- viii. Glass Carrier 2 Debond
- ix. Optional backside metal
- x. Proceed to substrate mounting
- xi. System level test

Ship Out

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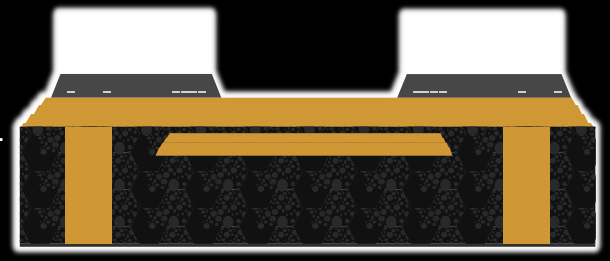
MFIT Process Flow - #2 Full Thickness

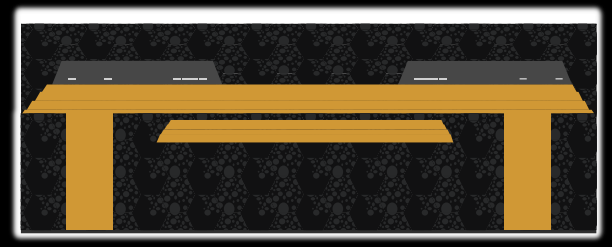
Chips Last & Finishing

1. RDL Bridge Die Fabrication → 2. Cu Stud Wafer (bridge, DTC, & other embedded devices) → 3. Backside Processing (optional) → 4. Interposer Core Formation → 5. Frontside Processing → **6. Chips Last & Overmold** → **7. Cu Pillar, BSM, Package Singulation**

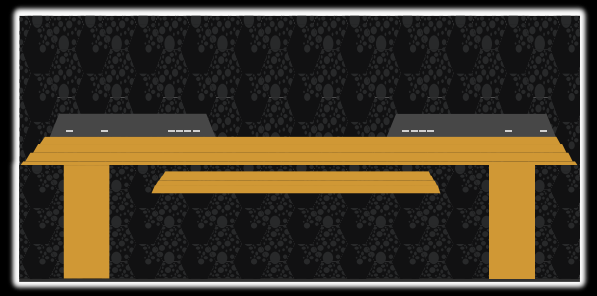
6.iii.



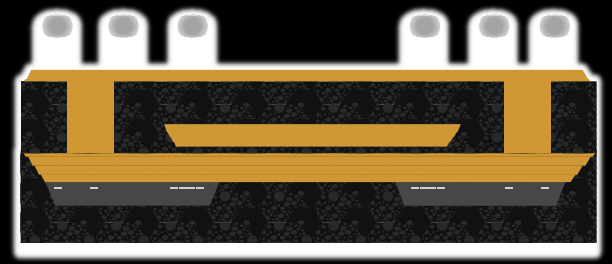
6.x.



6.v.



6.xi.



6.
- i. Chips Last FC bonding
- ii. Module level test
- iii. Die Underfill
- iv. Cure
- v. Mold
- vi. Cure
- vii. Backgrind
- viii. Marking
- ix. AOI
- x. Optional backside metal

7
- **i. Optional RDL Module** repeat for all RDL layers
- ii. UBM Seed PVD
- iii. UBM Photoresist
- iv. Expose & Dev
- v. Cu Pillar Plating
- vi. Strip & Etch
- vii. Reflow
- viii. AOI
- ix. Proceed to substrate mounting
- x. System level test

Ship Out

DECA

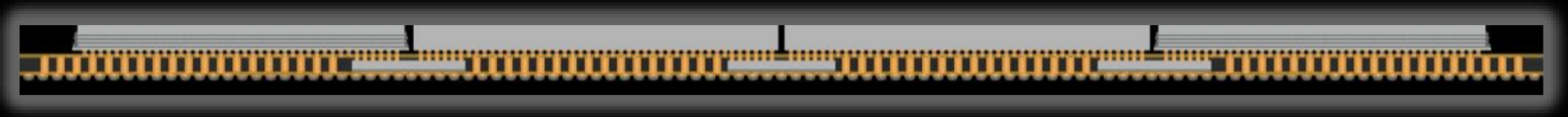
Multiple patents issued and pending

Outline

- Introduction
- MFIT Process Flow Overview
- MFIT Process Flow Details
- Conclusion

Conclusion

- AI & HPC driving multi-chip integration
- Fine-line, high-density RDL requirements (UCIe, HBM 3 & 4) increases yield risk
- Fan-out interposers with RDL bridges provide a scalable, high-yielding solution
- Full-Thickness flow with VIBs simplifies process complexity, reducing cost & improving manufacturability



MFIT provides a robust, scalable solution that reduces yield risk & improves manufacturability for next-generation AI & HPC packaging

Thank you from