Heterogenous Integration in High Volume: Now and Looking Forward

William Lambert
Advanced Micro Devices, Inc.

AMD
together we advance_

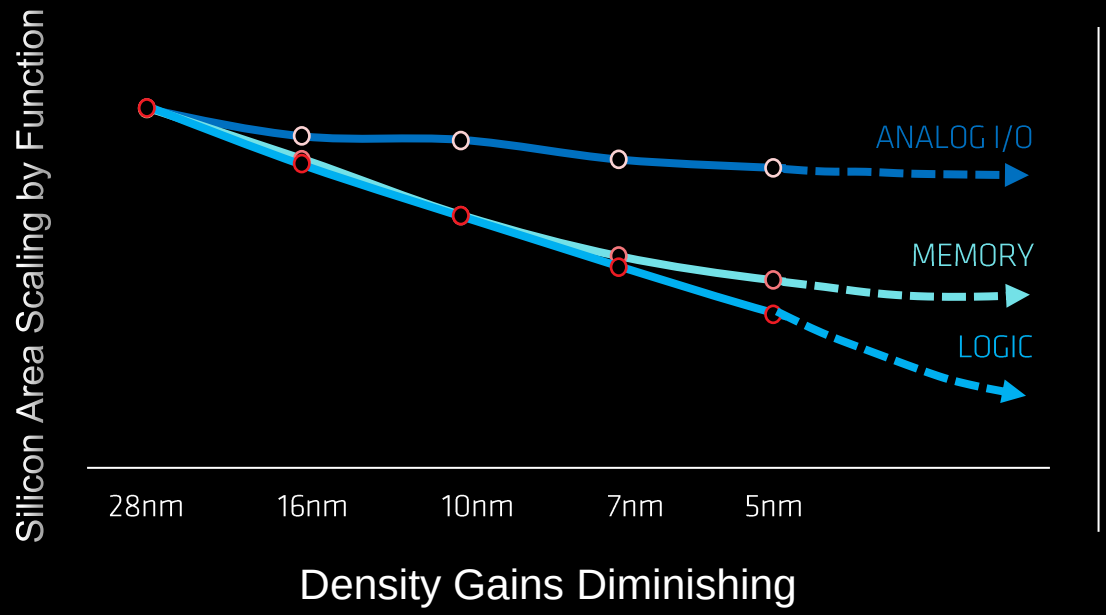
CAUTIONARY STATEMENT

This presentation contains forward-looking statements concerning Advanced Micro Devices, Inc. (AMD) such as the features, functionality, performance, availability, timing and expected benefits of AMD products; TAM for data center, PCs, embedded and gaming; and technology trends, innovation and roadmaps, which are made pursuant to the Safe Harbor provisions of the Private Securities Litigation Reform Act of 1995. Forward-looking statements are commonly identified by words such as "would," "may," "expects," "believes," "plans," "intends," "projects" and other terms with similar meaning. Investors are cautioned that the forward-looking statements in this presentation are based on current beliefs, assumptions and expectations, speak only as of the date of this presentation and involve risks and uncertainties that could cause actual results to differ materially from current expectations. Such statements are subject to certain known and unknown risks and uncertainties, many of which are difficult to predict and generally beyond AMD's control, that could cause actual results and other future events to differ materially from those expressed in, or implied or projected by, the forward-looking information and statements. Investors are urged to review in detail the risks and uncertainties in AMD’s Securities and Exchange Commission filings, including but not limited to AMD’s most recent reports on Forms 10-K and 10-Q.

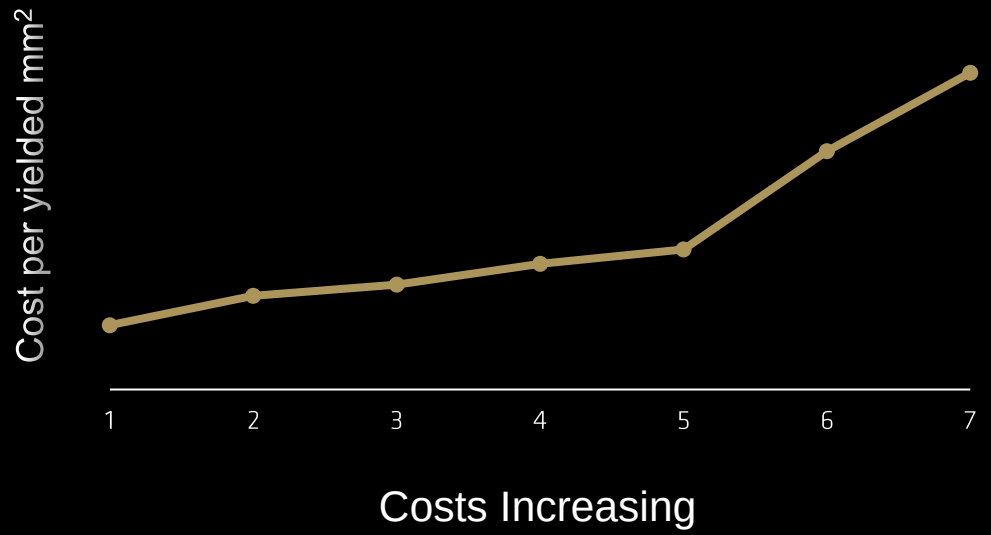
AMD does not assume, and hereby disclaims, any obligation to update forward-looking statements made in this presentation, except as may be required by law.

Long-Term Scaling Challenges We're Addressing

Limited and Divergent Scale Factors [1]



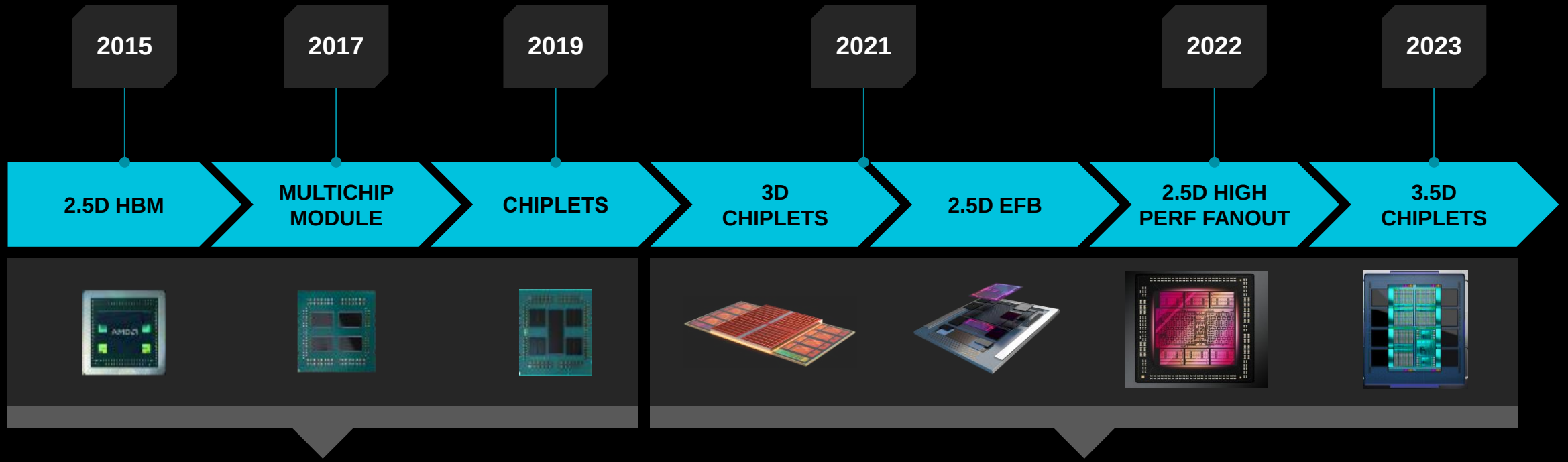
Increasing Costs[2]



Moore's Law slowing down and cost to add number of transistors/chip is increasing

Where we Are

Advanced Packaging Journey

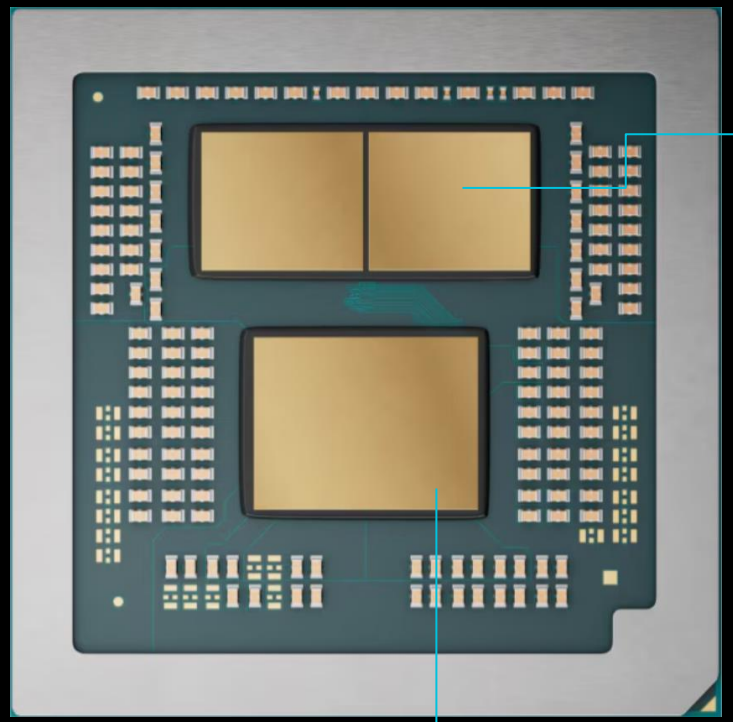


Led Industry in Chiplet Architecture

New Era of Products driven by Aggressive 3D/2.5D Integration Roadmap

Scaling Horizontally and Vertically to enable Compute and Memory Integration

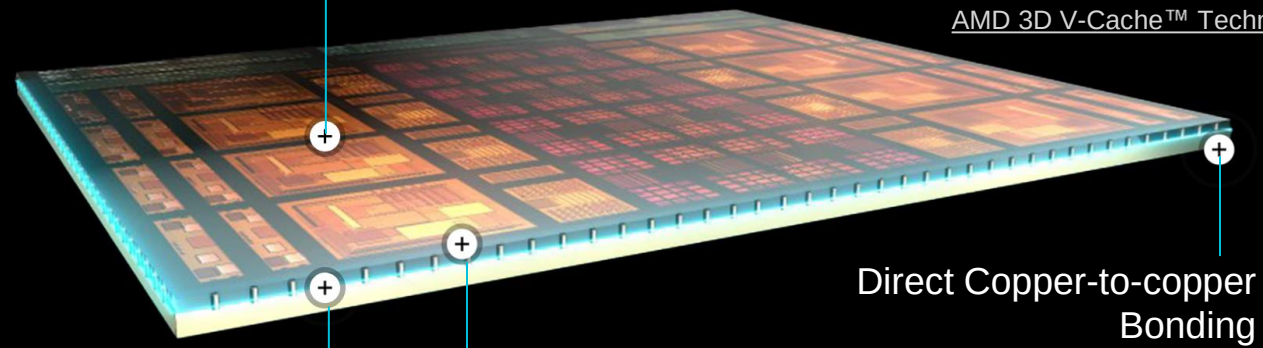
AMD Ryzen™ 9000X3D Series: 2nd Generation AMD 3D V-Cache™



AMD Ryzen™ 9 9955HX3D

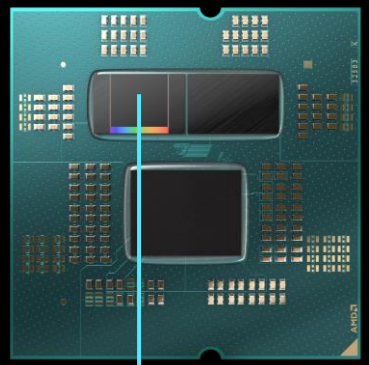
CPU Complex Die (CCD)
Up to 8-core “Zen5”

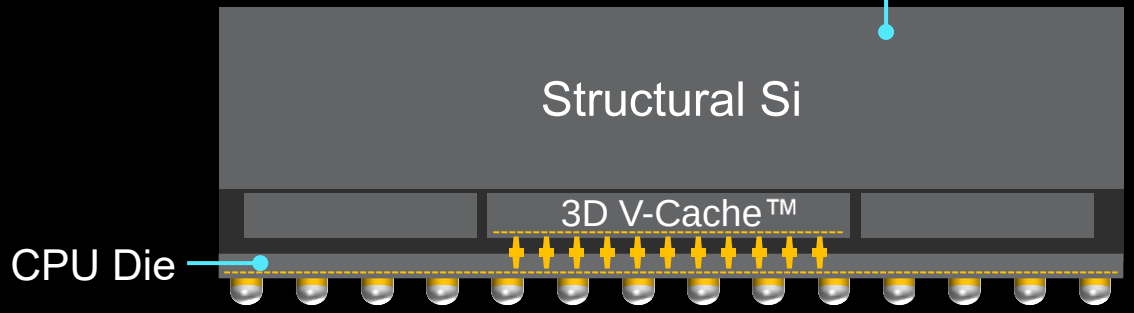
I/O Die (IOD)
Memory, other HSIO, Graphics



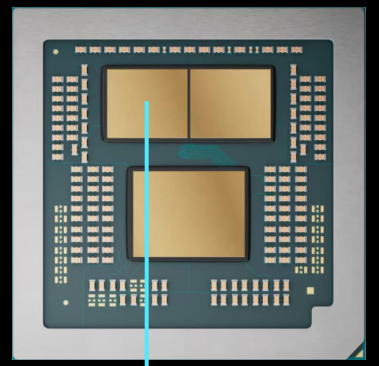
1st Versus 2nd Generation 3D V-Cache™

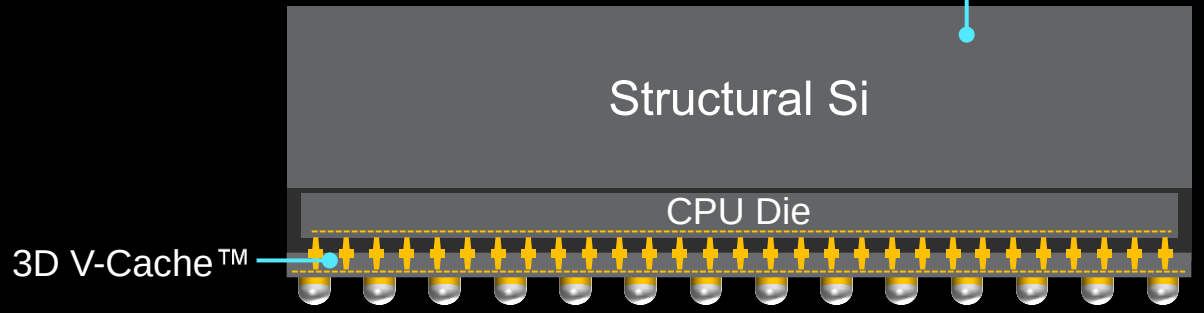
1st Generation:
AMD RYZEN™ 9
7950X3D

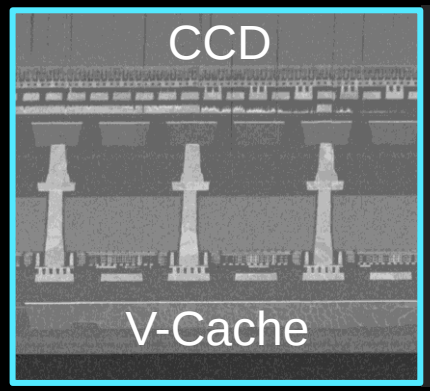




2nd Generation:
AMD RYZEN™ 9
9955X3D





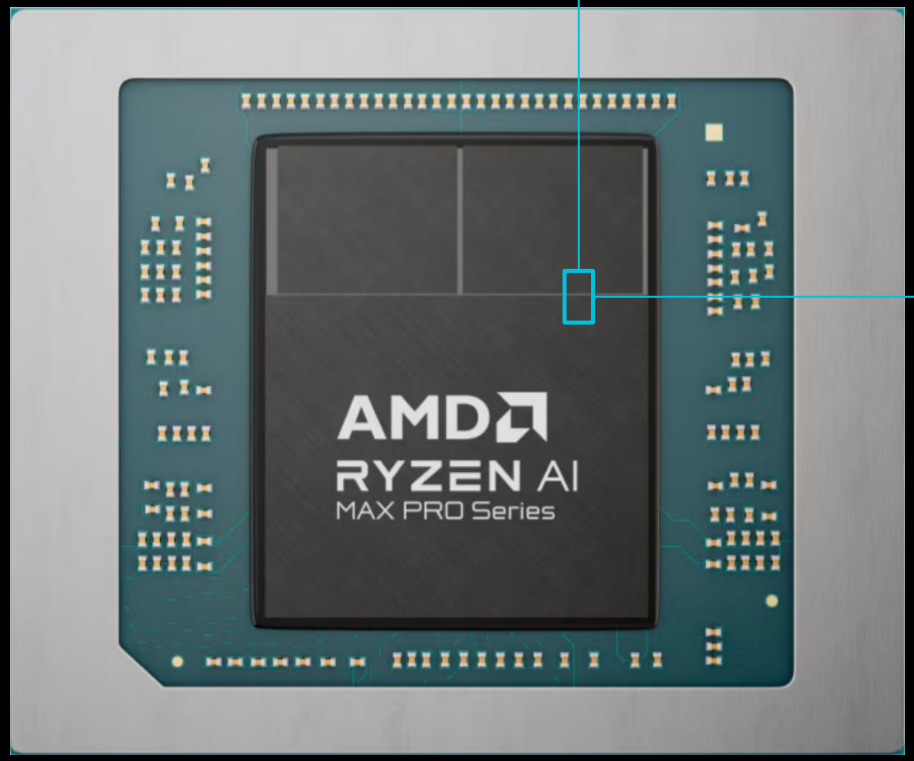


- **Face-to-Back Hybrid Bonding at <9um Pitch**
- **2nd Generation places CPU Die on top of the stack**

Ryzen AI Max PRO 300 Series

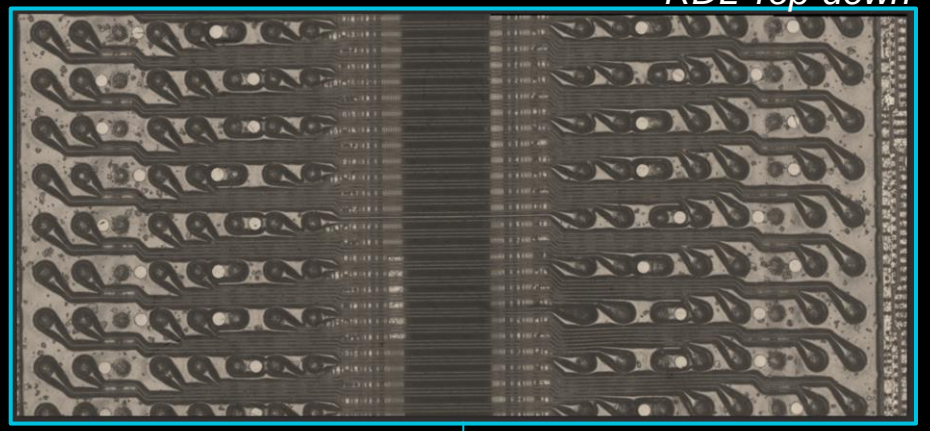
2.5D Advanced Packaging

Continued strategic use of 2.5D advanced packaging to reduce die-to-die power and latency

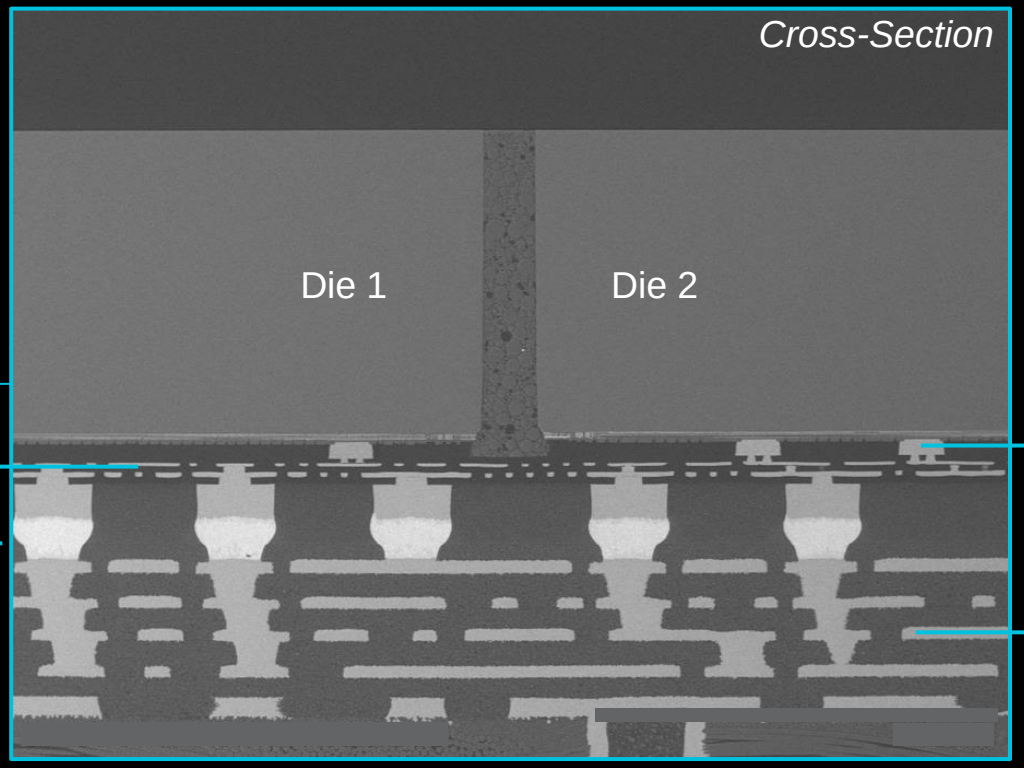


AMD Ryzen™ AI Max+ PRO 395

RDL Top-down



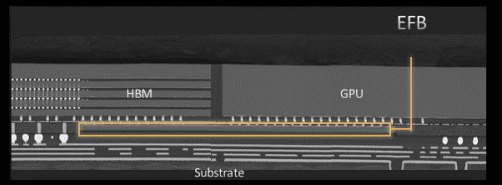
Cross-Section



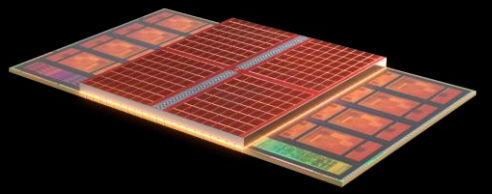
Advanced Packaging Innovations to Meet AI Challenges

Doubling Compute and Memory	**2.5D Packaging** to build larger chip-modules
Energy efficient interconnects	**3D Packaging** to reduce interconnect energy
Network bandwidth doubling	**Improved Package Loss, Connectors, CPO**
Growing demand for efficient power delivery	**Integrated Passives** in package
Thermal Challenges	**Liquid Cooling, Cold Plate Tech, New Materials**

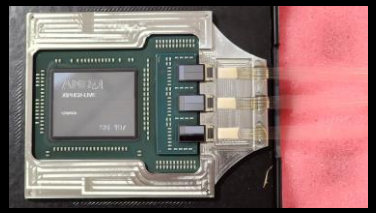
2.5D



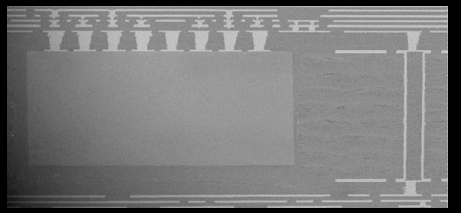
3D



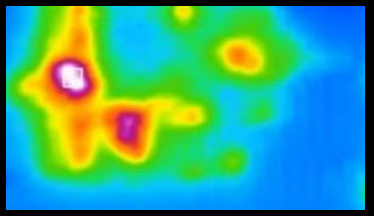
High Speed Signaling



Substrate Embedded Passives



Thermals



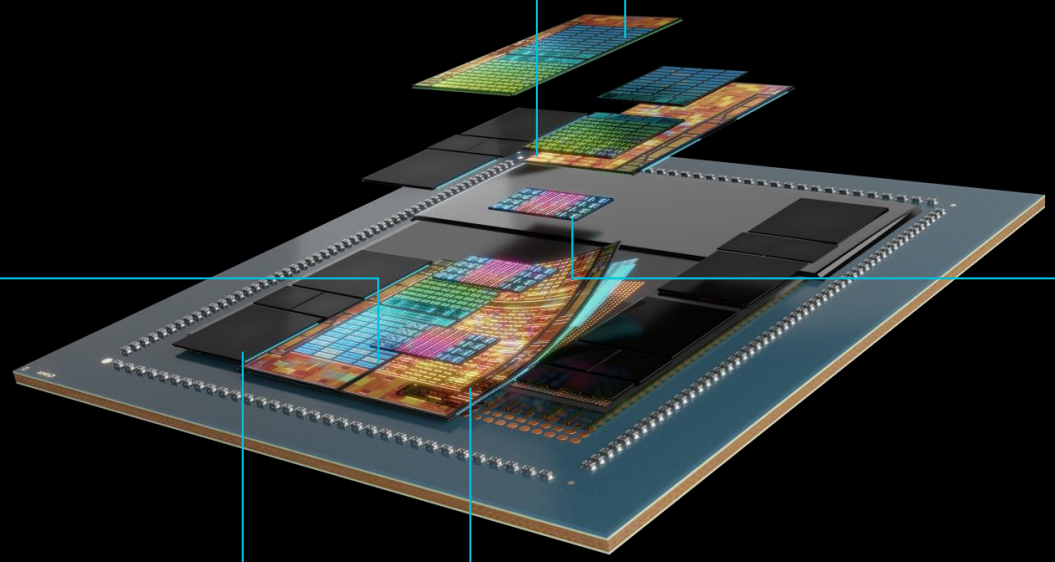
AMD Instinct™ MI300 Series Accelerators

Key Innovations

I/O Die (IOD)
256MB AMD Infinity Cache™
Infinity Fabric Network-on-Chip

AMD Infinity Fabric™ AP Interconnect

8 stacks of HBM3
MI300A: 128 GB (8H)
MI300X: 192 GB (12H)



Accelerator Complex Die (XCD)
6X38 AMD CDNA™ 3 Compute die

CPU Complex Die (CCD)
3 x 8 “Zen 4” Cores

3.5D Package
3D hybrid bonding
2.5D silicon interposer

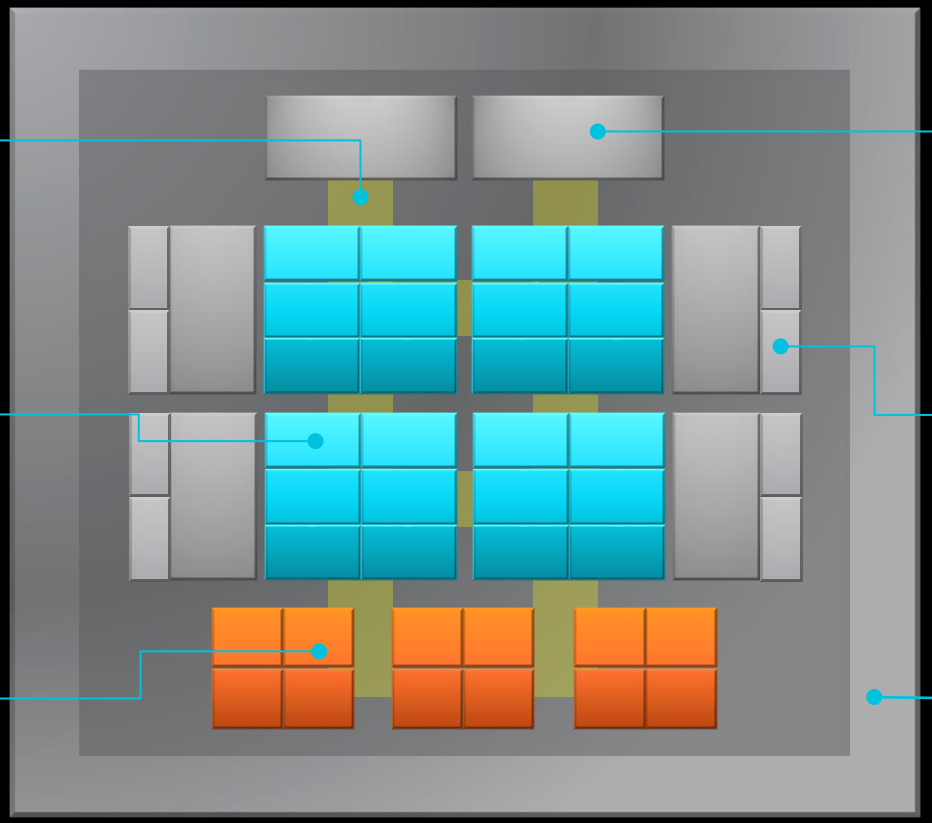
Where we are Going

Future System-in-Package Architecture

High-Speed Standardized Die-to-Die Interfaces (UCIe)

3D Components enabled by Front end Precision

Heterogeneous Compute (Accelerators, Novel memories))



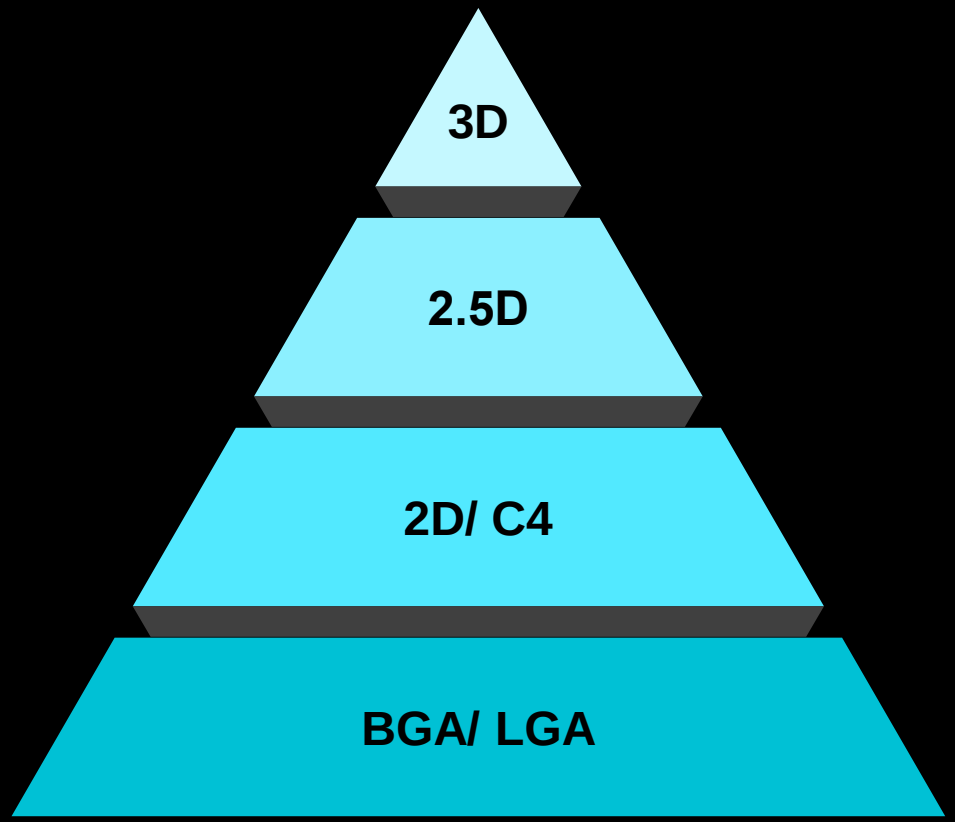
Co-Packaged Optics

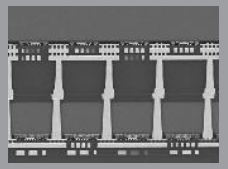
Memory

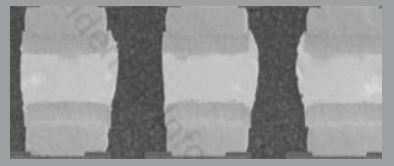
Advanced 3.5D Packaging

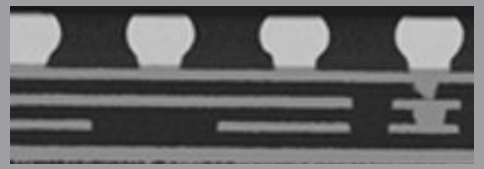
Compute density and heterogeneous integration drives module sizes beyond wafer-based processing

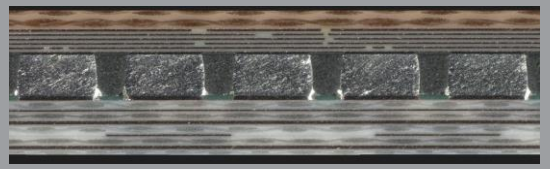
Interconnect Scaling Focus







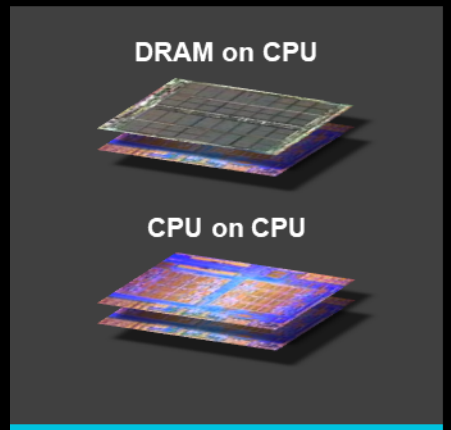




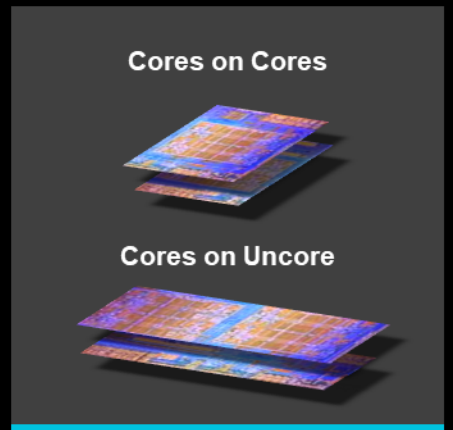
Future AI hardware requires investments in all key areas of advanced packaging to build best-in-class devices

3D Hybrid Bonding Using Front End Precision

Hybrid Bonding Pitch

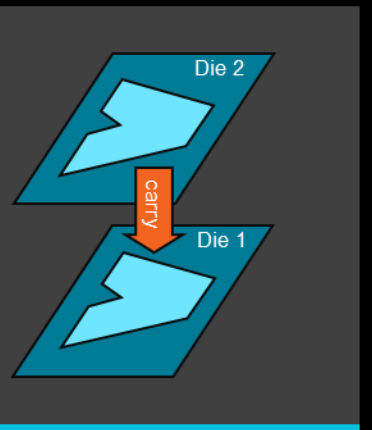


FULL DIE-TO-DIE

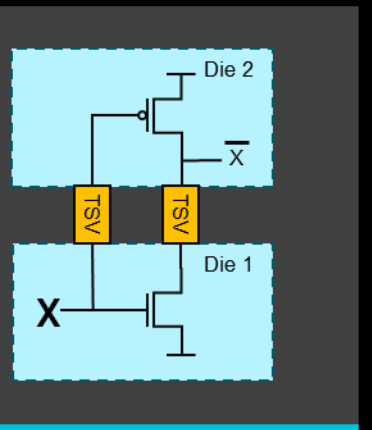


IP ON IP

MACRO IN MACRO



IP FOLDING/ SPLITTING



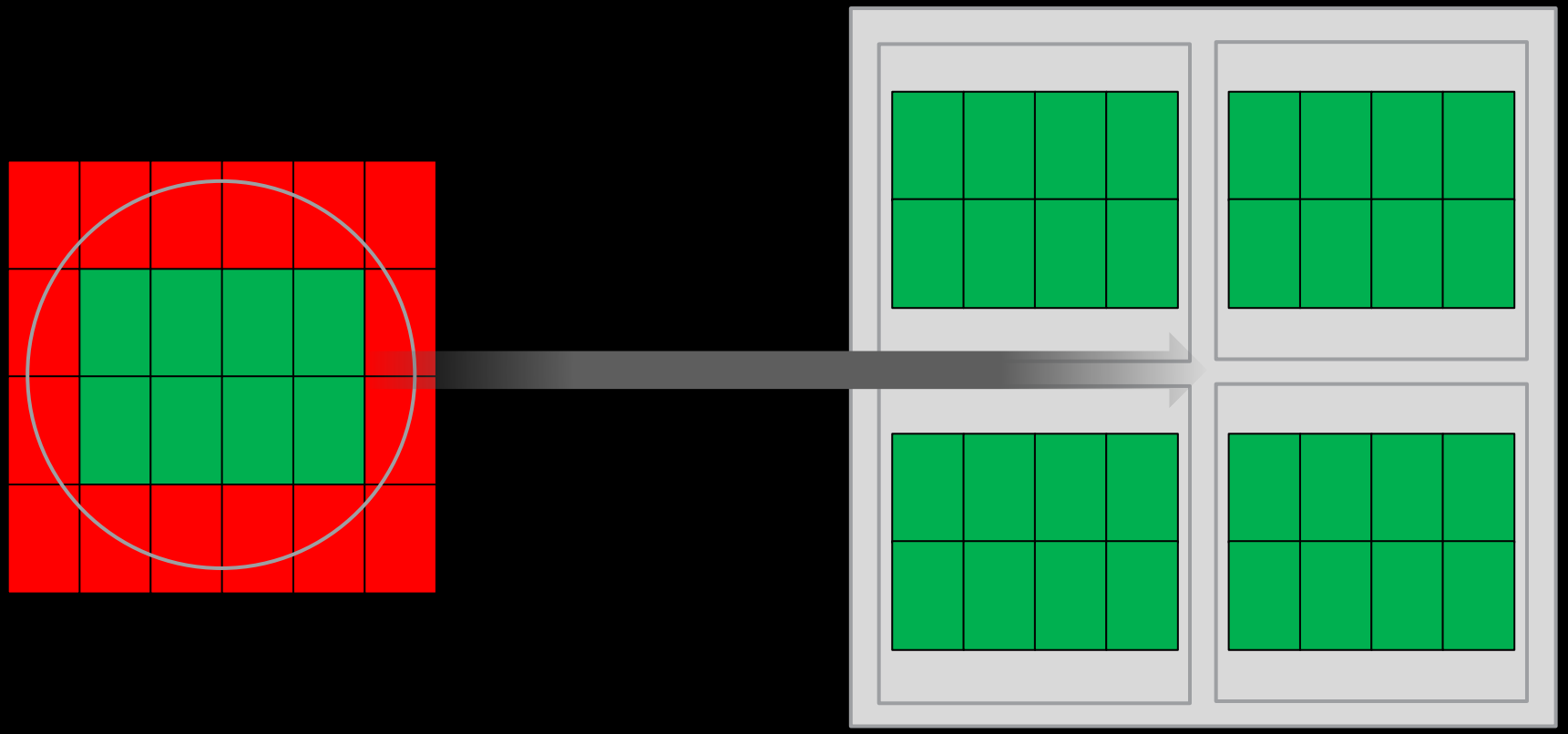
CIRCUIT SLICING

Revolutions in 3D Hybrid Bonding (process, materials) can enable groundbreaking architectures not possible with monolithic designs

Panel-Based 2.5D Architectures

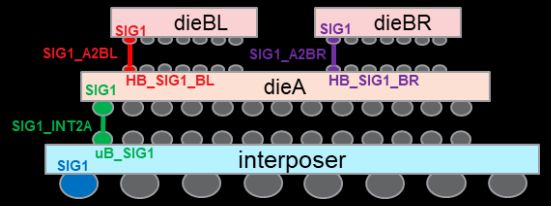
Wafer Level 2.5D

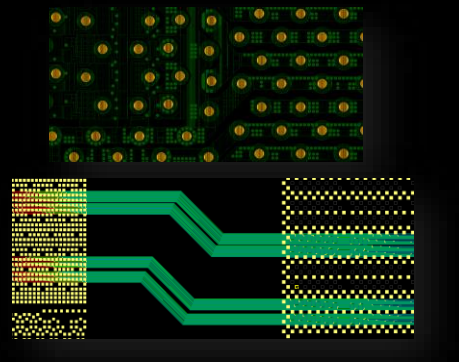
Panel Level 2.5D

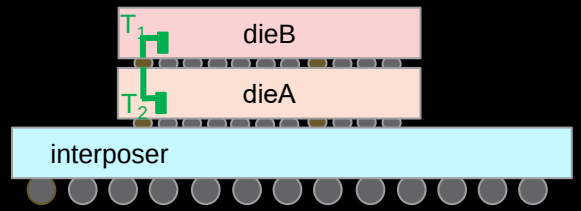


Panel Level 2.5D Capabilities Crucial for Continued Scaling

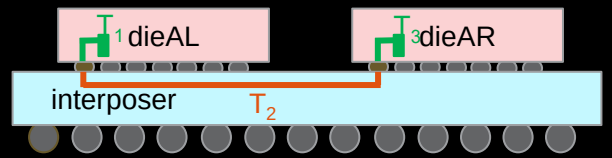
AMD Next-Gen 3DIC Methodology





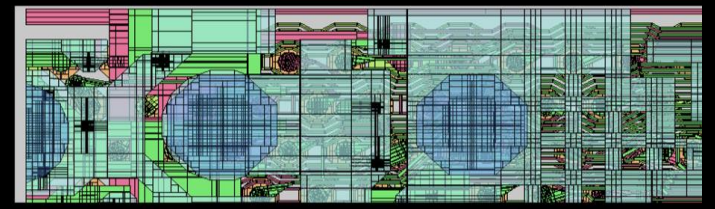


$T_{path} = T_1 + T_2$

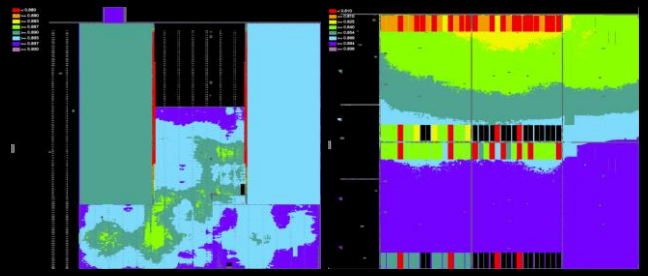


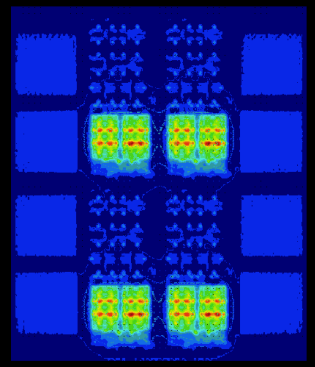
$T_{path} = T_1 + T_2 + T_3$

FLOOR PLANNING → **CONSTRUCTION** → **PARASITICS EXTRACTION**



INTERPOSER DELAY CALC. → **ELECTRICAL ANALYSIS** → **THERMAL ANALYSIS**



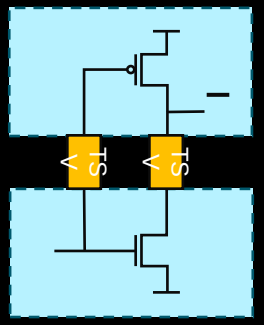


3Dblox adopted as the standard format for defining 3.5D Architecture

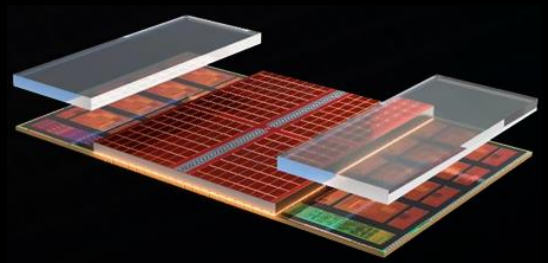
Source: Nitin Navale, Simon Burke, DAC 2024 Invited talk

Tools as a Major Focus for Innovation

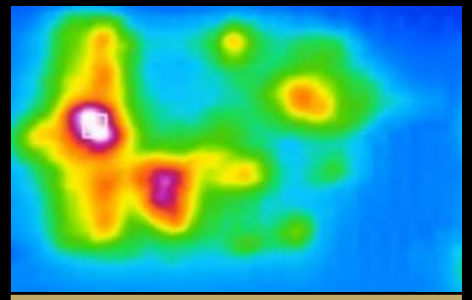
AI DRIVEN FLOOR PLANNING



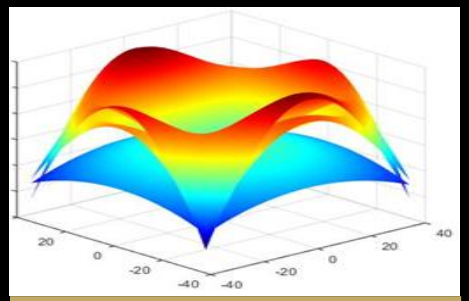
FULL EDA 3D PLACE AND ROUTE



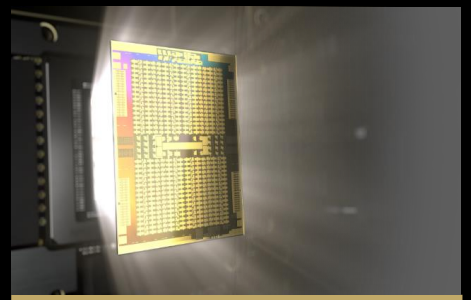
MERGED SILICON AND PACKAGE TOOL FLOWS



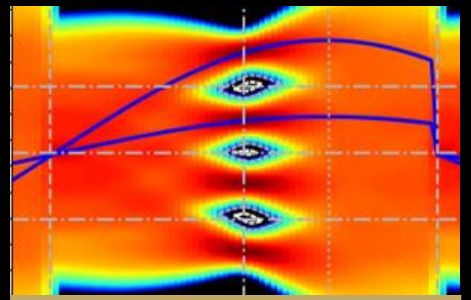
THERMALS



MECHANICAL



POWER DELIVERY



SIGNAL INTEGRITY


AMD