Breaking Barriers in Semiconductor Packaging:

Leveraging Glass-Based Substrates for Superior Connectivity

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Where we are at?

Advanced Packaging, Where are we at?

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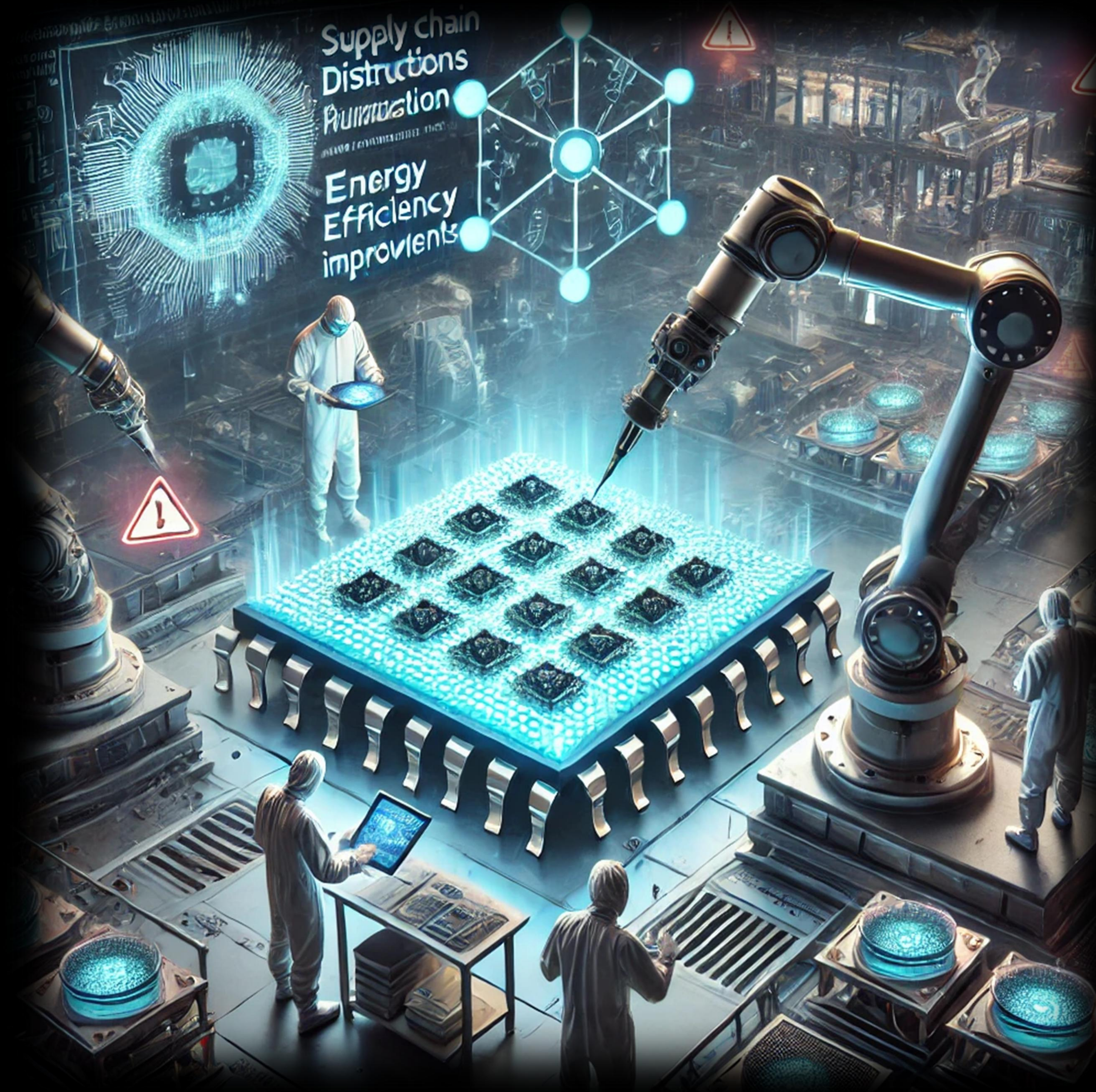
Artificial Intelligence

High Performance Computing

Next Gen Communications

Heterogeneous Integration



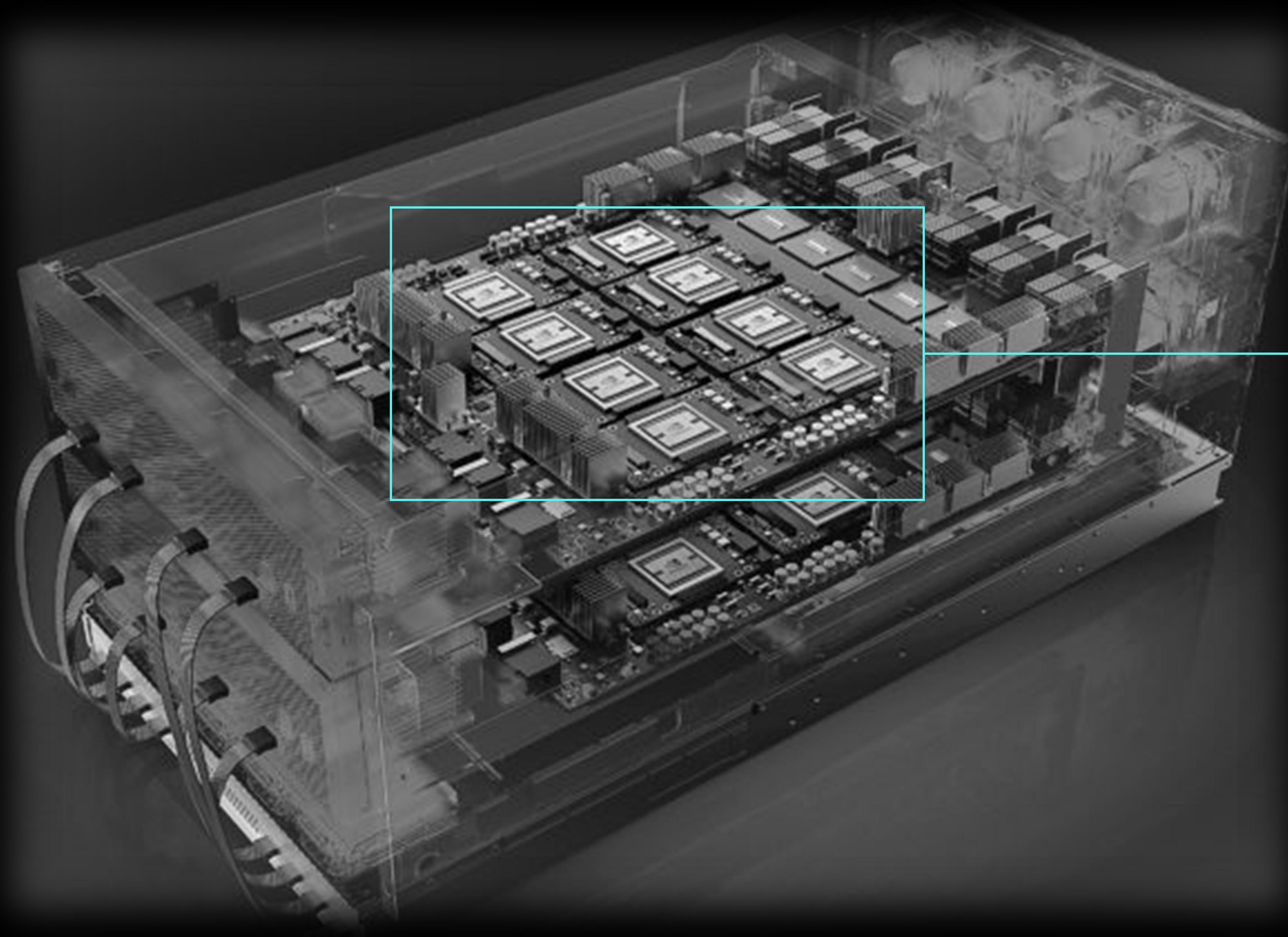
Too Many Interfaces

Complicated Supply Chain

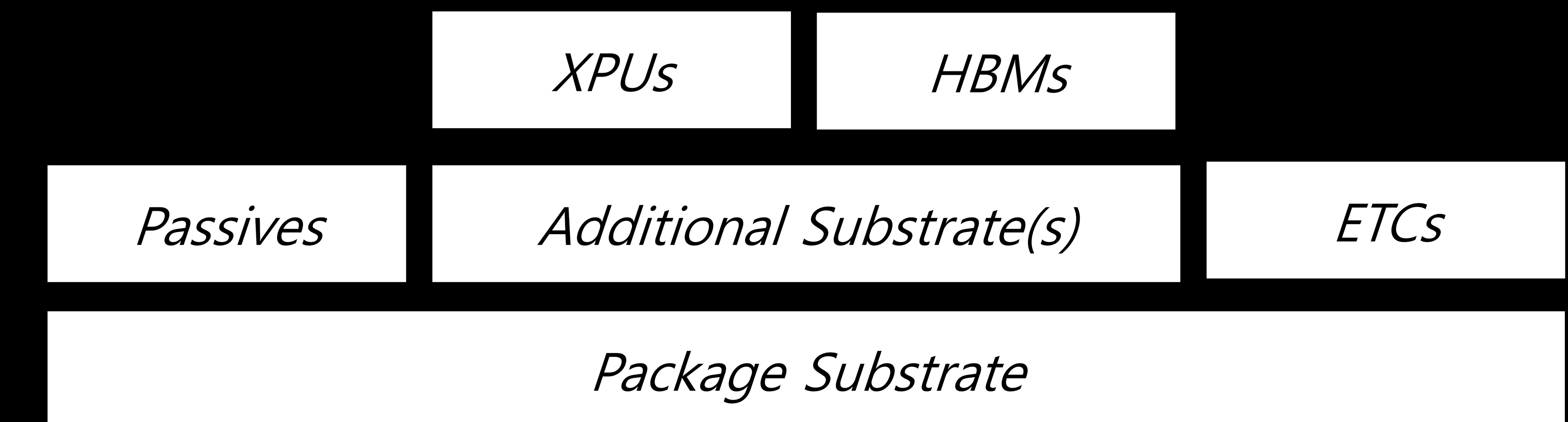
Performance Limitation

Miniaturization Challenges

A Typical AI System



HPC Chips
- *XPUs*
- *HBMs*
- *Passives*
- *Substrates*



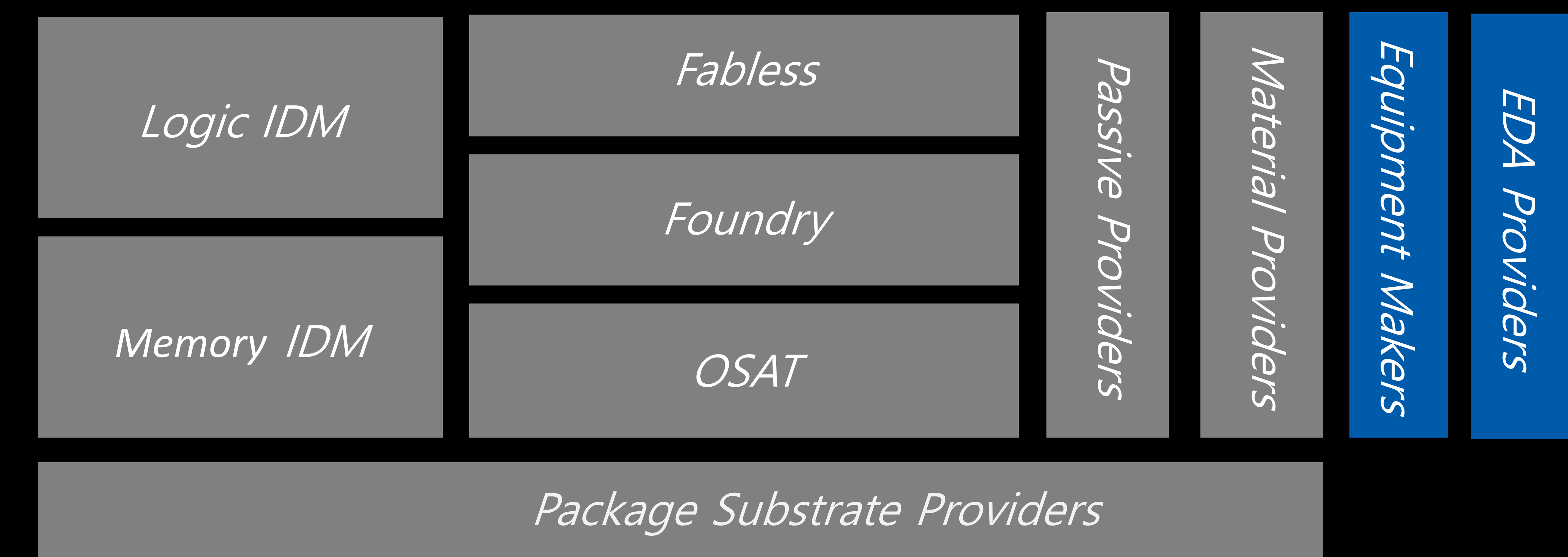


Image Source: https://www.nextplatform.com/2018/11/13/nvidia-pulls-all-of-the-ai-pieces-together/

Necessities – Advanced Packaging Industry

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✓ Packaging Requires Out-of-Box Solutions for

- **More Functionality** for more chips and devices
- **More Bandwidth**
- **Higher Performance**
- **Technology Scalability** for Sustainability
- **Lower Energy Consumption**
- **Shorter Development Leadtime**
- **Reasonable Cost Packaging Options**
- **And, more …**

Industry Approaches

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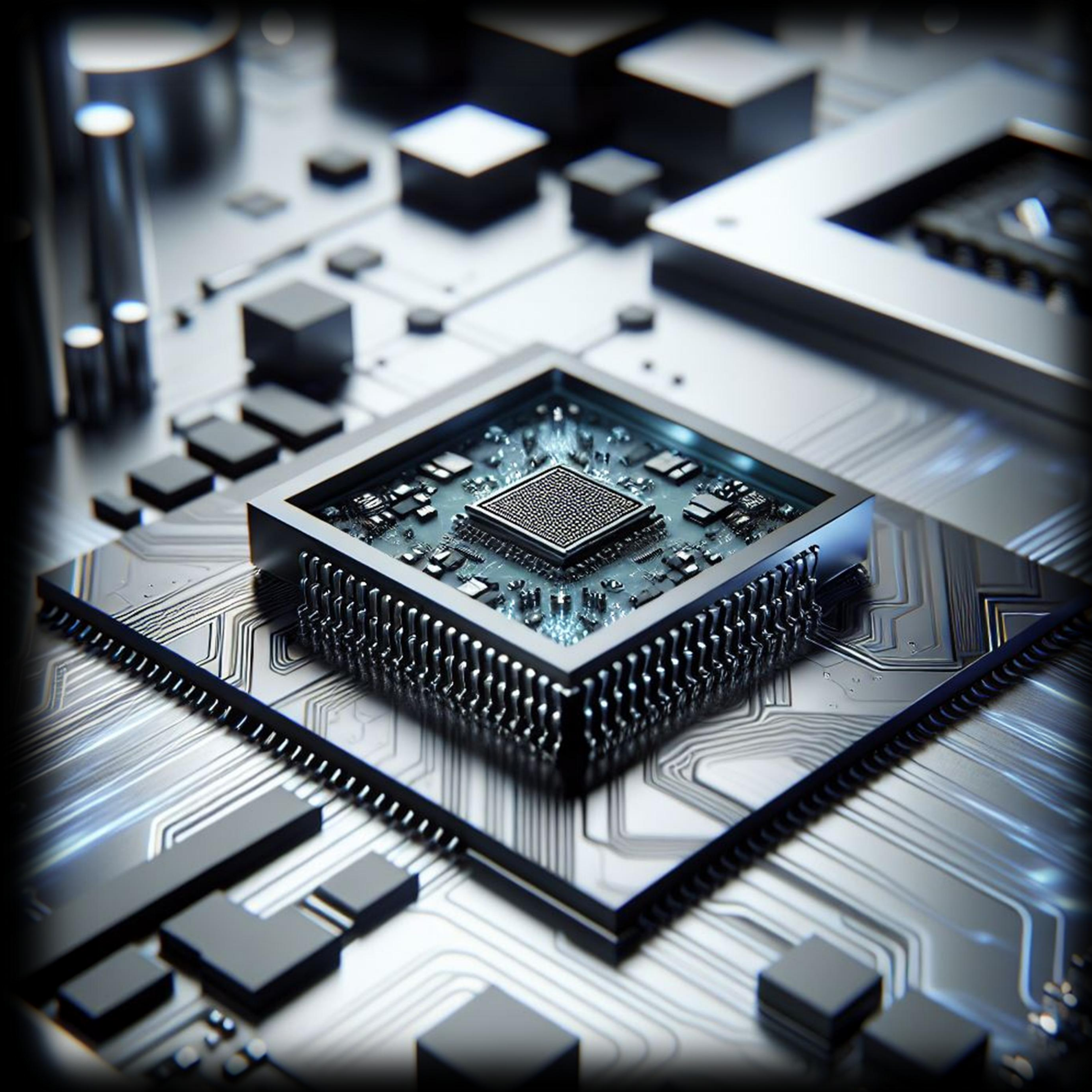
2.5D Technologies

3D Technologies

Novel Interconnections

Instrumental Advancements



Packaging Substrates

Today's Focus

Packaging Substrate Challenges

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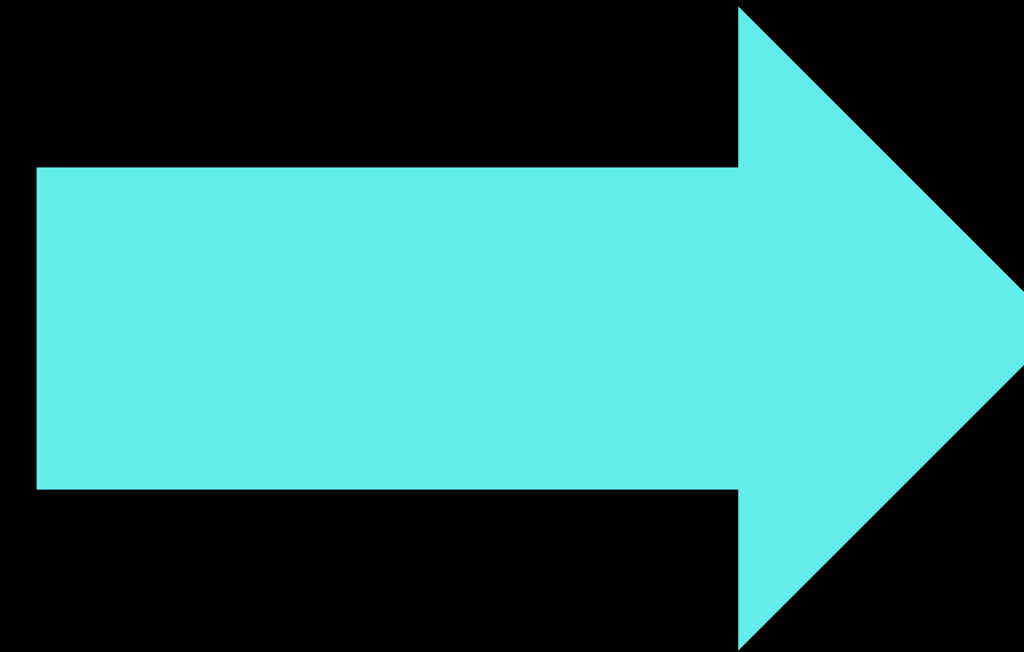

✓ User Demands

- More Functionality
- More Bandwidth
- Higher Performance
- Technology Scalability
- Lower Energy Consumption
- Shorter Development Leadtime
- Reasonable Cost Packaging Options
- And, More …

Simpler Package Structure

Denser RDL (Traces and BVH)

Larger Package Body Size

Flatter Conductor Surface

Less Company Involvement

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What we need to focus?

To Solve Substrate Challenge, What We Need Today?

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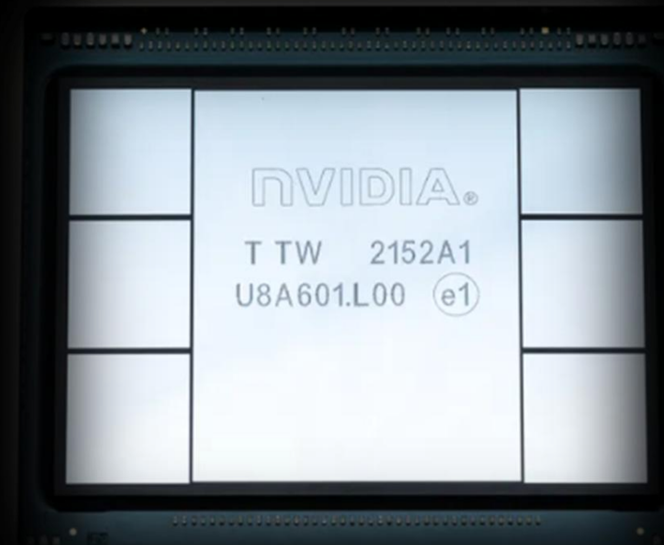

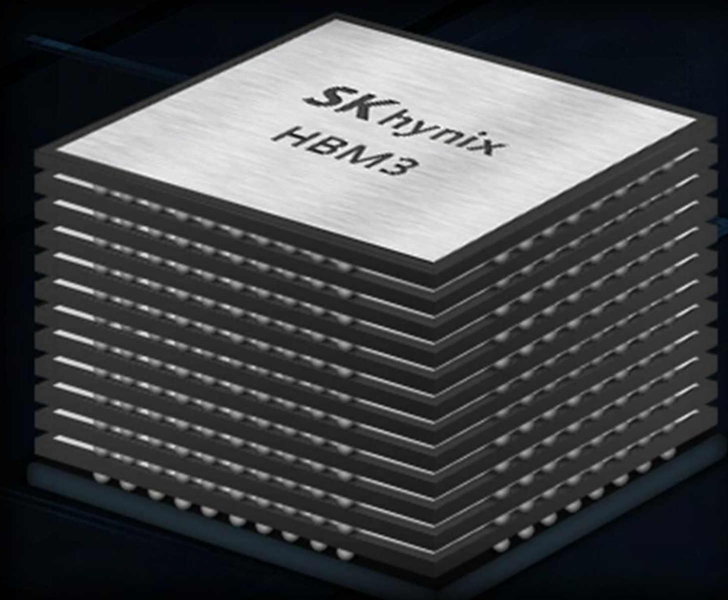

Common Features for These 3 Products?

- ✓ In an industry, an **underdog** refers to a company, startup, or individual that is at a disadvantage compared to dominant competitors, often due to factors like limited resources, brand recognition, market share, or experience. However, **underdogs** are known for their resilience, innovation, and ability to disrupt the market by challenging established players through unique strategies, groundbreaking technologies, or superior customer experiences. For example, a small semiconductor startup competing against giants like Intel or TSMC could be considered an **underdog** if it introduces a novel technology that challenges industry norms despite having fewer resources.

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Providing the Ultimate Solution to 3DHI

absolute solution for integrated circuits

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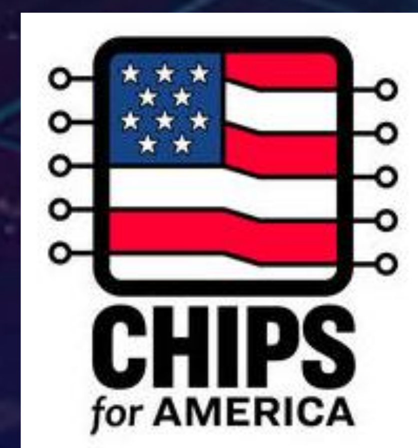
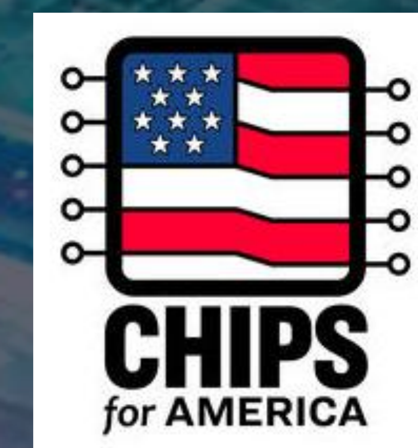
'IC' On A Thin Glass Substrate



Manufacturing Incentives



NAPMP(National Advanced Packaging Manufacturing Program)
R&D Incentives

Glass Substrate in Semiconductor Packaging

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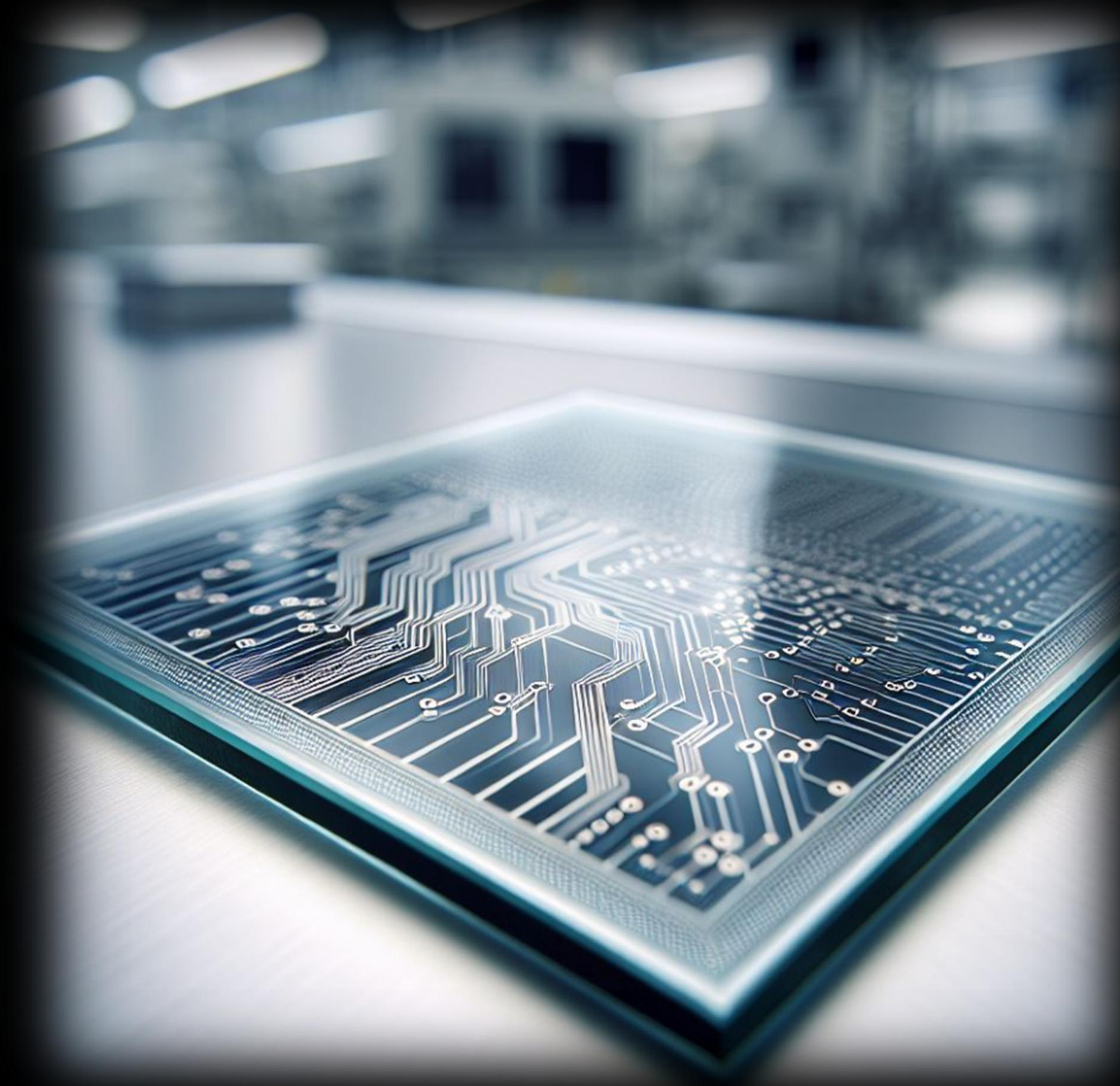
Advantages

- Superior Electrical Performance
- High Dimensional Stability
- Fine-Line Routing Capability
- Improved Thermal Stability
- Higher Integration Potential



Challenges

- Fragility and Mechanical Strength
- Manufacturing Complexity
- Cost Considerations
- Thermal Conductivity
- Adoption Barriers

Challenges facing are significant | Opportunities for **'Innovation'** and **'Growth'**

absolics, Past 10+ Years in SK Group

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1st Glass Core Substrate MFG PJT Start

2018. APR

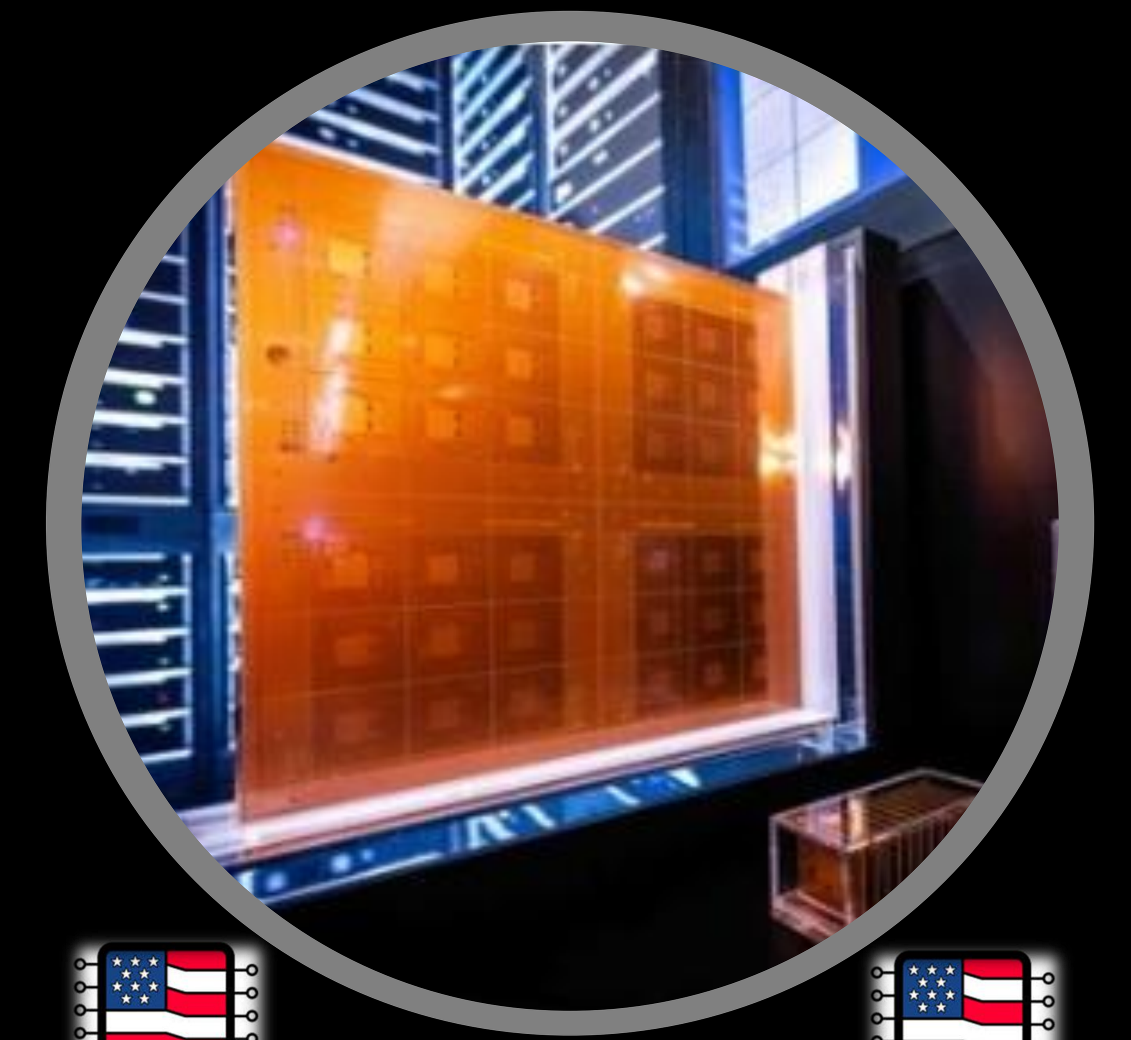
Established USA Corporation

2021. NOV

1st Plant Completion @ Covington GA

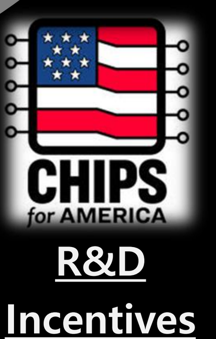
2024. APR

World 1st Glass Core Substrate Volume Production



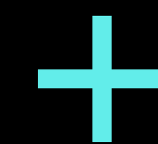
MFG Incentives

2025



R&D Incentives

Business Technology Assessments → **Lab-to-Fab** with Customer Engagements



Unprecedented **Ecosystem** Builds → Process Transfer & **Customer Site-Qualification**

(3 Years) **(6 Years)** **(1+ Years)**

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How Does Glass Substrate Break Barriers?

3DHI(3D Heterogenous Integration)

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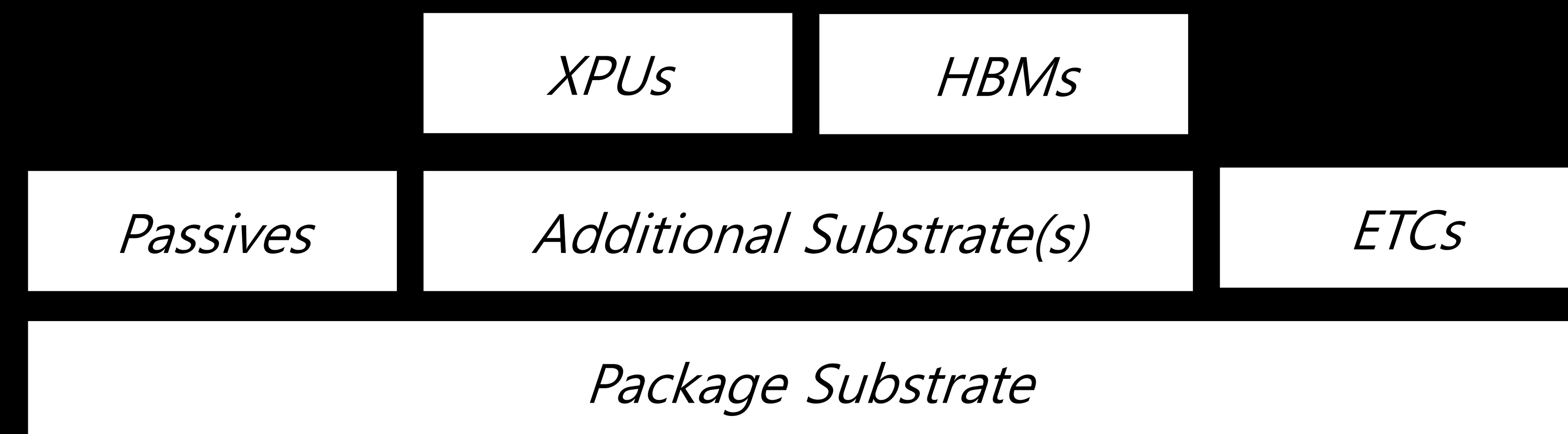
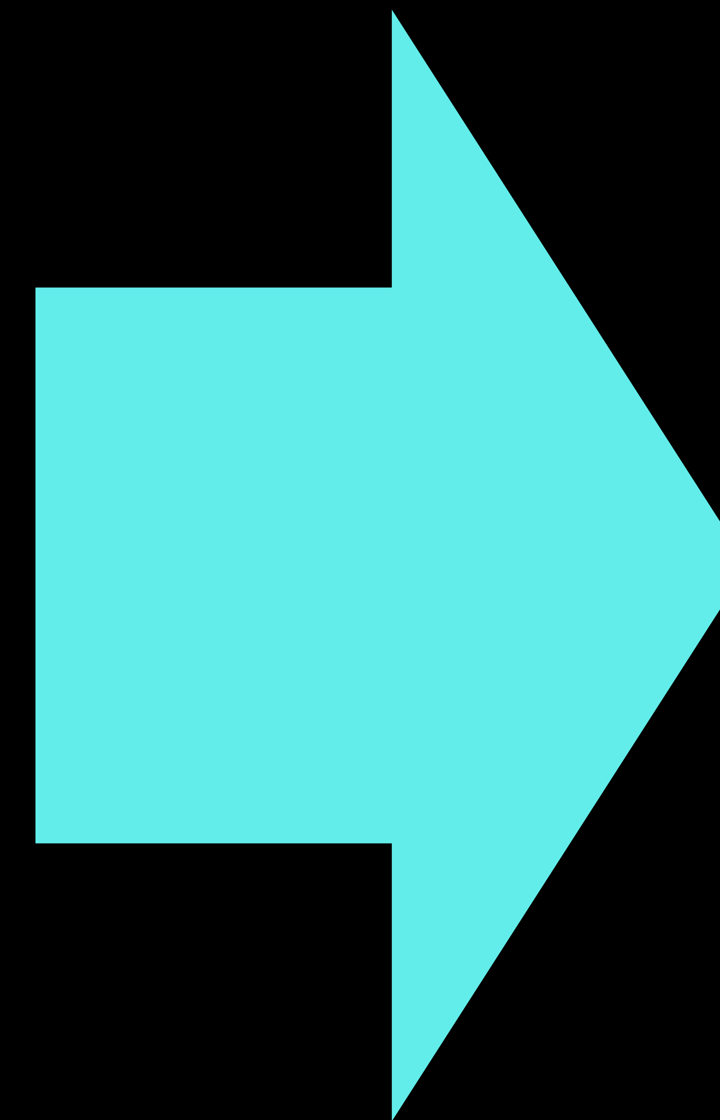
Today, companies are heavily working on 3DHI (3-Dimensional Heterogeneous Integration)





Simpler Package Structure

Denser RDL (Traces and BVH)

Larger Package Body Size

Flatter Conductor Surface

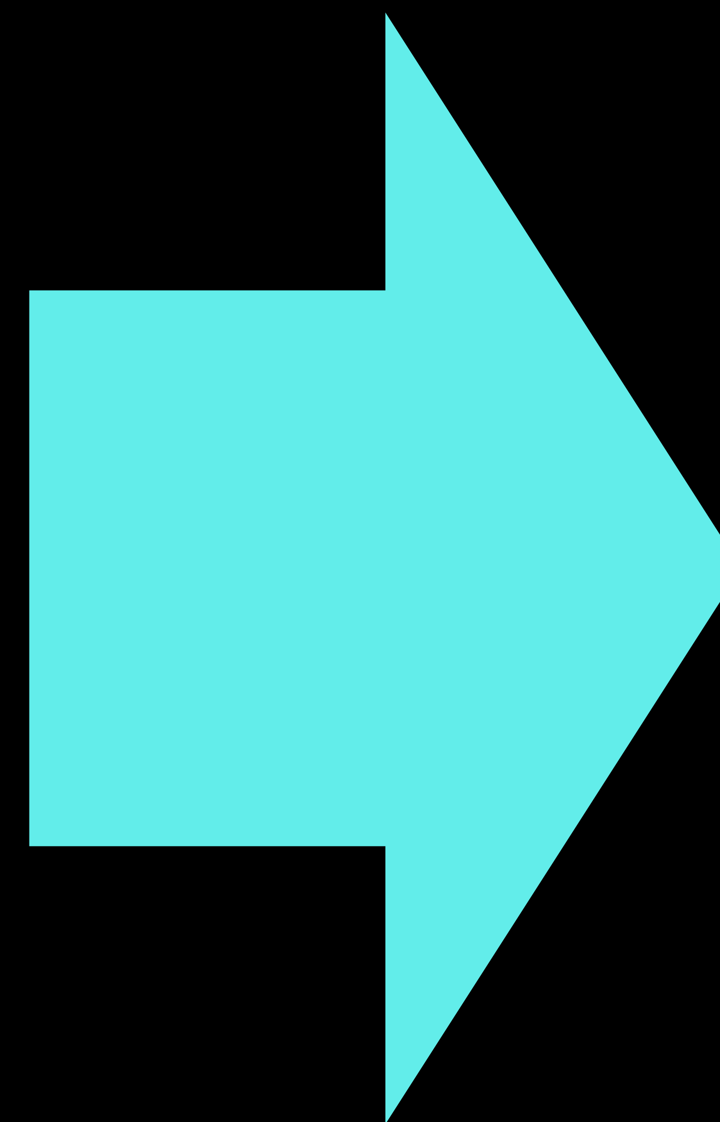
More Company Involvement

Dream Packaging Solution for 3DHI Systems

What if, we have **An Ultimate Solution for Die-to-Die Interconnections** for **'More Bandwidth'** with **'Reasonable Package Cost Options'**

- ✓ Parallel Interface with 2.5D+ PKG
  - Lower Power Consumption
  - Higher Bandwidth
  - Higher PKG Cost

- ✓ Serial Interface with 2D PKG
  - Higher Power Consumption
  - Limited Bandwidth
  - Lower PKG Cost



- ✓ **Parallel Interface with 2D PKG**
  - **Lower Power Consumption**
  - **Higher Bandwidth**
  - **Lower PKG Cost**

absolics Contribution to 3DHI

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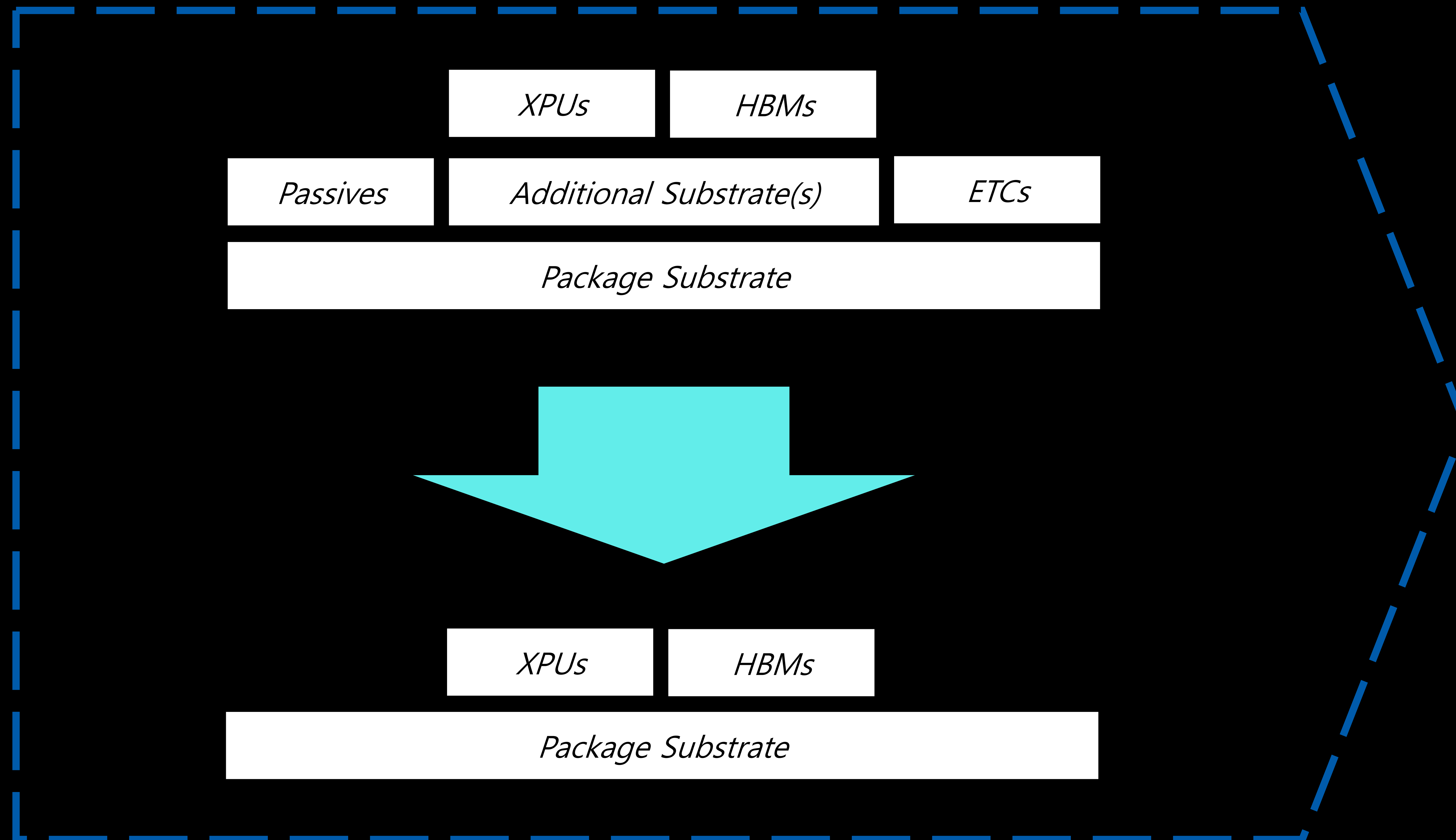
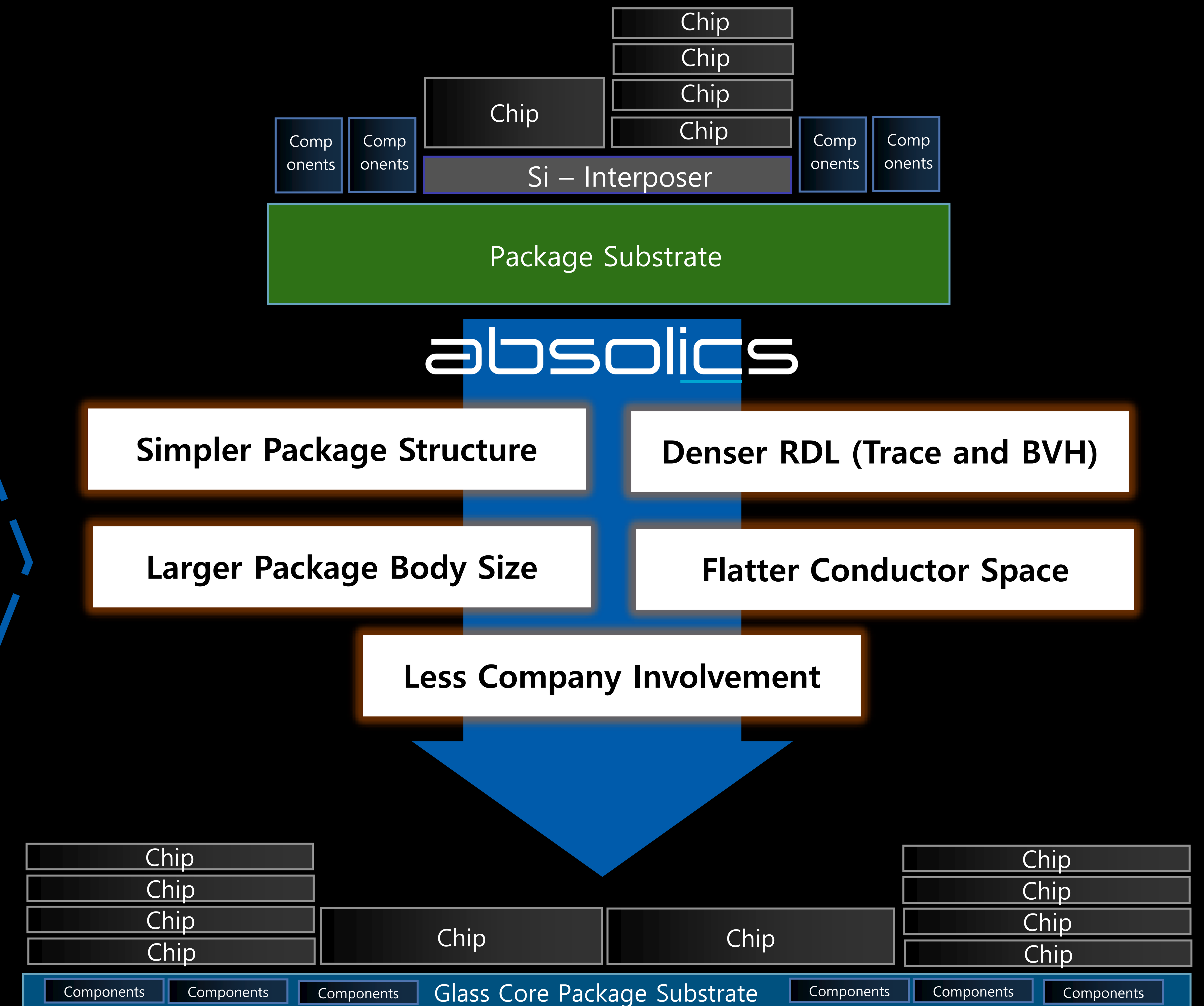
absolics enables **'Parallel Interface'** with **'2D PKG Options'**





absolics Provides Ultimate Solutions to 3DHI Systems

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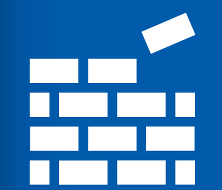
3DHI Requirements

More TR / mm2

→ Finer RDL

→ Finer Interconnection Pitch

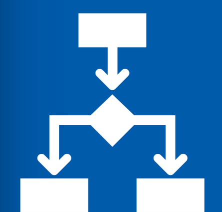
→ Larger Package



Minimum BU Layers

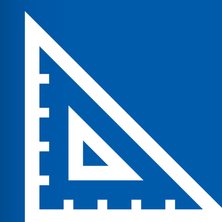
→ Higher Yield & Performance

Less Energy Consumption



Simpler SC/Process Flow

→ Lower Cost & Higher Yield



Ultra Flatness both in:

→ Warpage

→ Conductor Surface

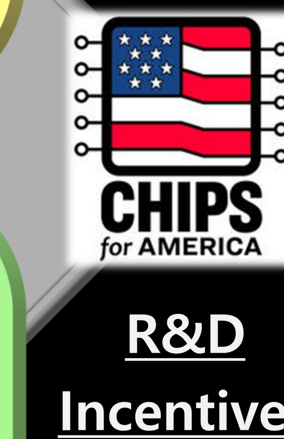
Scaling Up
HPC System Performance Improvement

Scale Down
Energy Usage, Formfactor, Supply Chain

Scale Out
Expandability with affordable Chiplets Solutions

Scale In
Ultra Fine Interconnections with Glass Core

MFG Incentives



R&D Incentives