

# Investigation of Behavior of Nanovoids in Electroless Cu Layer of 1<sup>st</sup> via Bottom of 3-Layer Stacked Micro-via Integrated in Substrate under Thermal Shock Test

Masahiko Nishijima\*, Ming-Chun Hsieh, Zheng Zhang, Rieko Okumura, Hiroyoshi Yoshida, Chuantong Chen, Aiji Suetake, Kimihiro Yamanaka, and Katsuaki Suganuma

*Flexible 3D System Integration Laboratory, Osaka University*

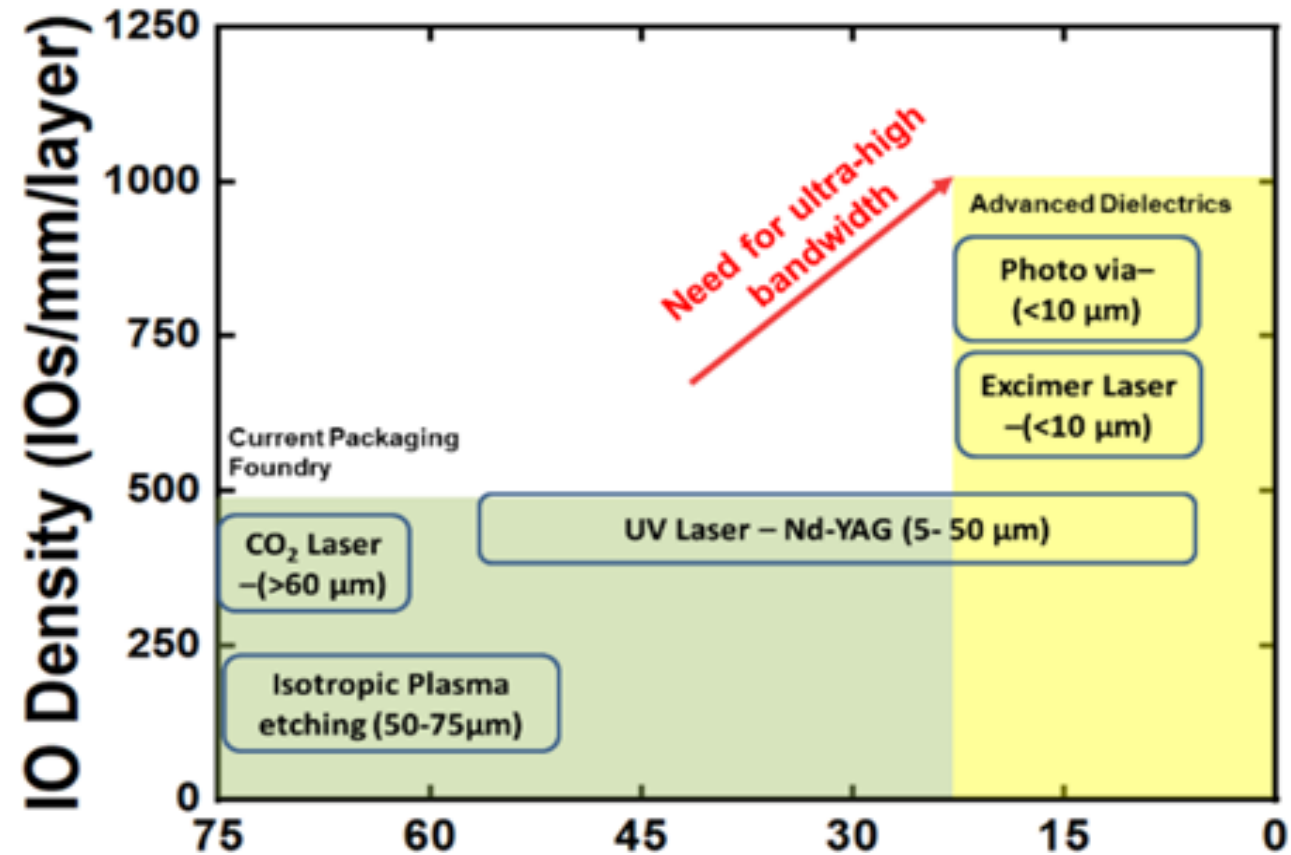
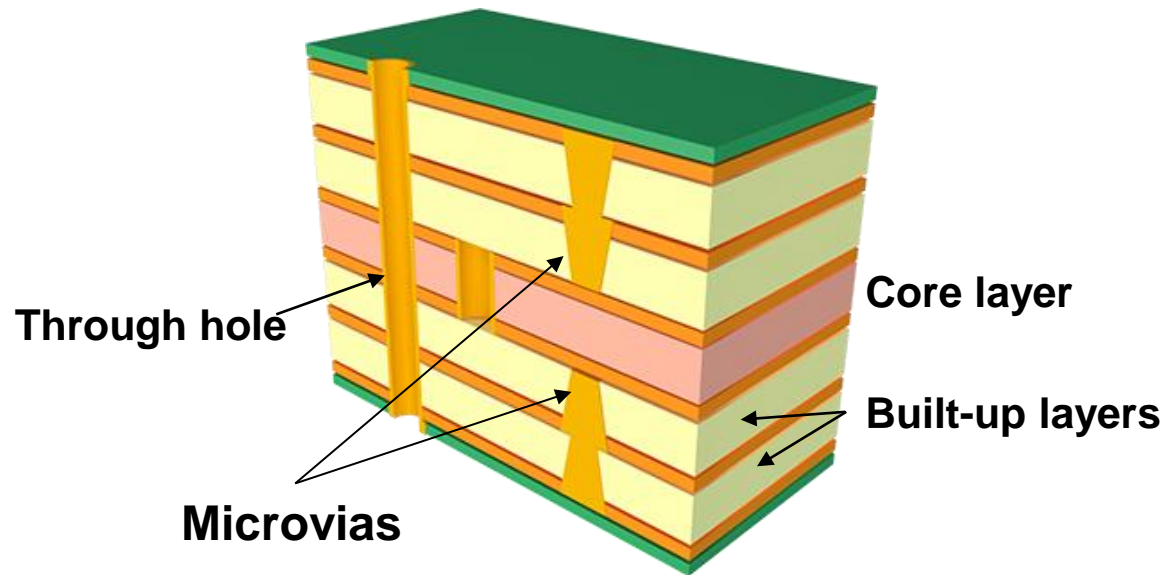
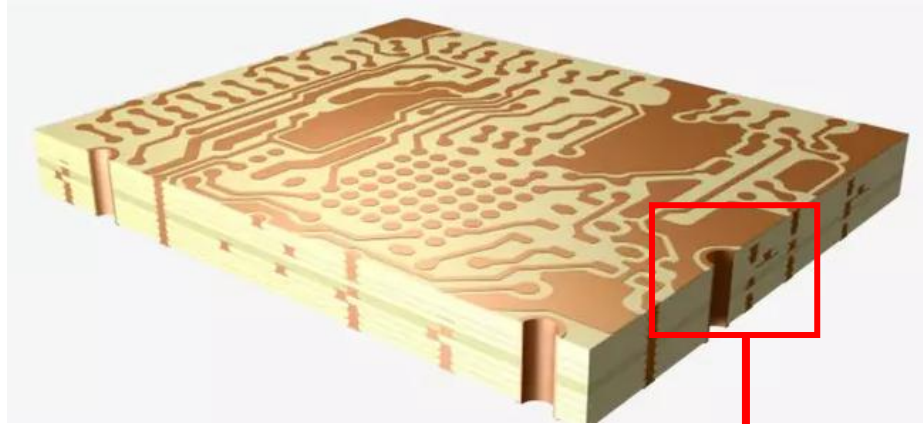
Hiroki Seto, Yuhei Kitahara, Kei Hashizume,

*Okuno Chemical Industries Co. Ltd.*

# Outline

1. Introduction
2. FEM simulation for three-layer stacked micro-vias
3. STEM/Atom probe analysis on nanovoids in e-less Cu
4. ToF-SIMS for e-less-Cu layer
5. Summary

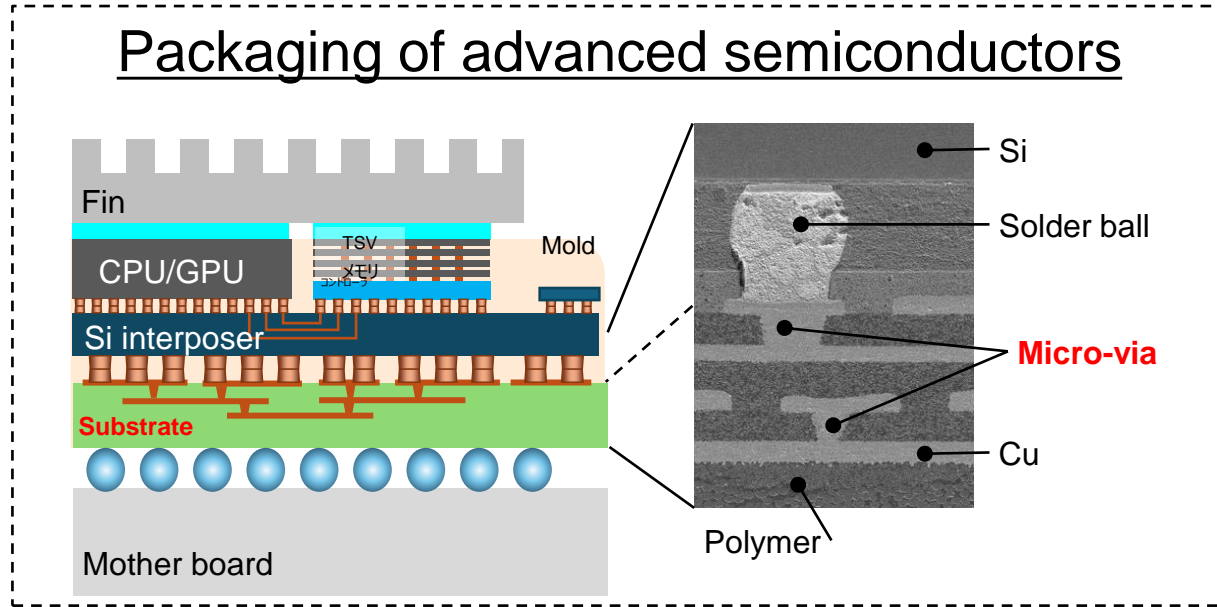
# Trends in high density interconnect of substrates



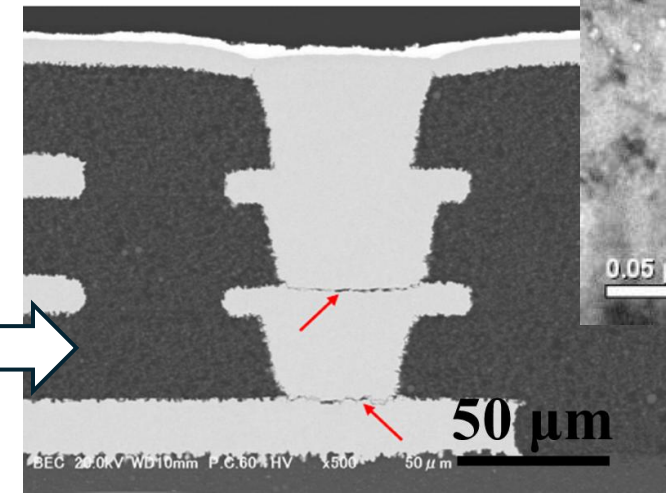
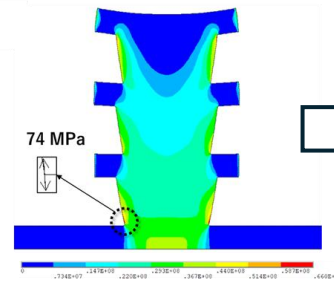
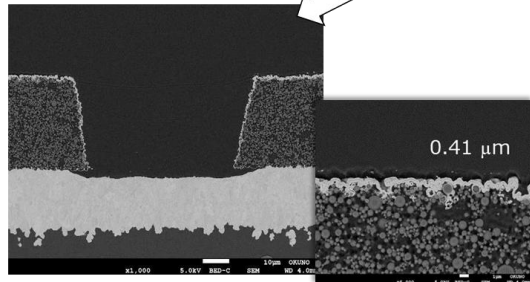
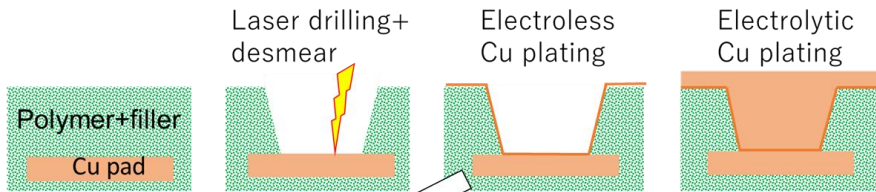
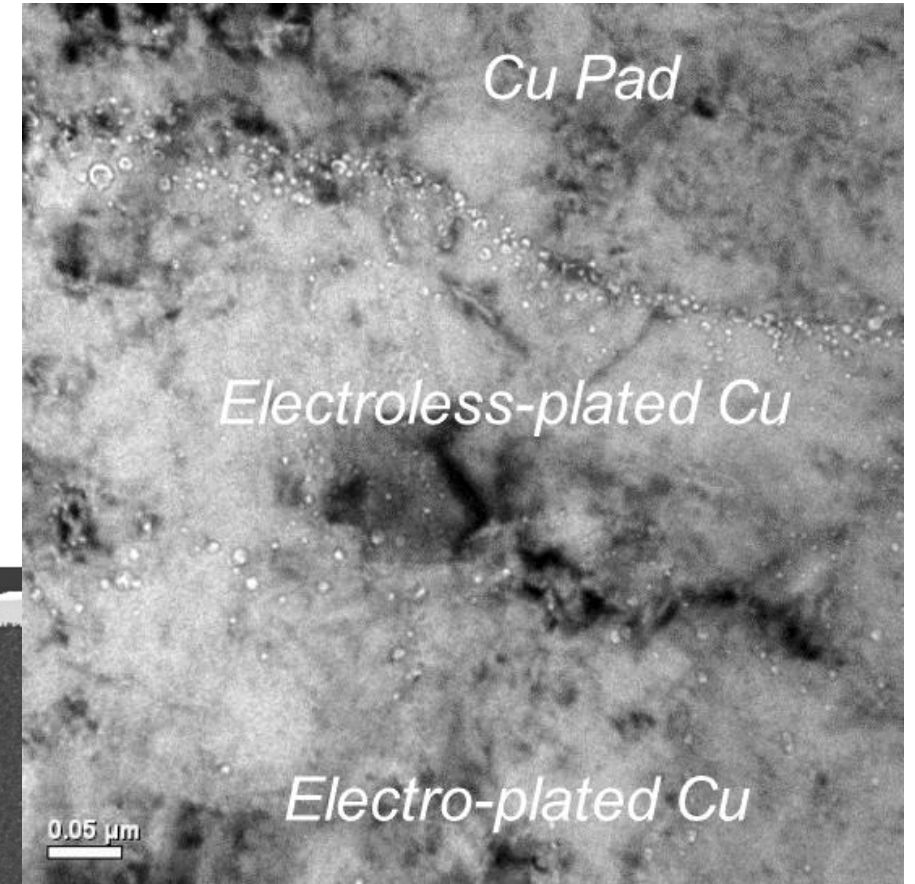
Shreya Dwarakanath May 2020

# Weak Micro-Via Concern of Substrates

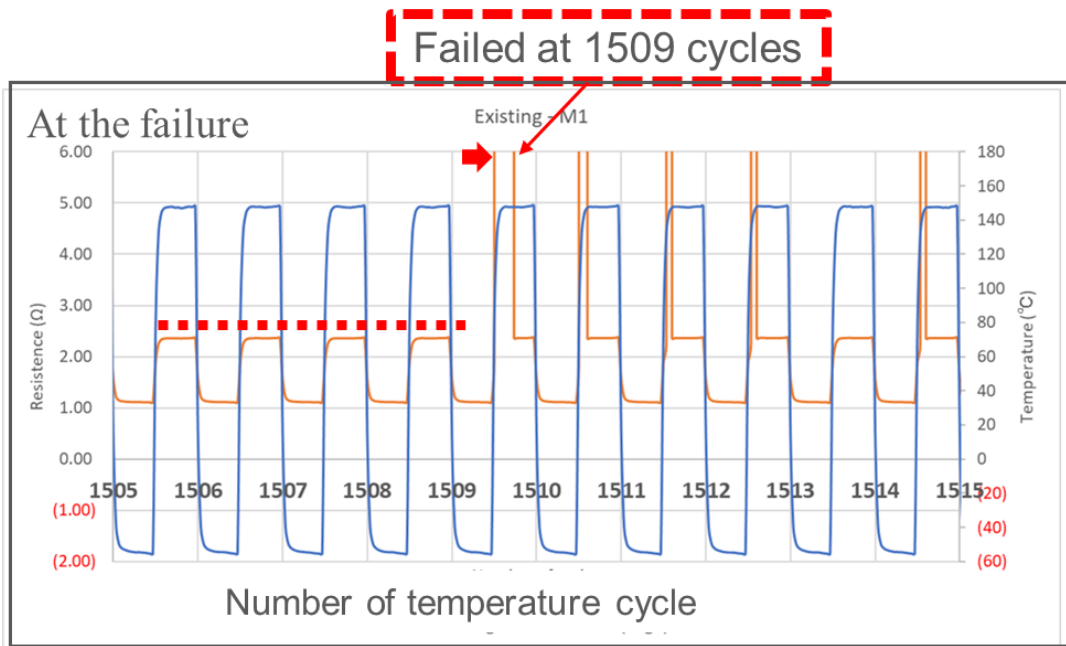
## Packaging of advanced semiconductors



## Nano voids in e-less Cu

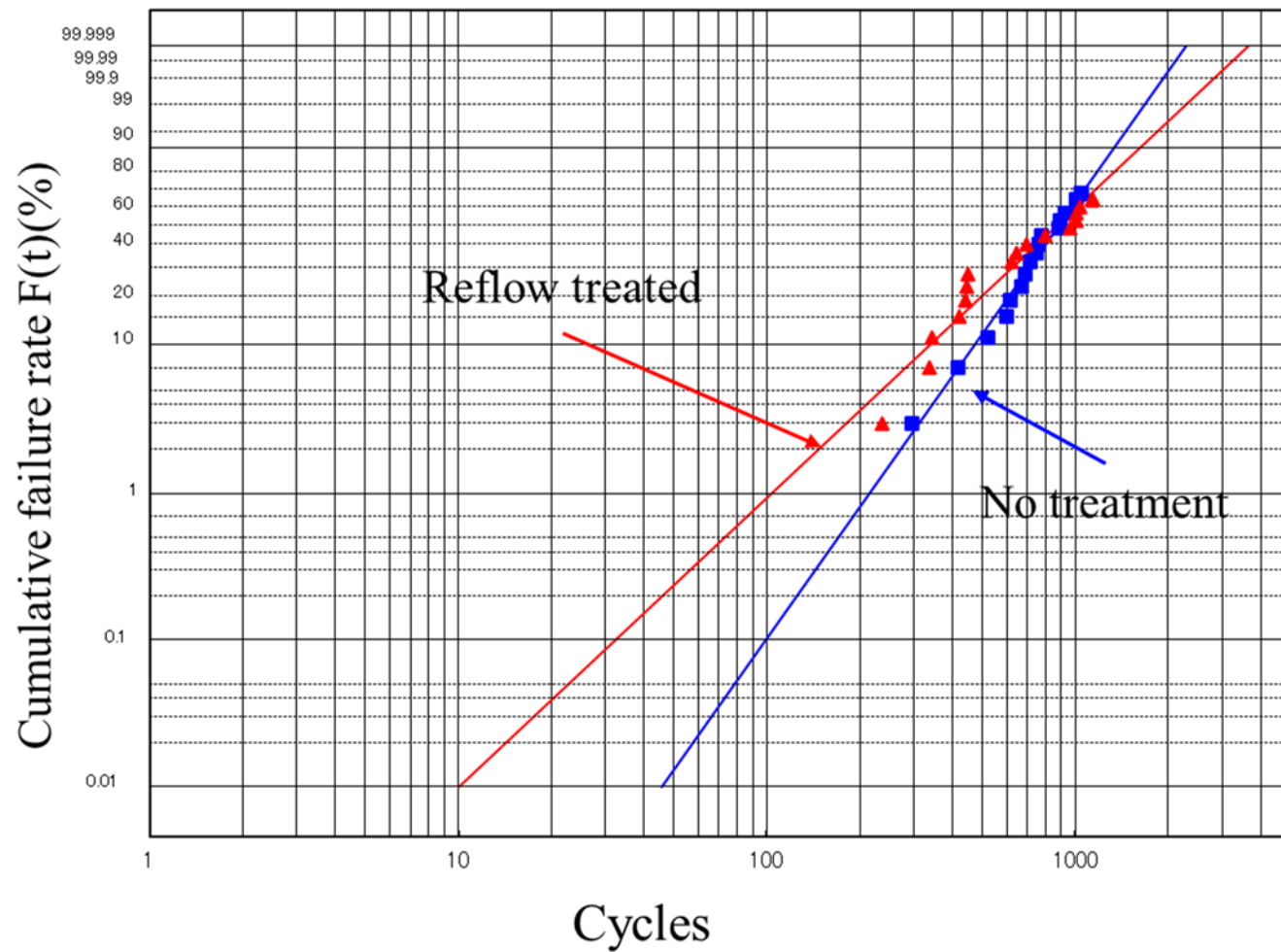


# Thermal shock failure



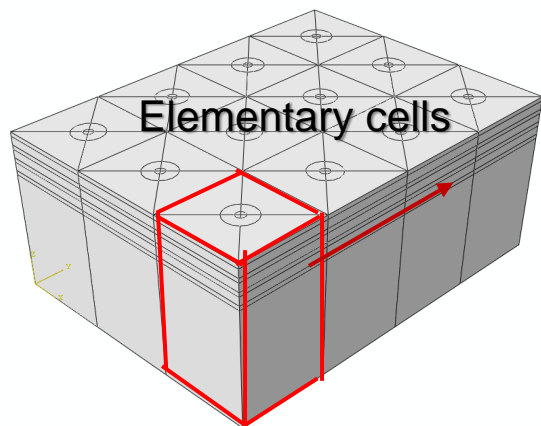
— Resistance — Temperature

-55°C~150°C



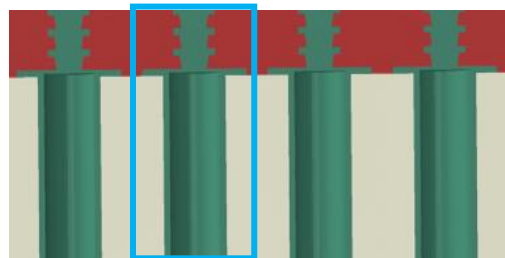
Reflow treatment enhances degradation

# FEM 3D Model of HDI substrate

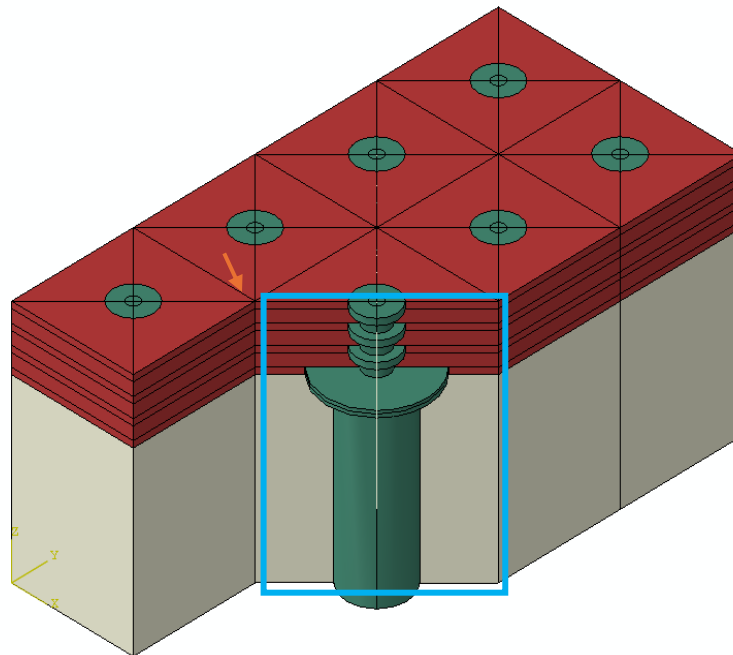


Elementary cells

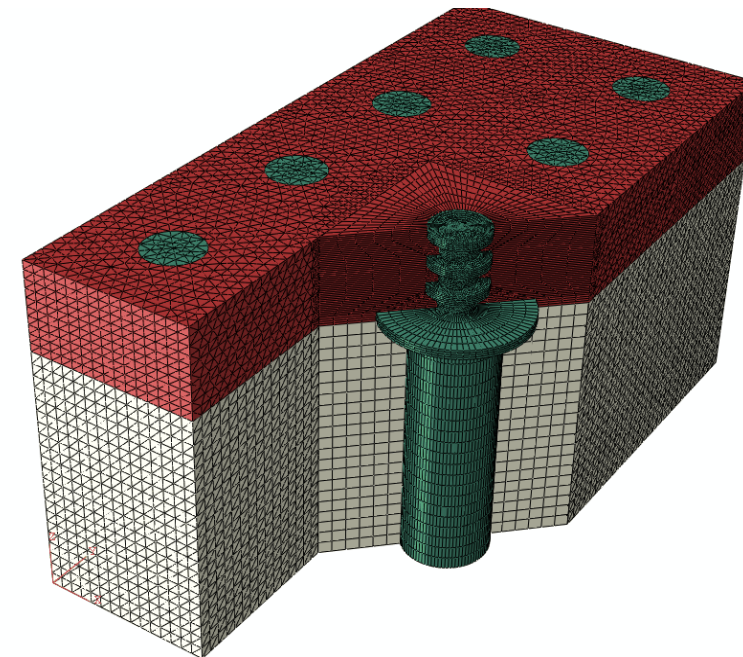
Sketch



Cross section view



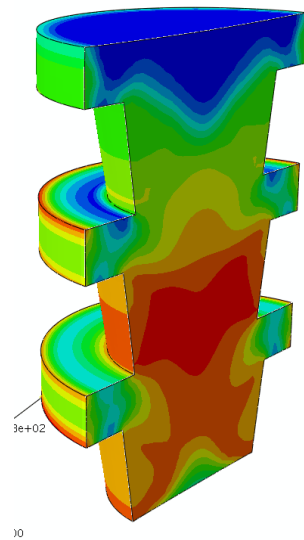
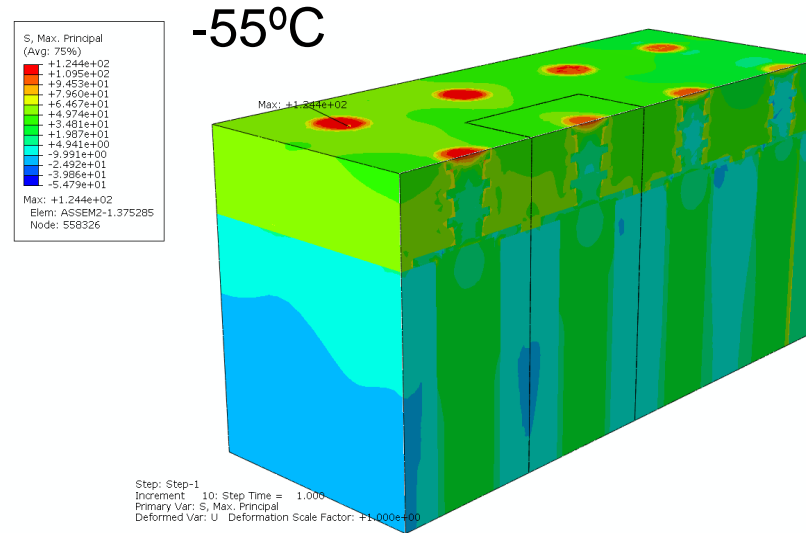
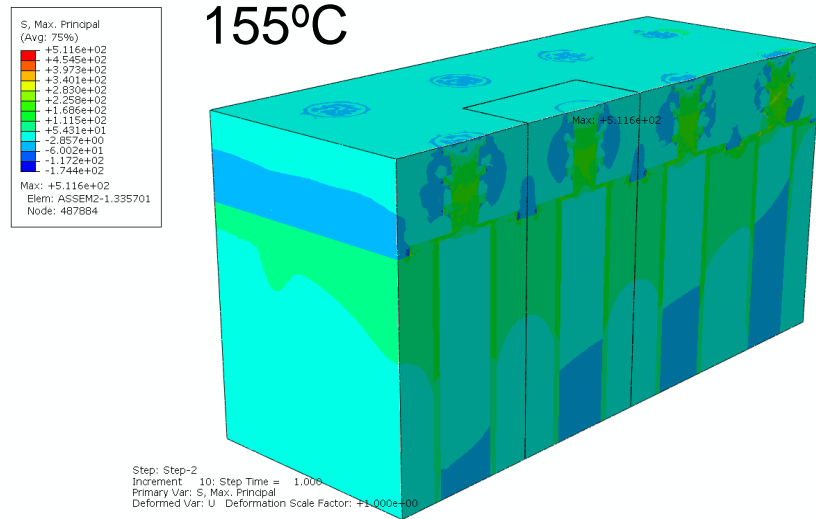
Internal view



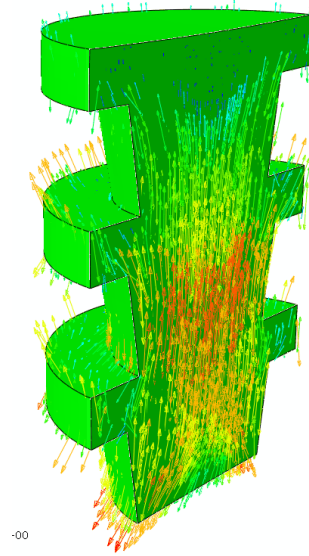
Mesh

-55°C ~ 150°C

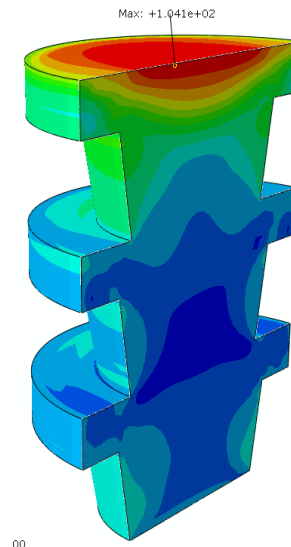
# Stresses in substrate at low and at high temperature



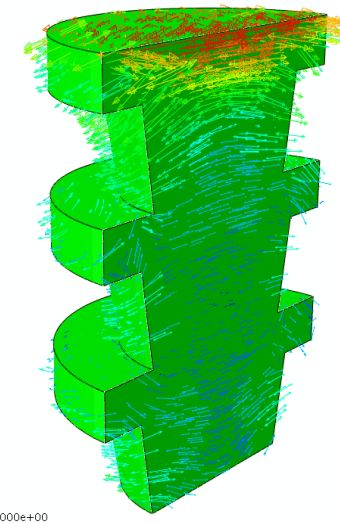
Stress distribution



Stress direction

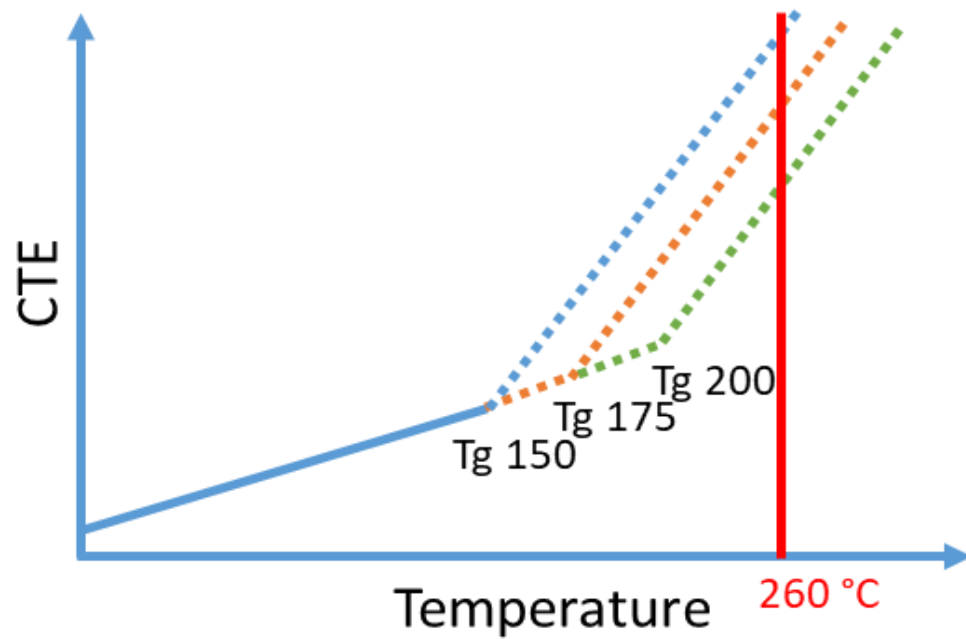


Stress distribution

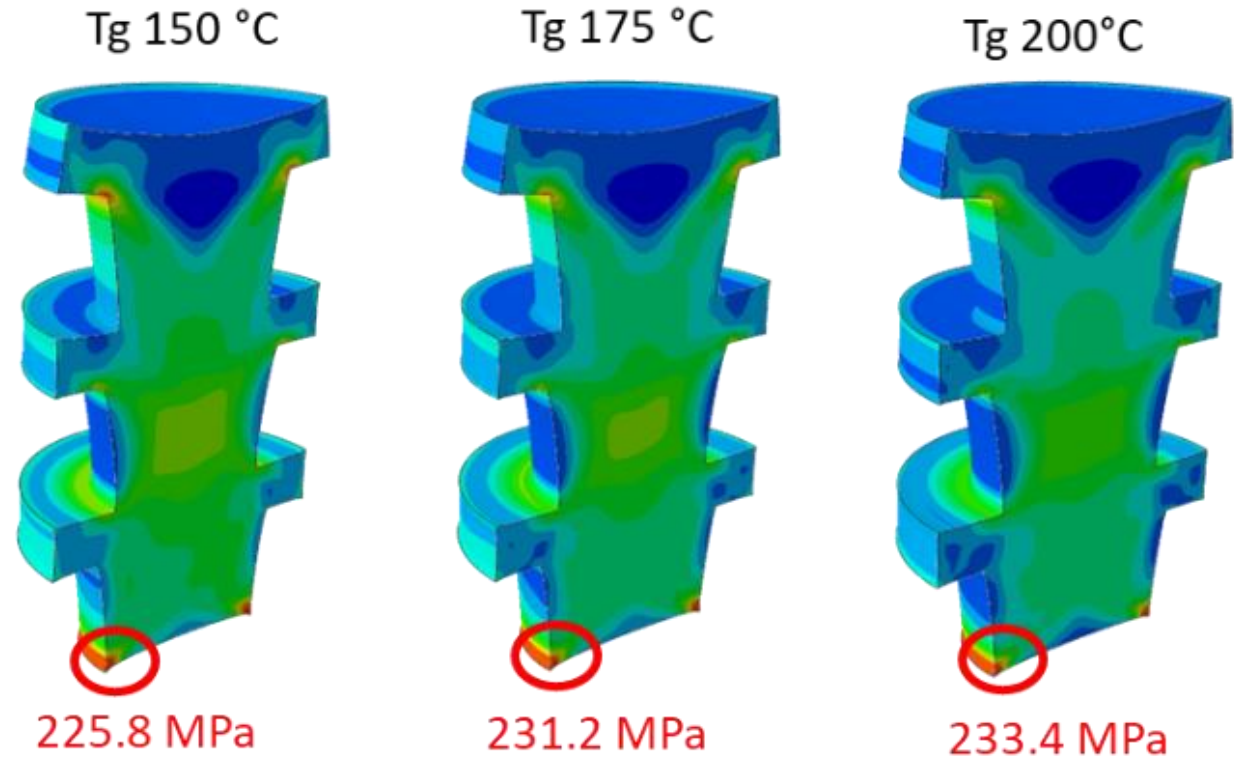


Stress direction

# Stresses in substrate with different T<sub>g</sub> temperature



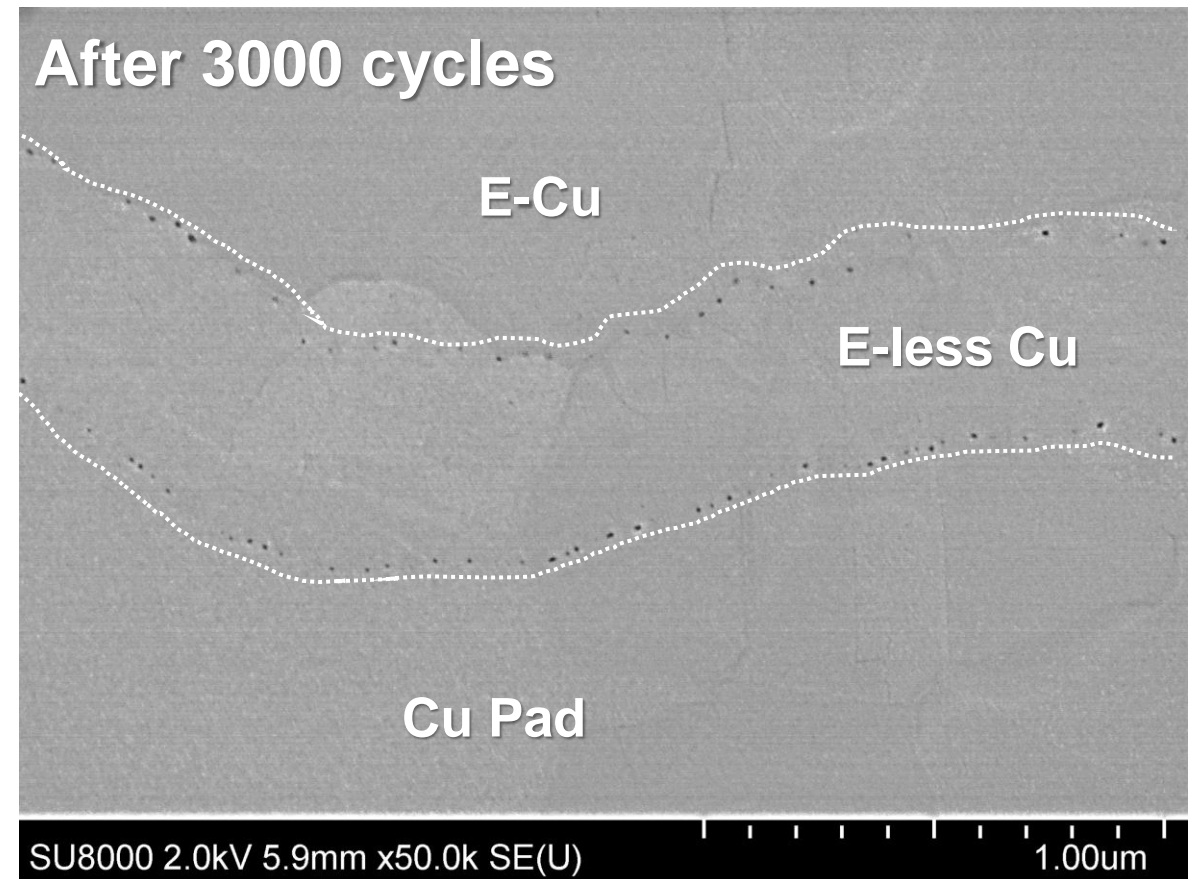
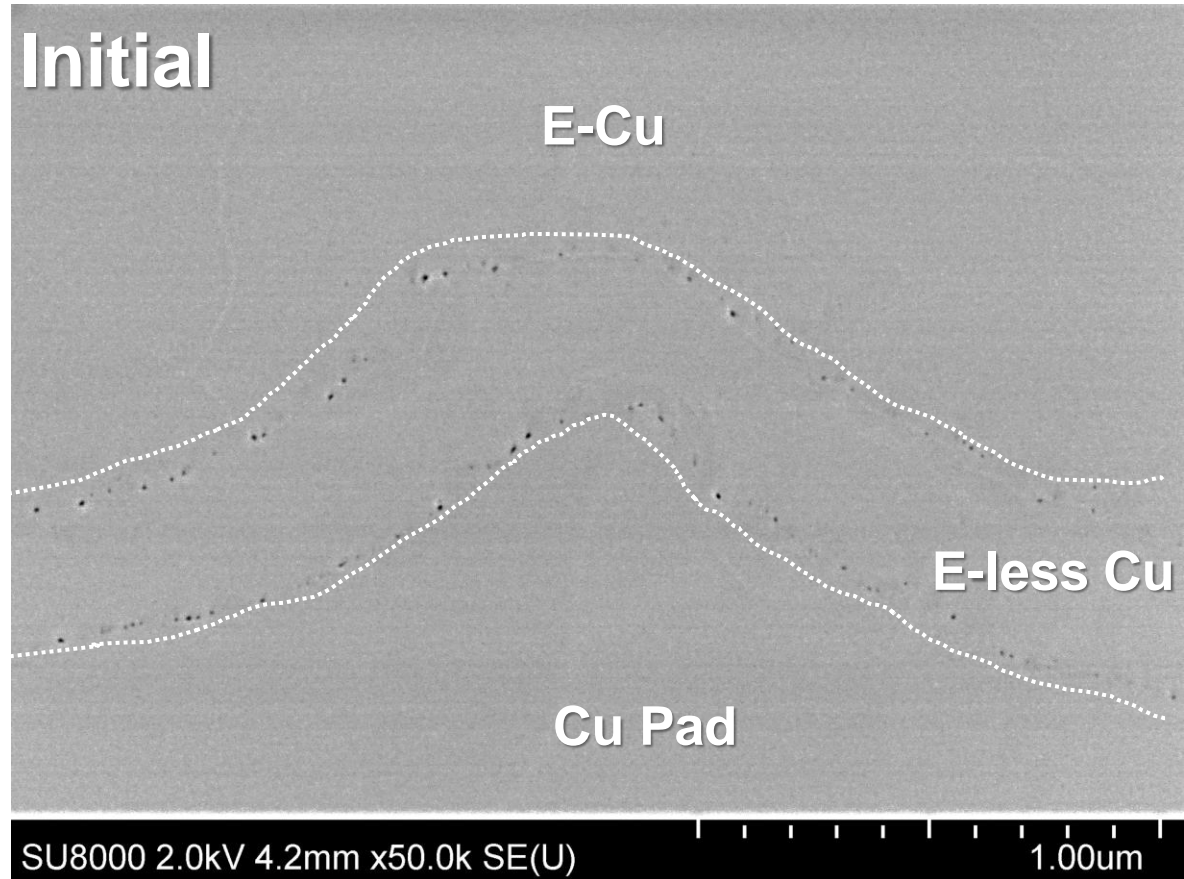
$$*CTE(@260C)=0.3489*T_g+22.67+1.3283*(260-T_g)$$



At higher temperature above T<sub>g</sub> of Resin materials, stress becomes stronger at the edge corner of the bottom of the 3-layer stacked micro-via.

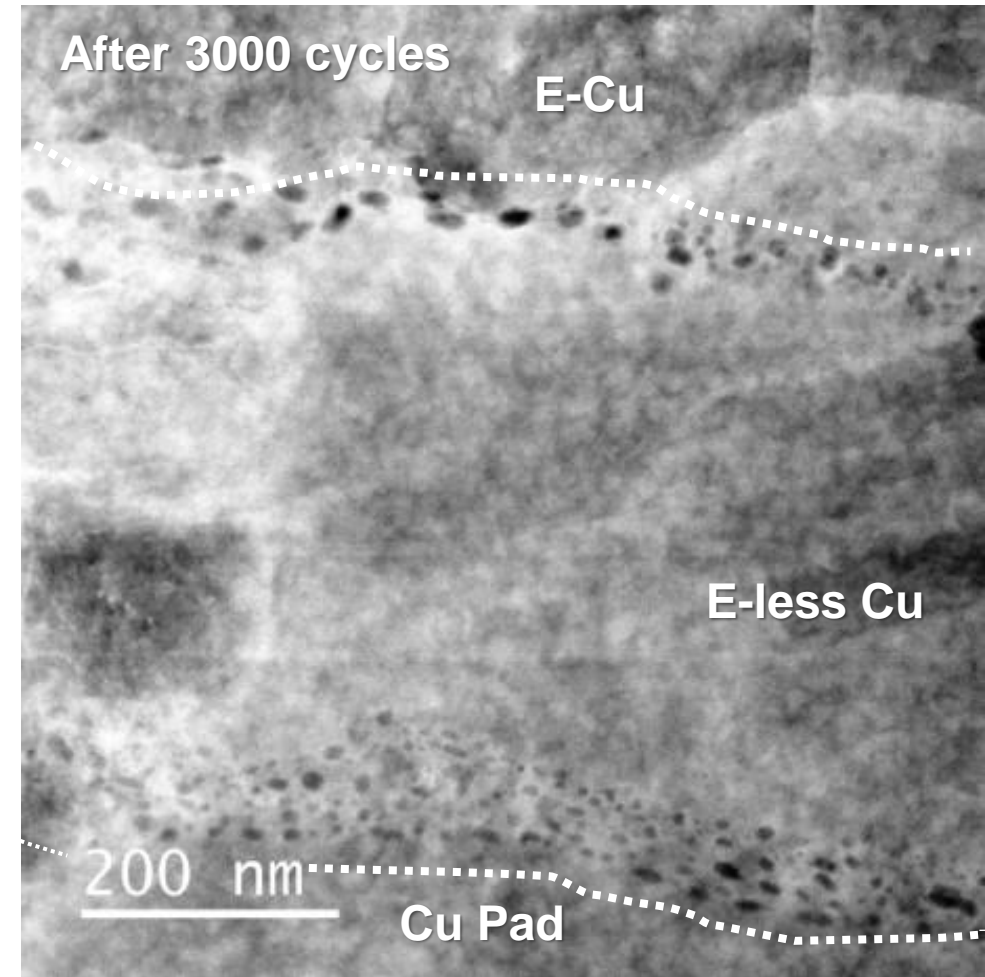
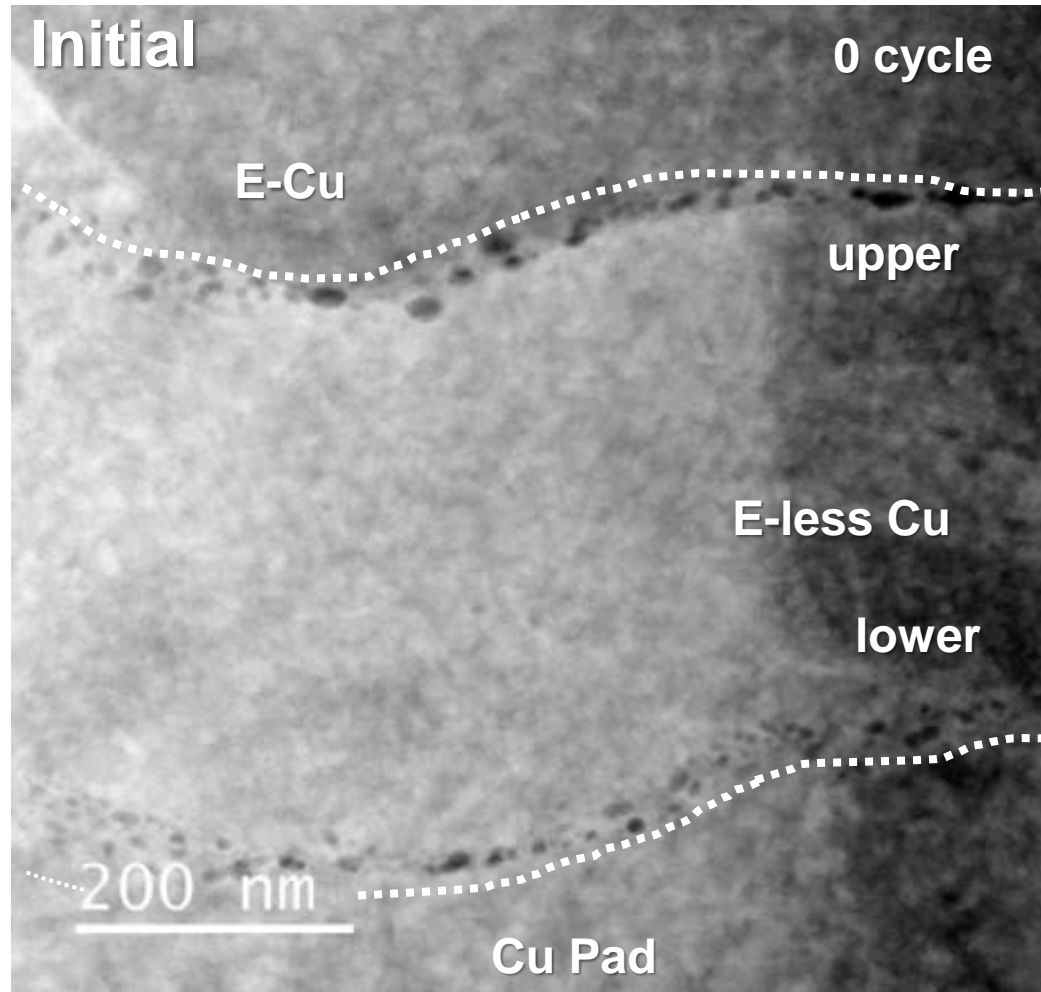
Stress sometimes induced and causes the destruction of micro-via.

# Low acceleration voltage SEM observation of e-less Cu layer



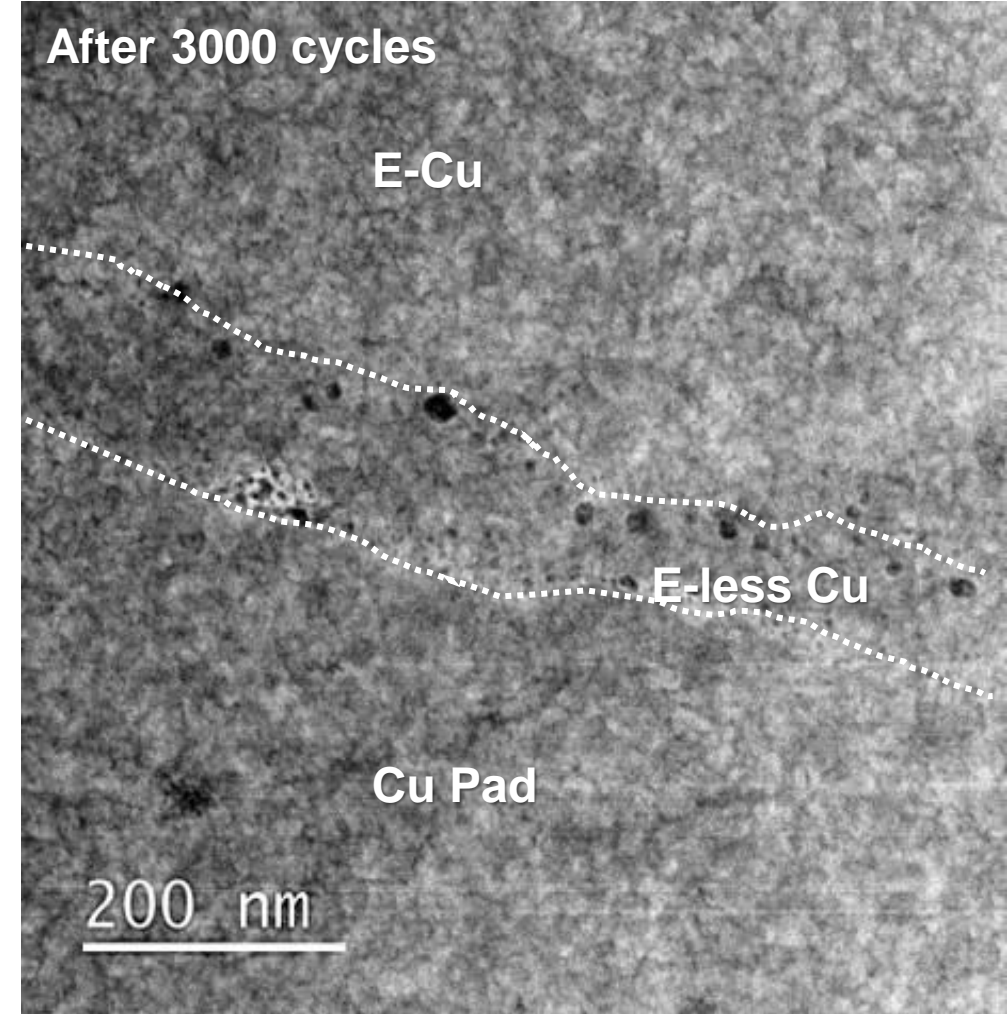
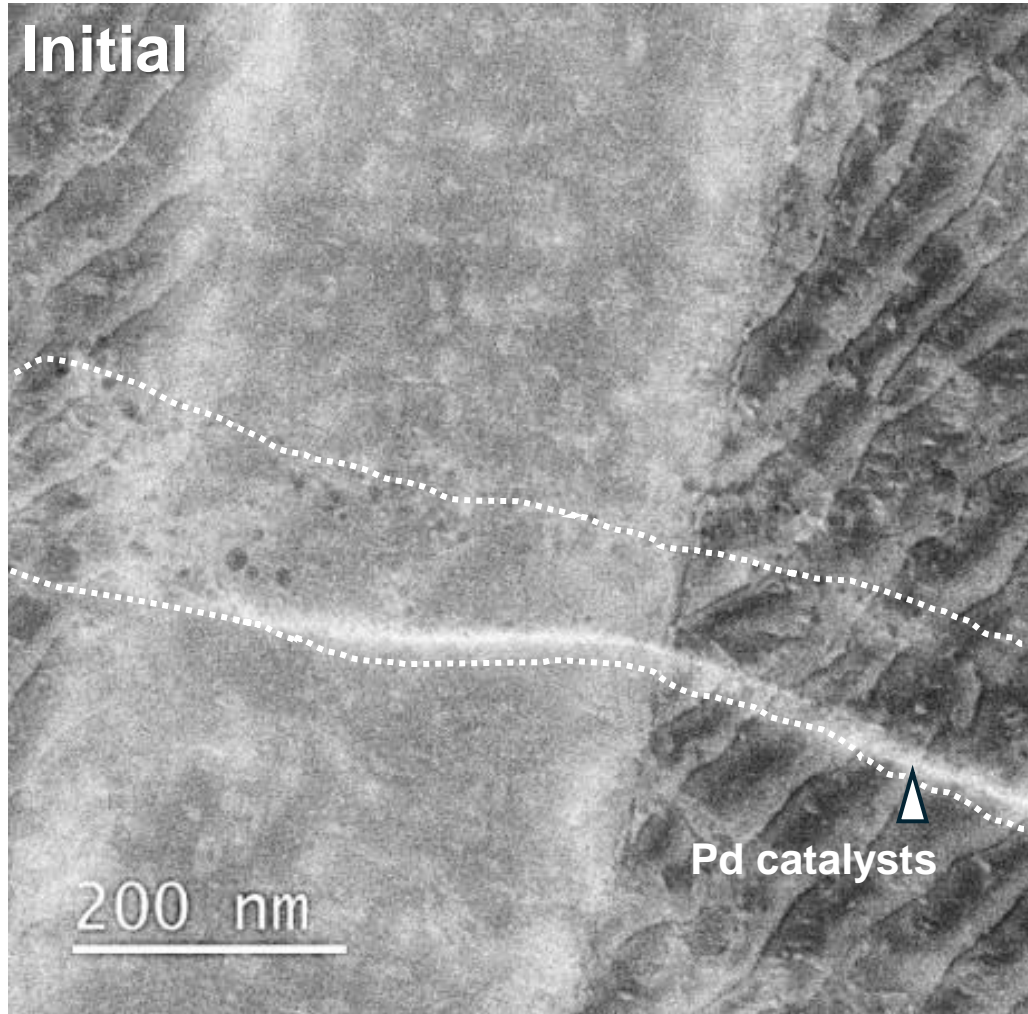
SEM  $V_{acc} = 1-2$  kV

# HAADF-STEM Observation of e-less Cu layer



STEM  $V_{acc} = 200$  kV

# HAADF-STEM Observation of e-less Cu layer for FLET

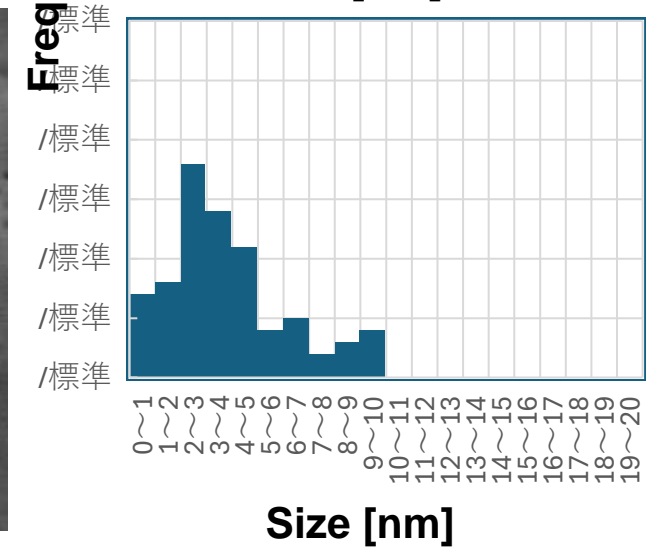
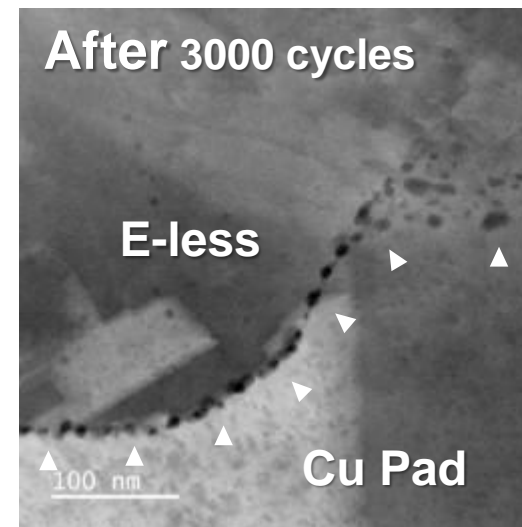
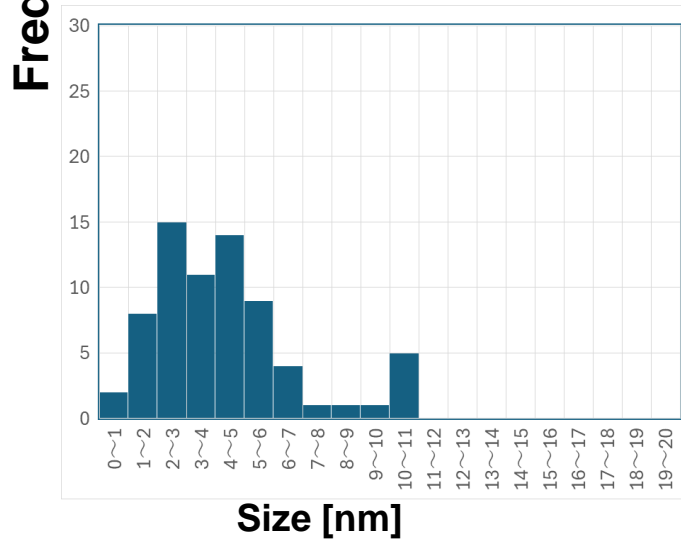
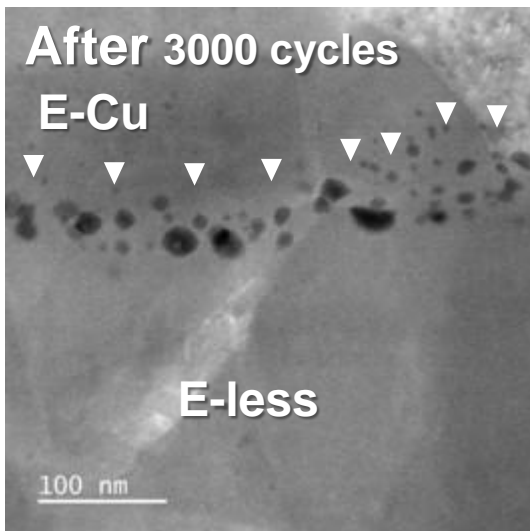
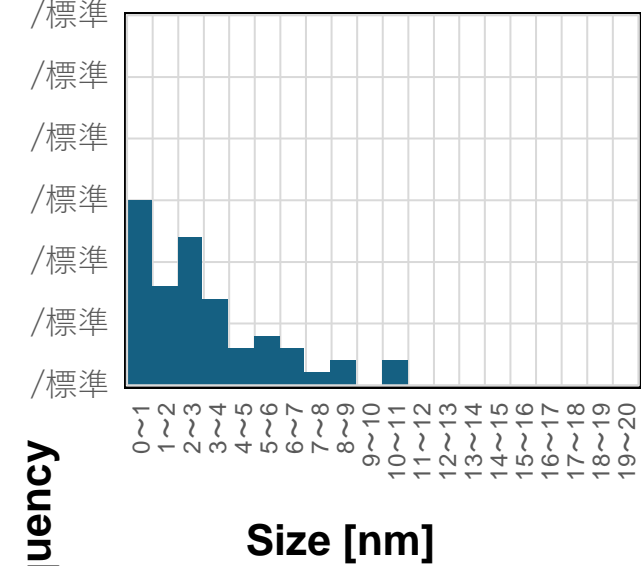
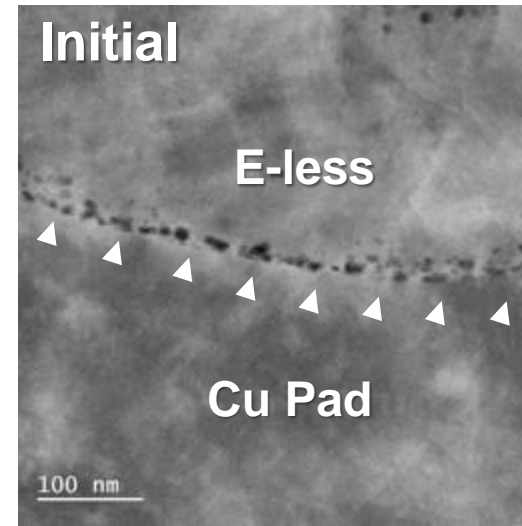
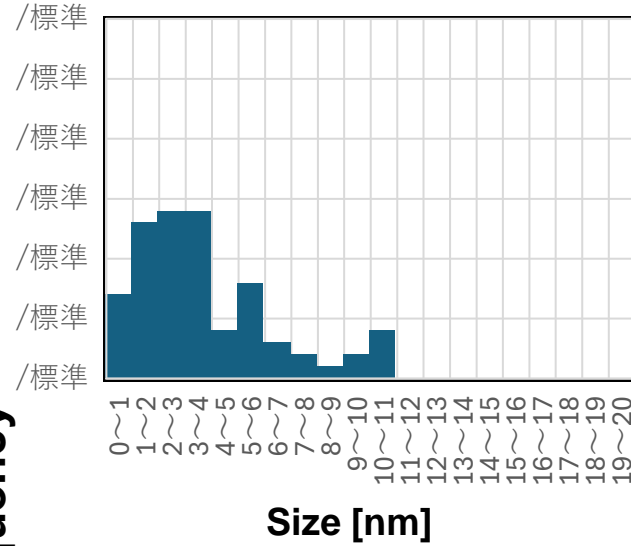
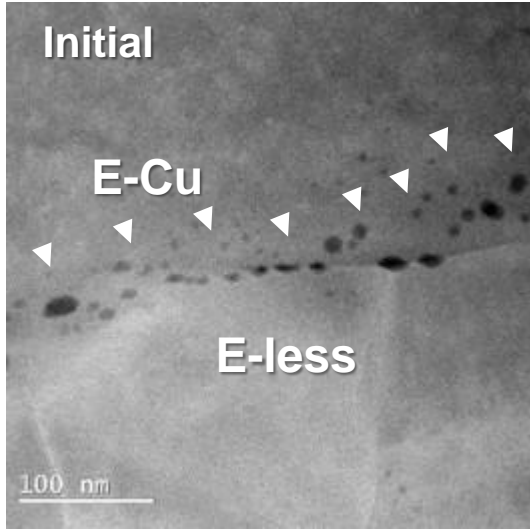


STEM  $V_{acc} = 200$  kV

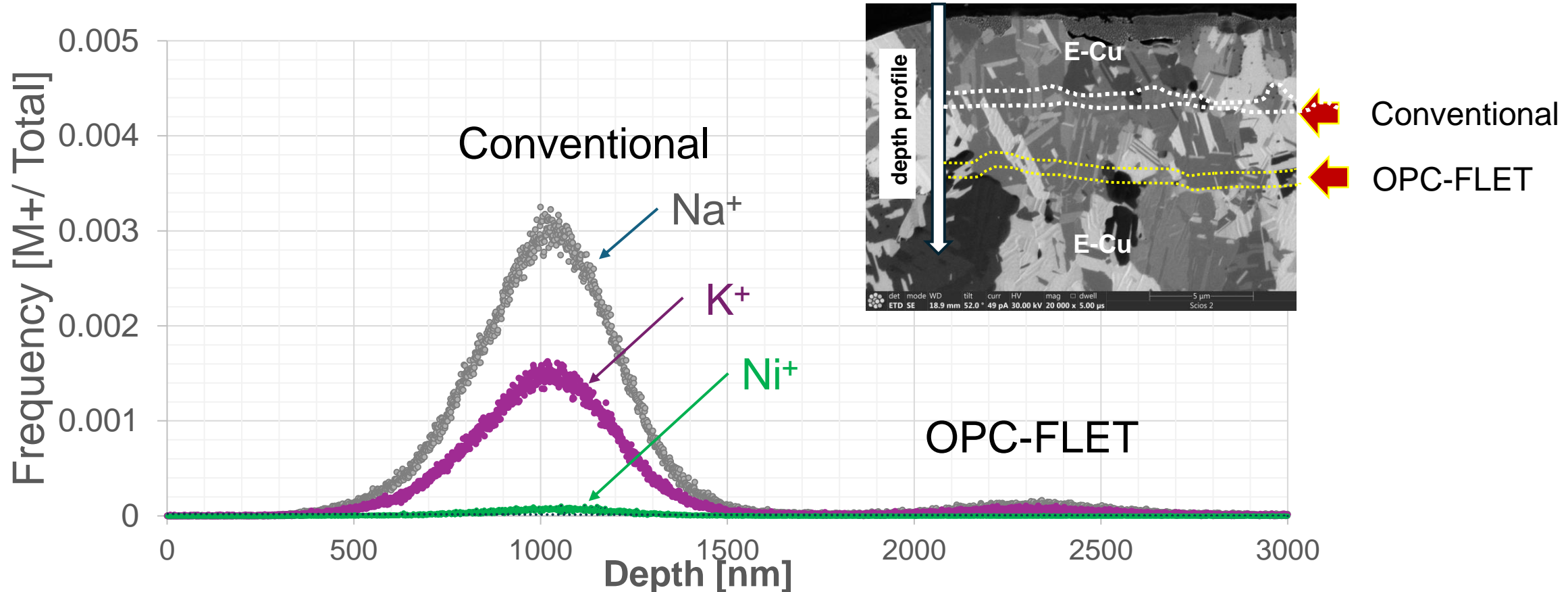
# Distribution of nanovoids

Upper

Lower

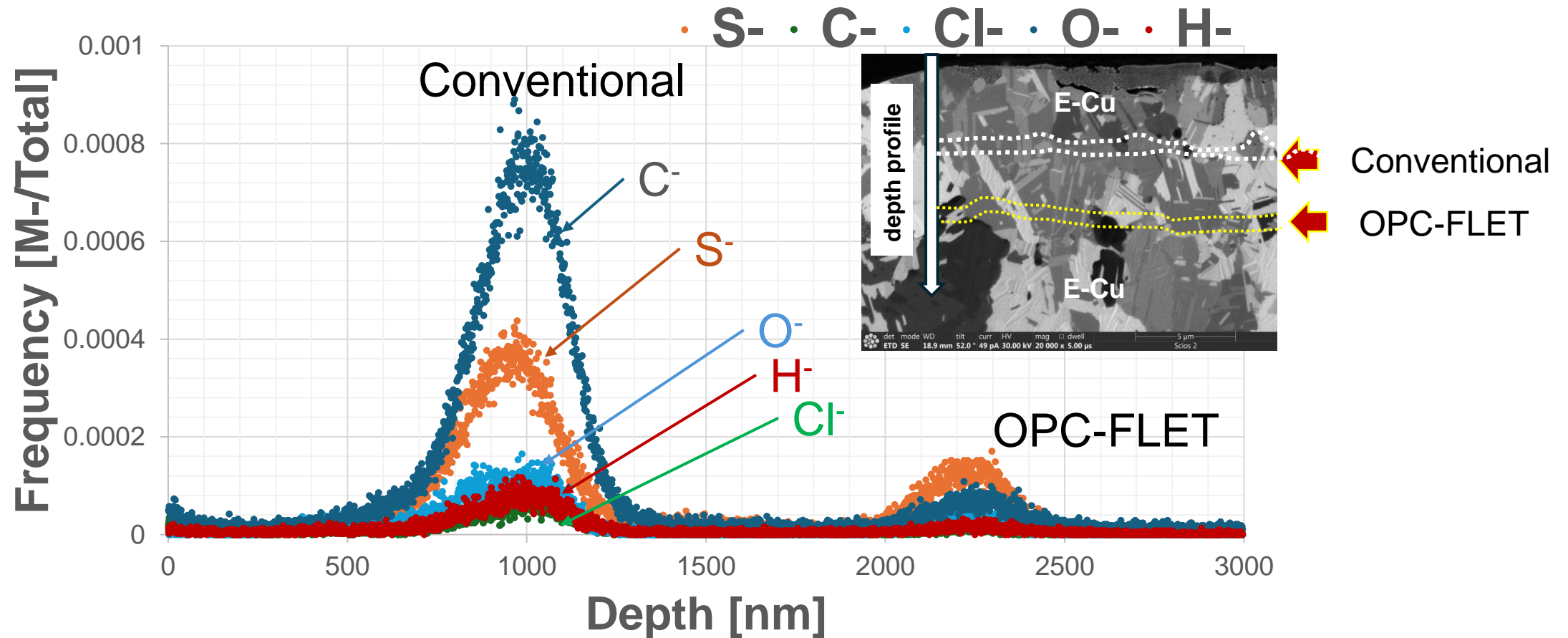


# SIMS measurement across electro/electroless plated layers



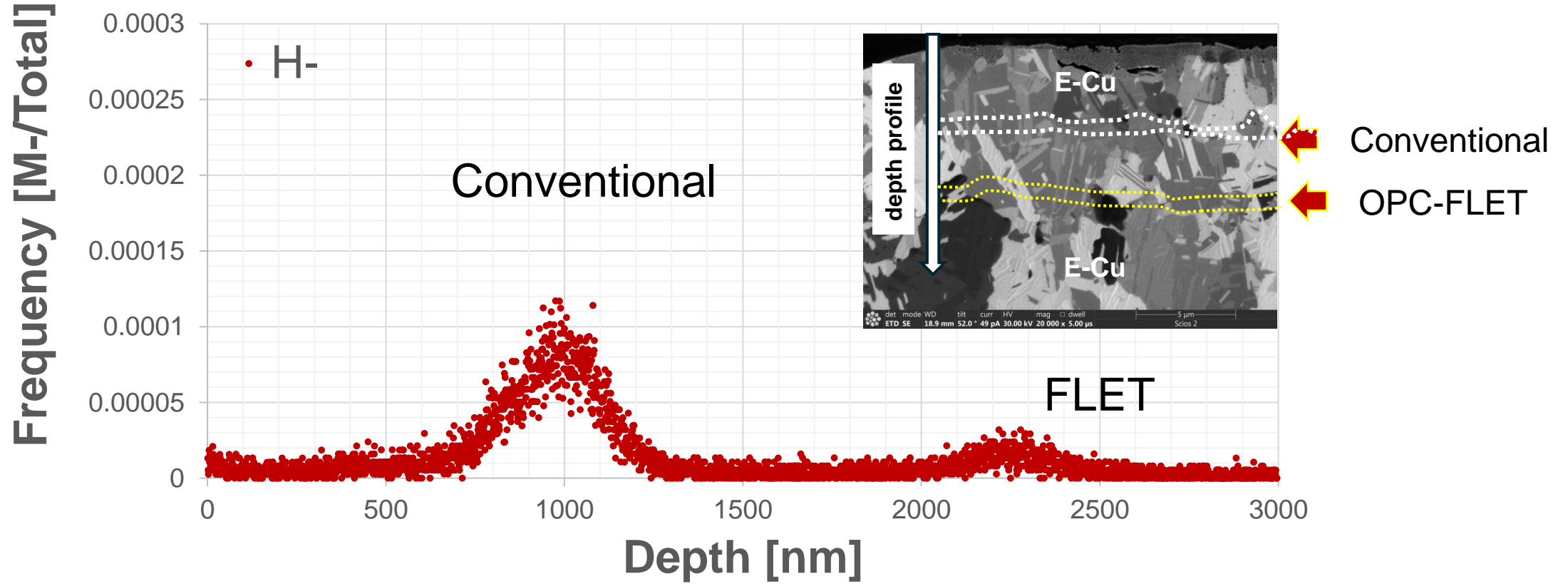
- Na<sup>+</sup> and K<sup>+</sup> ions are increasing around the electroless Cu layer

# SIMS measurement across electro/electroless plated layers

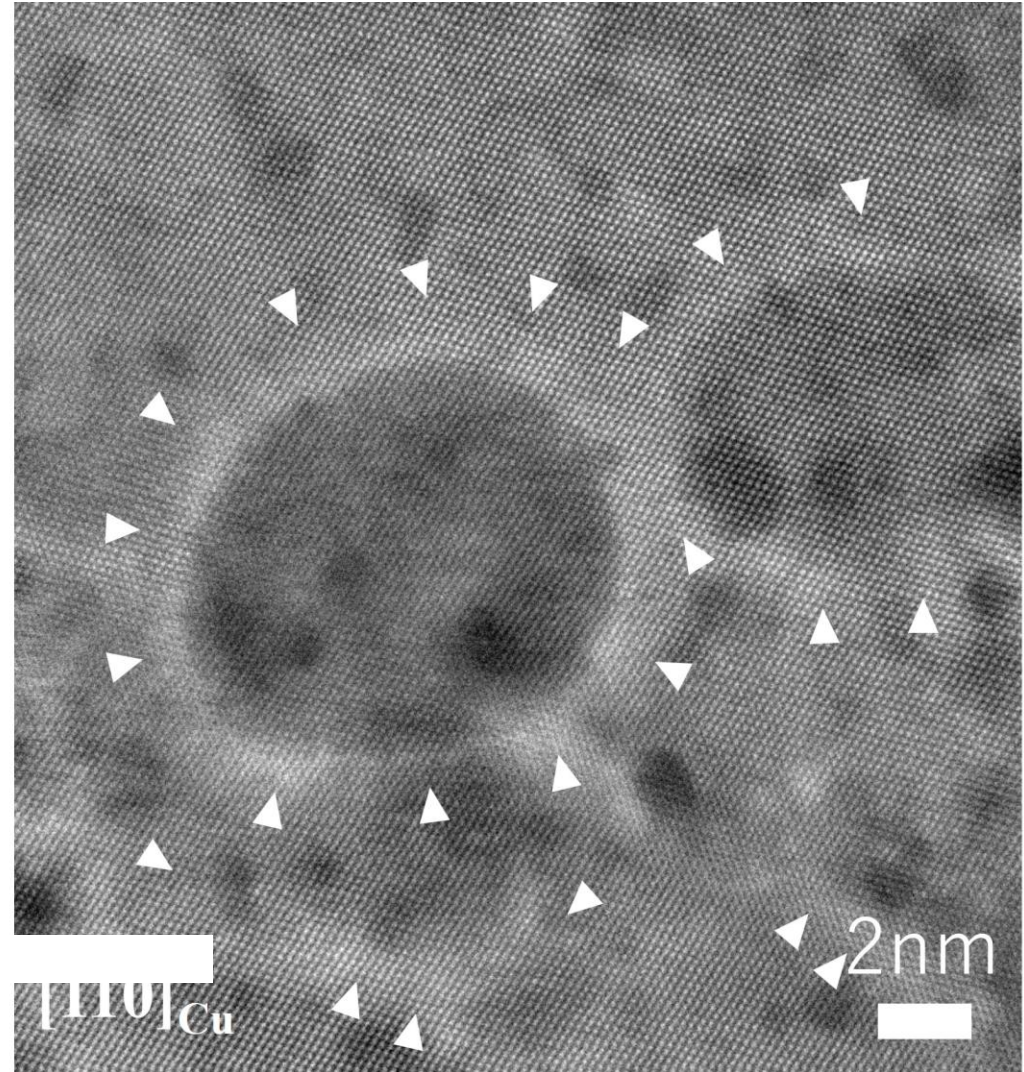
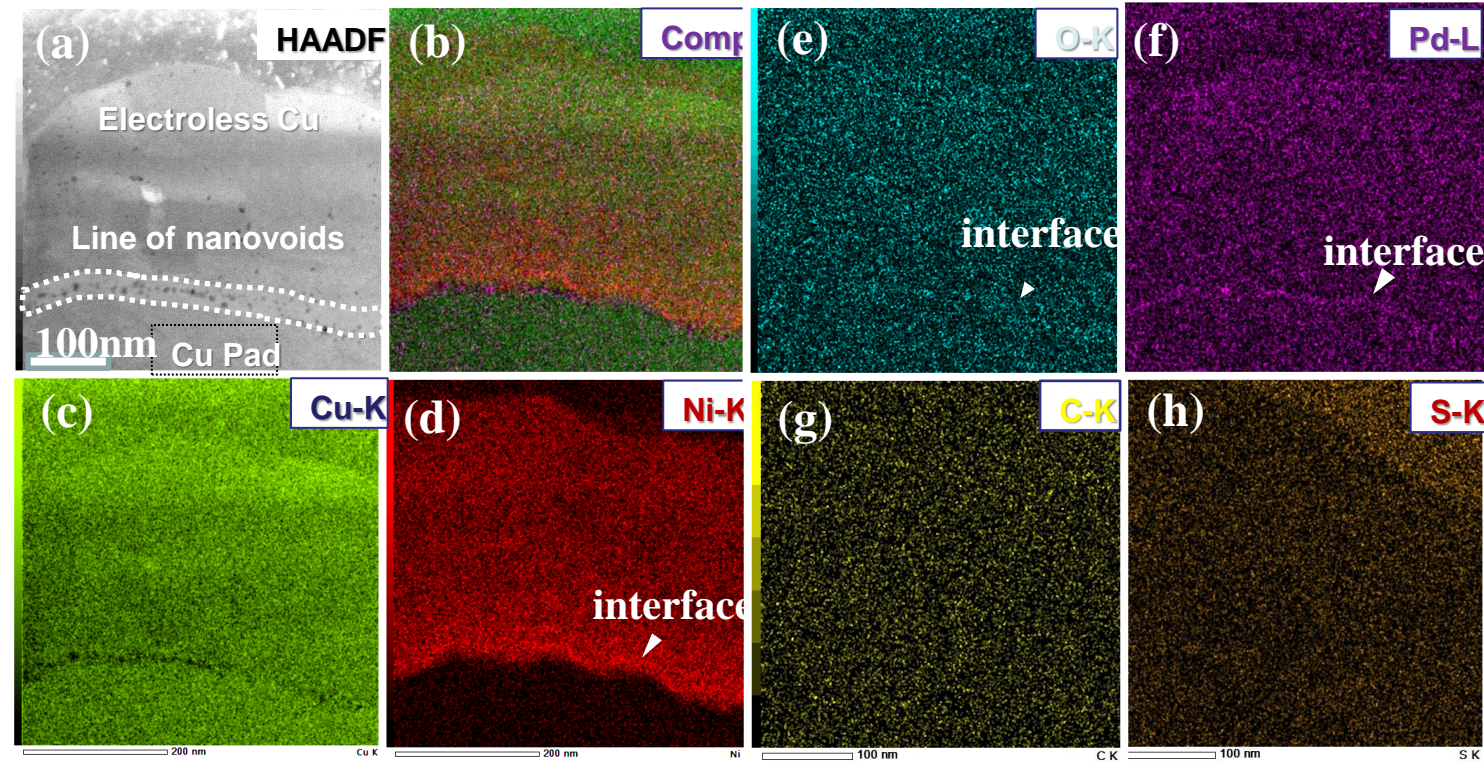


- S<sup>-</sup> , C<sup>-</sup> , Cl<sup>-</sup>, O<sup>-</sup> and H<sup>-</sup> ions are high in the electroless Cu layer

# H- profile across e-less cu layers



# STEM-EDS maps of traditionally processed E-less Cu layer



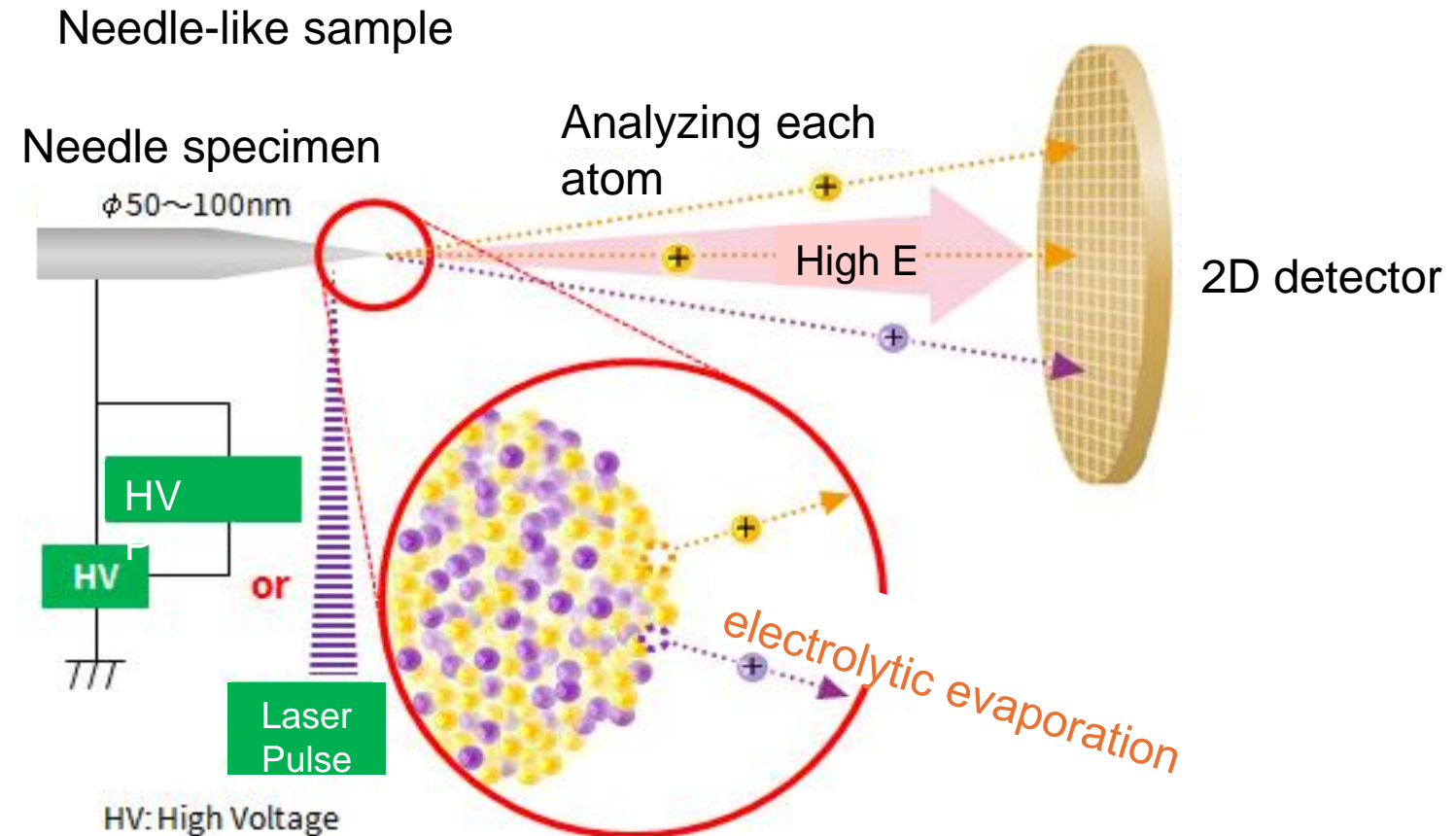
Nishijima et als, ECTC(2023)

K.Suganuma, F3D, Osaka University

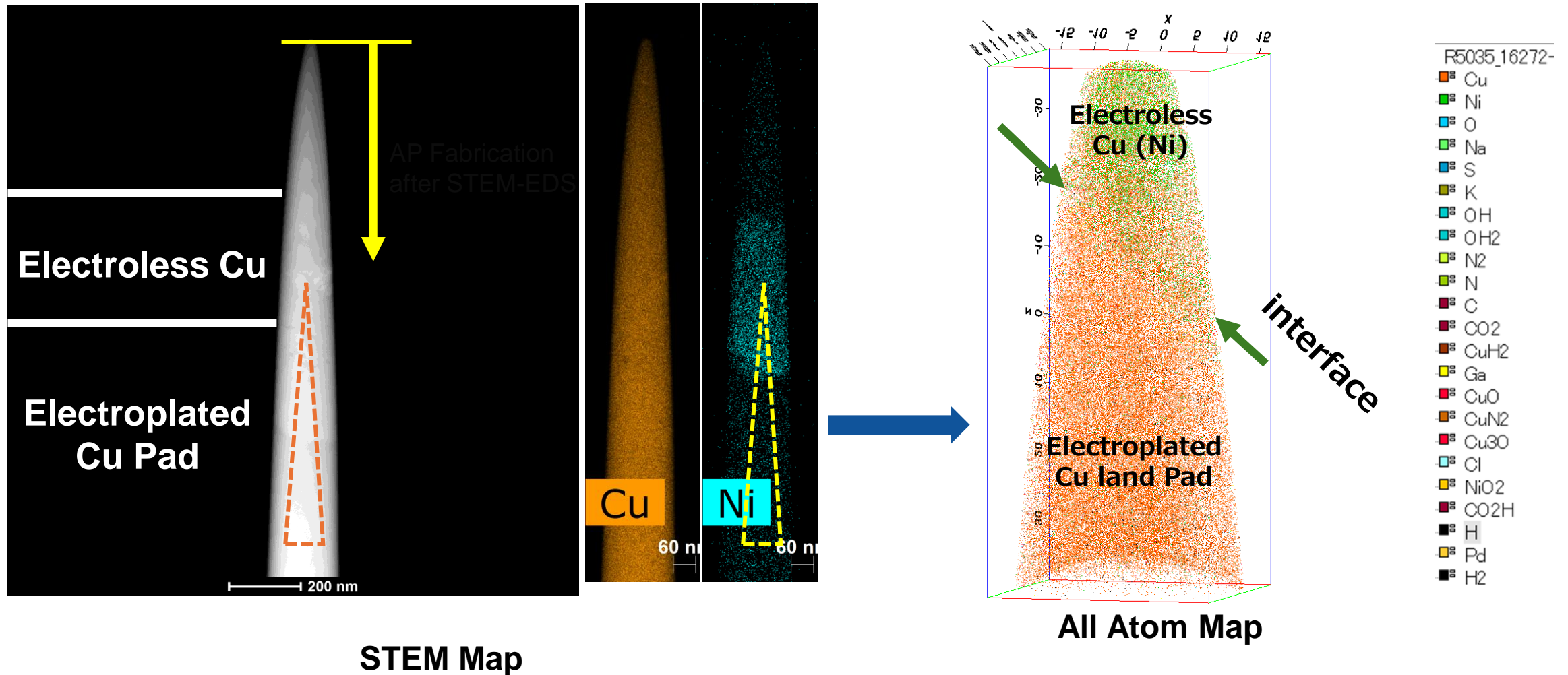
# Atom Probe Tomography

1. HV is applied to a needle-like sample, a high Electric Field is generated at the tip of it, causing the field evaporation
2. The atomic arrangement of the field-evaporated ions is determined by a 2D detector.
3. The ion species is also identified based on the flight time.
4. 3D atomic distribution can be obtained and 3D arrangement reconstructed.

## Schematic of 3DAP



# Analysis for nanovoids in lower electroless layer

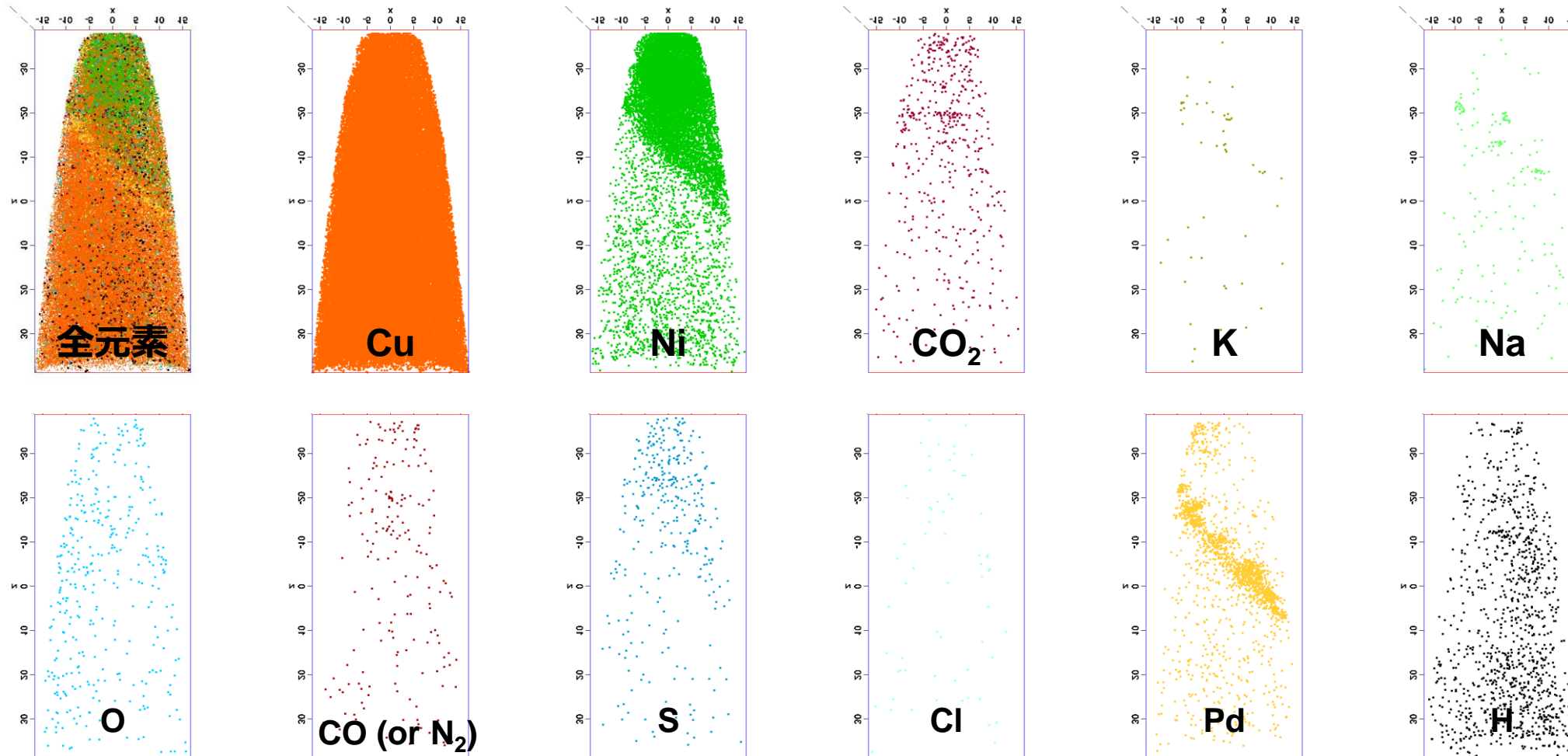


**STEM Map**

**All Atom Map**

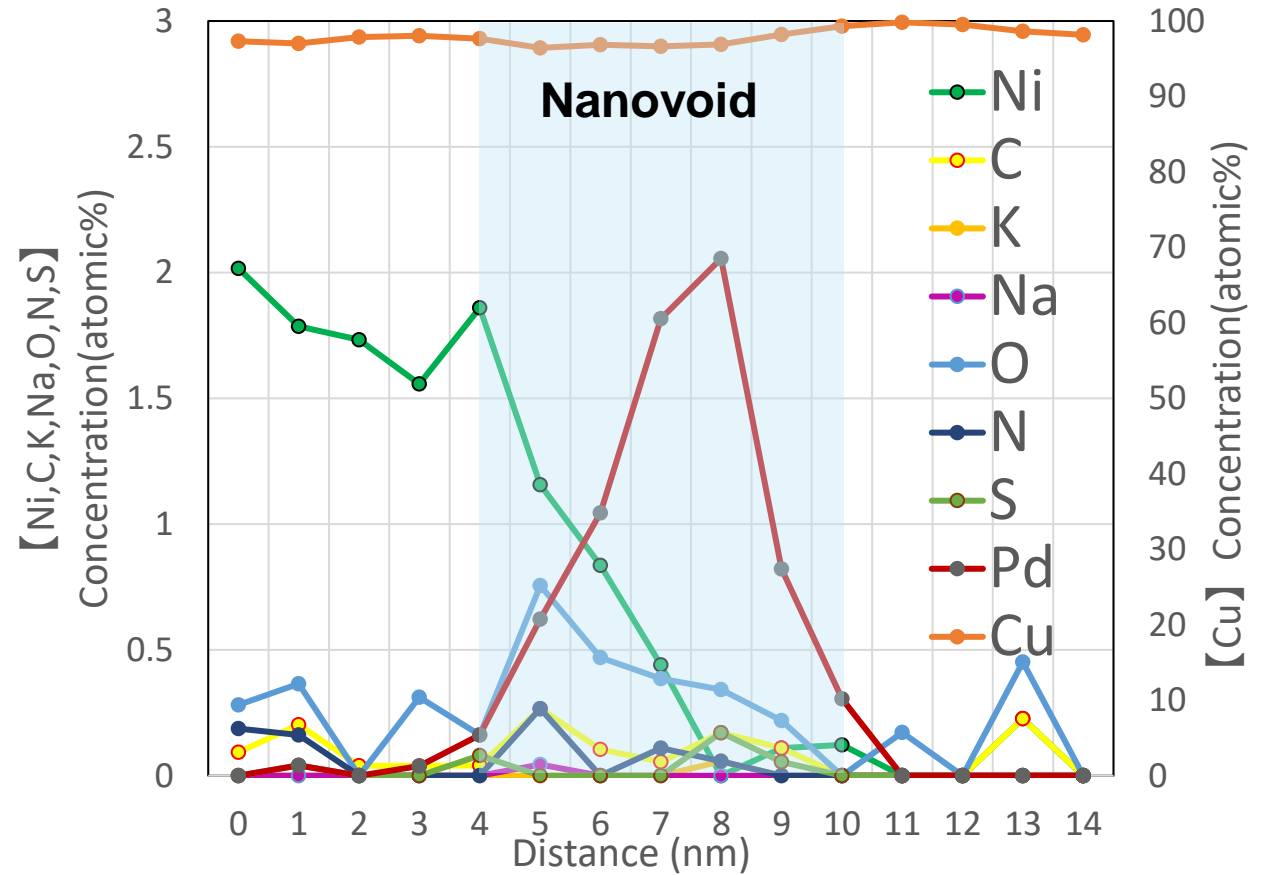
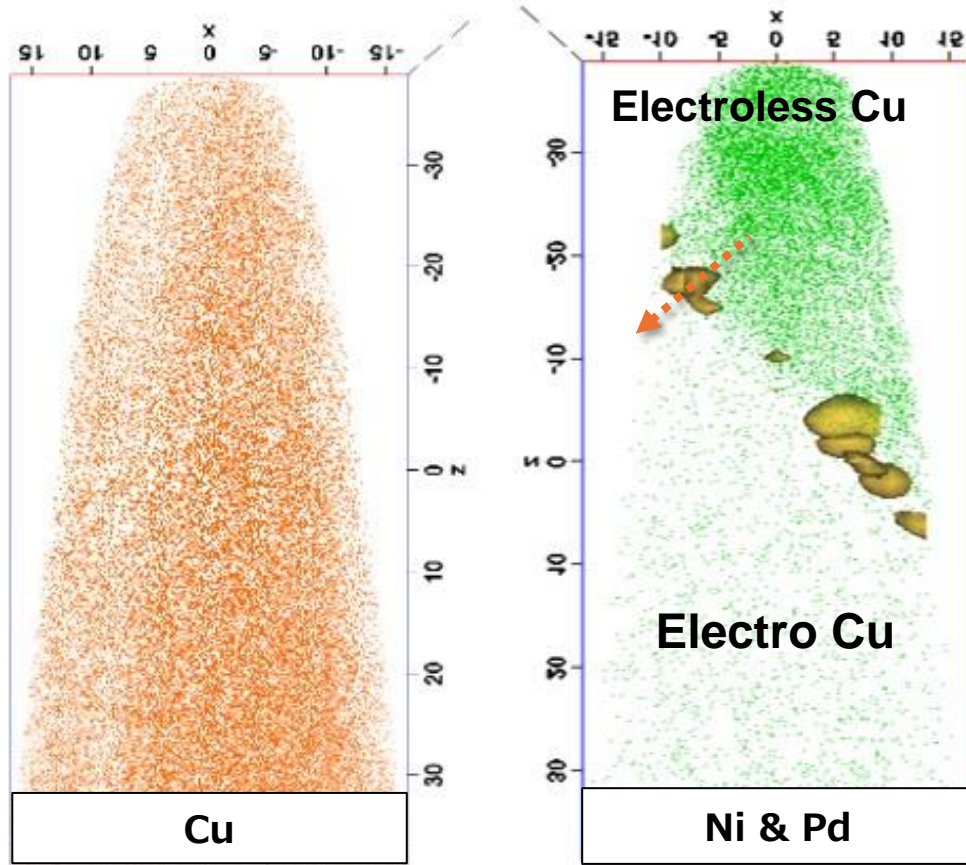
Check the electroless layer which contains Ni element by STEM-EDS measurement and prepare needle like Atom Probe sample at the  $\Delta$  position by using FIB

# Analysis for nanovoids in lower electroless layer



- Ni, K, Na, and Pd show characteristic distribution compared to other elements

# Pd across the nanovoid

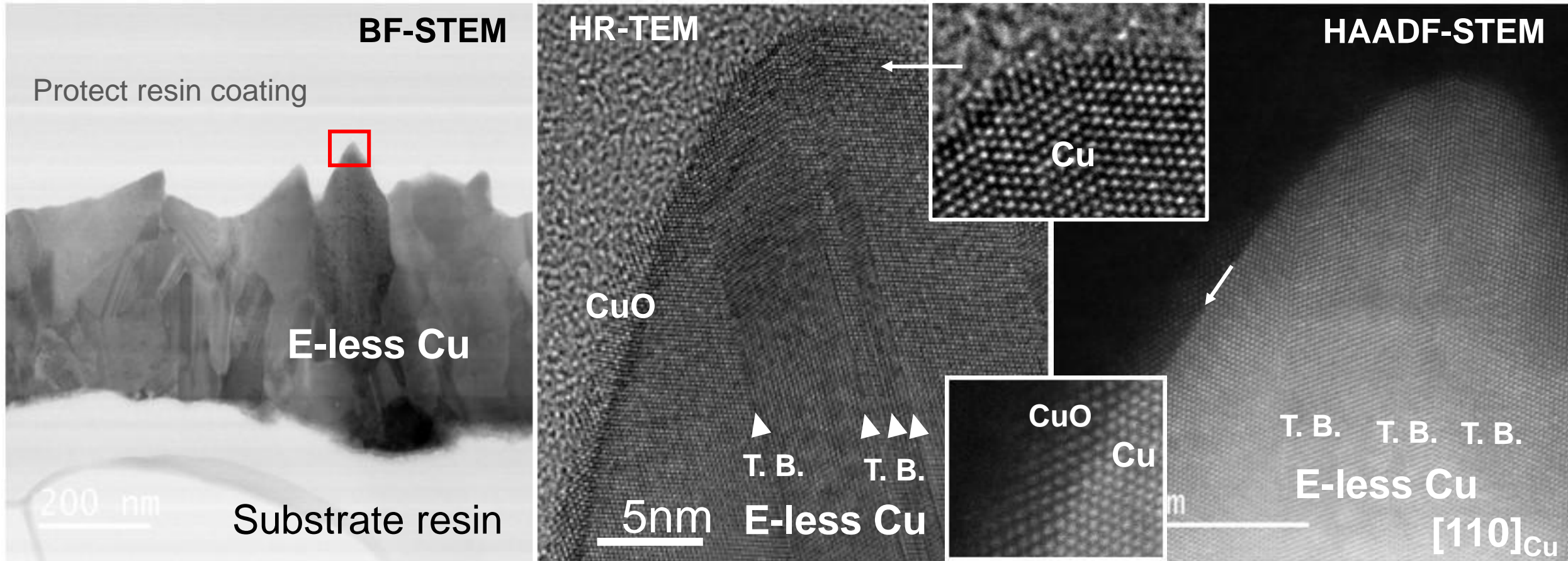


atom maps of Cu, Ni and Pd by Atom Probe Tomography (APT).

Cu (Orange) and Ni (Green) elemental Maps  
 Iso-concentration surface of Pd (yellow ocher)

Elemental distribution of Pd-covered nanovoid

# Microstructure of electroless Cu layer surface



- CuO cannot be completely removed in cleaning processes
  - Residues in desmear process are not completely removed
- } → Nanovoid formation

# Summary

1. FEM simulation of microvias show stress concentration at the bottom of microvia during thermal cycle test. The bottom interface corner shows highest tensile at high temperature.
2. Nanovoids at the lower interface (Pd-covered nanovoids) that are unavoidable with traditional methods also arise and co-exist. However, Pd-covered nanovoids, which can be suppressed effectively in FLET plating.
3. Atom probe tomography and ToF-SIMS show exhibit clear image of residues across electroless Cu plating. Electroless Cu layer contains trace elements, impurities. Conventional electroless Cu plating contains a lot of impurities compared to the FLET.

# Thank you for your attention !



大阪大学  
OSAKA UNIVERSITY



SANKEN  
OSAKA UNIVERSITY



