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THE THIN FILM POWERHOUSE

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21ST INTERNATIONAL CONFERENCE & EXHIBITION ON
DEVICE PACKAGING
New Location!
SHERATON GRAND AT WILD HORSE PASS • PHOENIX, AZ
MARCH 3-6, 2025 • WWW.DEVICEPACKAGING.ORG

Advanced Packaging Innovations for AI and HPC
Enhancing Performance with SiCN for Hybrid Bonding and SiN or SiON for Wafer Flatness Optimization

March 6, 2025

Mohamed ElGhazzali

OUR HOME

Headquarters in Trübbach, CH
Global Headcount
≈ 600

Assembly of
>40
systems simultaneously

>3000m^2
application laboratory down to ISO 4 with 30 measurement techniques

Business Fields
Semiconductor & Advanced Packaging /
Compound & Photonics

PRESENTATION OUTLINE

INTRODUCTION

- Dielectric Layers will play a crucial role in the future of Advanced Packaging as:
  - **Passivation Layer, Barrier Layer, Bonding Interface, Stress Compensation, Gap Fill Interface**

- Plasma Enhanced Chemical Vapor Deposition (PECVD) technology is widely used to deposit dielectric layers like SiO_2

- SiN Deposition by Physical Vapor Deposition (PVD) Opens up a **Wide Range of Advantages** for Future 3D Packaging Applications

  - Low Temp Compatible Process (<200C)
  - Bond Strength
  - Wafer Bow/ Stress Compensation
  - Adhesion to Mold and CTE Matching to bare Si Die
  - High Rate Process (low COO)

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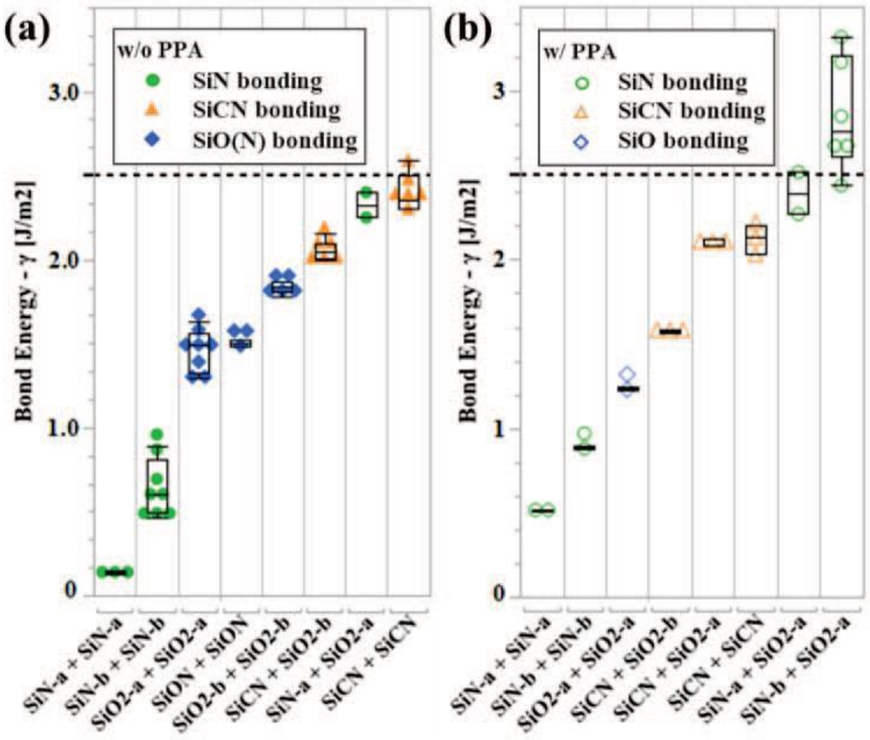
LOW TEMP SIN (<200C) BOND ENERGY

	Composition						Density (g/cm^3)
	Si	C	N	O	Ar	H	
PVD SiCN #1 (Ar/N_2 1:1)	1.00	1.01	1.37	0.01	0.06	0.01	2.81
PVD SiCN #2 (Ar/N_2 2:1)	1.00	1.02	1.10	0.01	0.13	0.01	2.77
PVD SiCN #3 (Ar/N_2 3:1)	1.00	1.03	0.88	0.01	0.16	0.01	2.65
PECVD SiCN	1.00	1.05	0.73	0.00	0.00	1.87	2.00



Yi Yang et. al., "Towards Standardization of Hybrid Bonding Interface: In-depth Study of Dielectrics on Direct Bonding", 2024 IEEE 74th Electronic Components and Technology Conference (ECTC), 2024, pp. 599 – 605

- PVD Films are Higher Density (Lower Hydrophilicity)
- Yang et al 2024 study for bonded pairs, shows "optimal candidate for fusion bonding interface"
  - Non-hydrogenated SiN + hydrogenated SiO2
- PECVD Films are Lower Density and require higher anneal temperatures to perform best

Takeaway #1: PVD SiN Films Deposited at Very Low Temp (<200C) can be used for Bonding Applications

LOW TEMP SIN (<200C) ADHESION PERFORMANCE

Type	Sample		Reliability results [# units with delamination/total units]		
	Mold type	*Pre-Etch*	*168hrs 60°C/60% RH +10x reflow 260°C*	*216hrs 30°C/60% RH + 3x reflow 260°C*	*1000hrs 150°C*
Inorganic	None	No	0/6	0/6	0/6
Organic	Granular	No	6/6	6/6	3/6
	Granular	Yes	0/6	0/6	0/6
	Liquid	No	0/6	2/6	0/6
	Liquid	Yes	0/6	0/6	0/6

Interface Type	Sample		Mechanical Properties	
	Stack	*Interface Material*	*CTE [ppm]*	*E [GPa]*
Inorganic	1.5um SiN / 775um Si	Silicon	2.3	170
Organic	1.5um SiN / 100um Mold / 775um Si	Granular EMC	+	-
		Liquid EMC	++	--

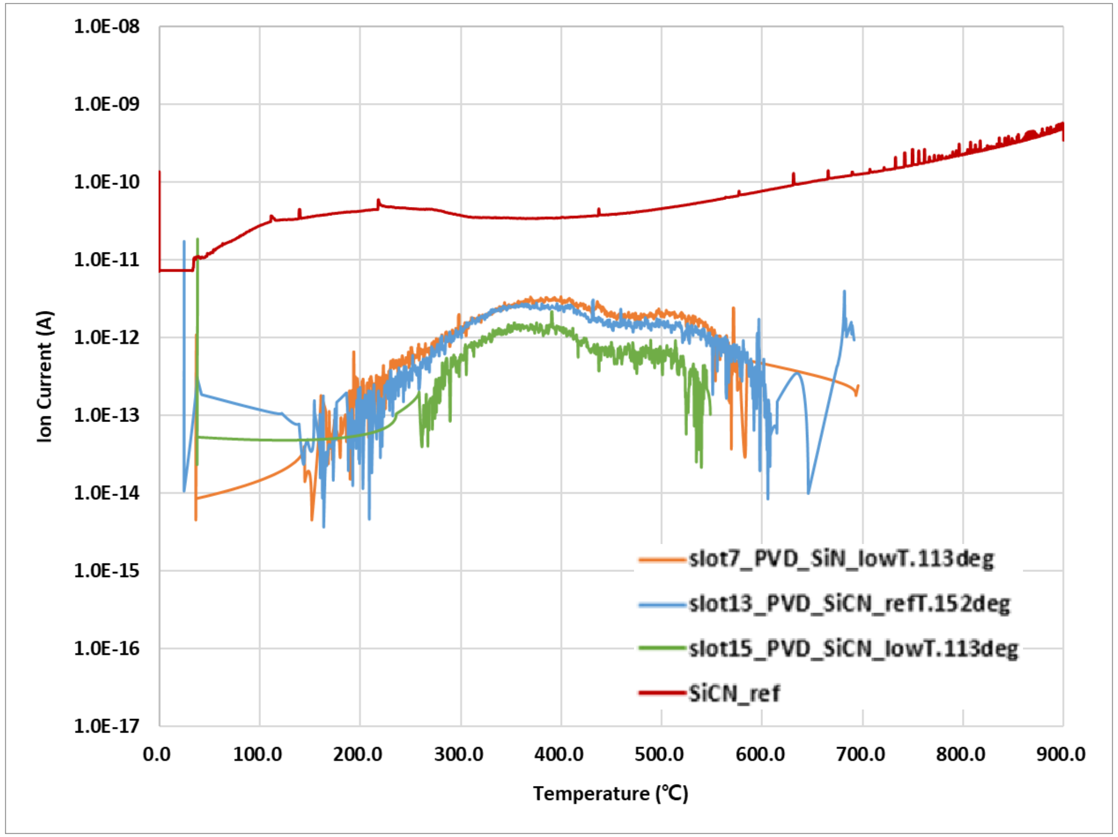
- 2 Type Of Organic Materials are compared with silicon wafer
- Use Of ICP Etch Pre-Clean shows clear benefit for adhesion with organic Materials
- For Si, No Delamination seen for any Wafers (w/ or w/out Etch) due to CTE Matching

Takeaway #2: PVD Sin Process is Compatible with Organic Materials

LOW TEMP SIN (<200C) OUTGASSING PERFORMANCE

Process conditions of each samples PVD Films vs PECVD Ref

- 50nm SiN @ 113 C
- 50nm SiCN @ 152C
- 50nm SiCN @ 113C

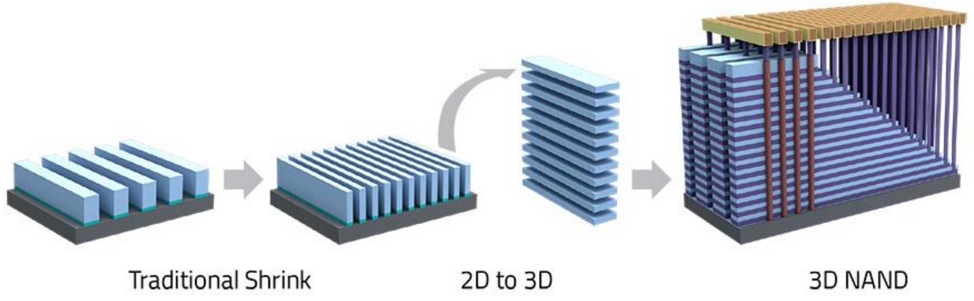


The analysis was performed using fusion Thermal Desorption Spectroscopy (fTDS) under the following heat conditions: RT – 900°C with 20°C temperature increase per minute.

- SiCN PECVD reference layer detected species including H_2, CxHy, and OHx groups
- Not Able to measure exact values of MS (only qualitative measurement)
- However, measured values of <1.0E-11 are similar to the background gas detection level

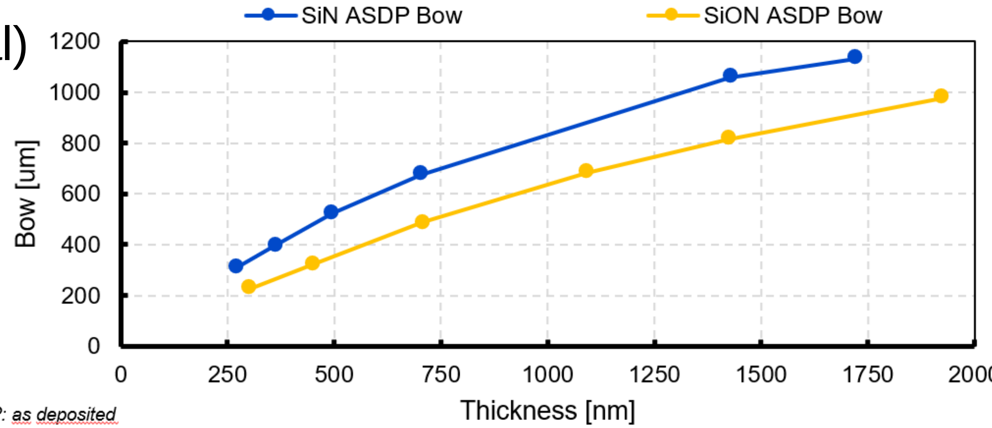
Takeaway #3: No Outgassing confirmed for SiN and SiCN layers using low Temperature PVD

STRESS COMPENSATION



Items	SiON (high WER)	SiN (high Stress)	SiN (Prot. Layer & WPC)
Deposition Rate [nm/s]	3.5	3.5	3.5
Thickness [nm]	100…1950	100…1700	100…3000
WiW THK Uniformity EE5 [%]	< 5	< 5	< 5
WtW THK Uniformity EE5 [%]	< 0.5	< 0.5	< 0.5
Refractive Index	1.9	2.01	2.05
Bow [um]	100…1000	100…1000	100…1000
Compressive Stress [MPa]	Up to 1200	Up to 1800	Up to 1000
Normalized HF Wet Etch Rate	7	1	0.2

- High Efficiency / Bow Compensation per Material Thickness
- Wet Etch Compatible for Wafer Flattening Application (Sacrificial)
- Tunable Stress Available (Thickness Independent)



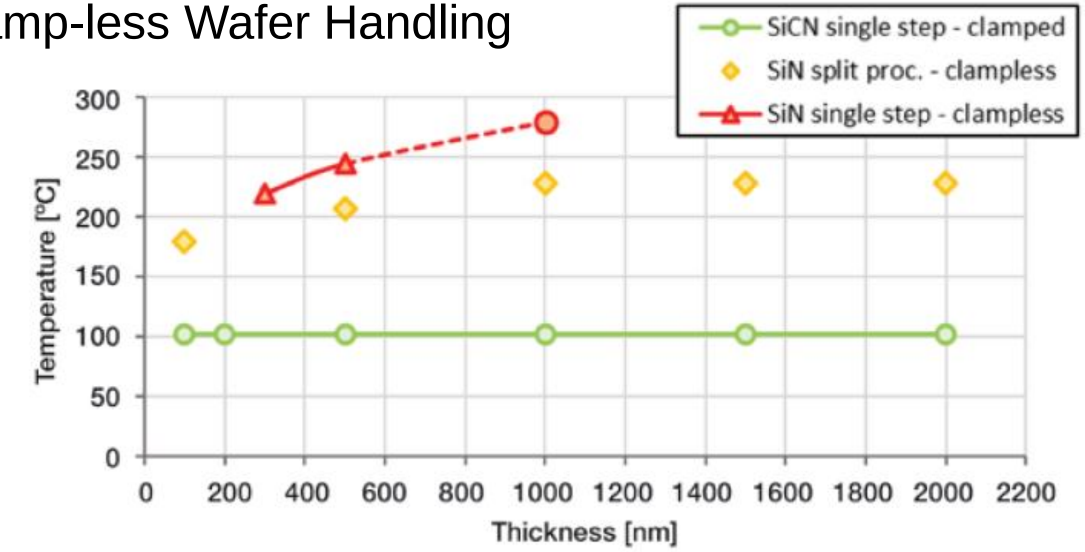
ASDP: as deposited

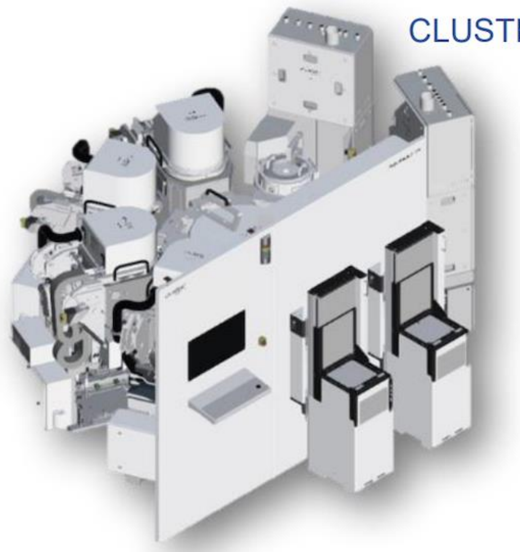
Takeaway #4: PVD SiN Films are Used for 3D NAND Processing (Sacrificial Layer) due to Robust Qualities

PVD EQUIPMENT SETUP (200MM)

200mm Setup used for Initial Testing of Clamp vs. Clamp-less Wafer Handling

Hardware and Process Conditions	Film / PVD System	
	SiN / Platform A	*SiCN / Platform B*
Target	Si polycrystalline (disc Φ=400mm)	SiC powder pressed (1:1 ratio, disc Φ=300mm)
Power source	Pulsed DC (frequency=350kHz; pulse-off time=1100ns)	Continuous DC
Power density [W/cm^2]	6.37	4.95
Gas ratio N2/Ar [-]	1.0	1.2
Sputtering pressure [mbar]	1.3e^{-2} (pump throttled)	9.7e^{-4}
Pedestal type	Clampless, recessed chuck top, PCW cooled pedestal	Clamped, flat chuck top with back-gas inlet, PCW cooled pedestal
Pre-treatment process	Radiation degas (load-lock) and ICP-Etch	ICP-Etch

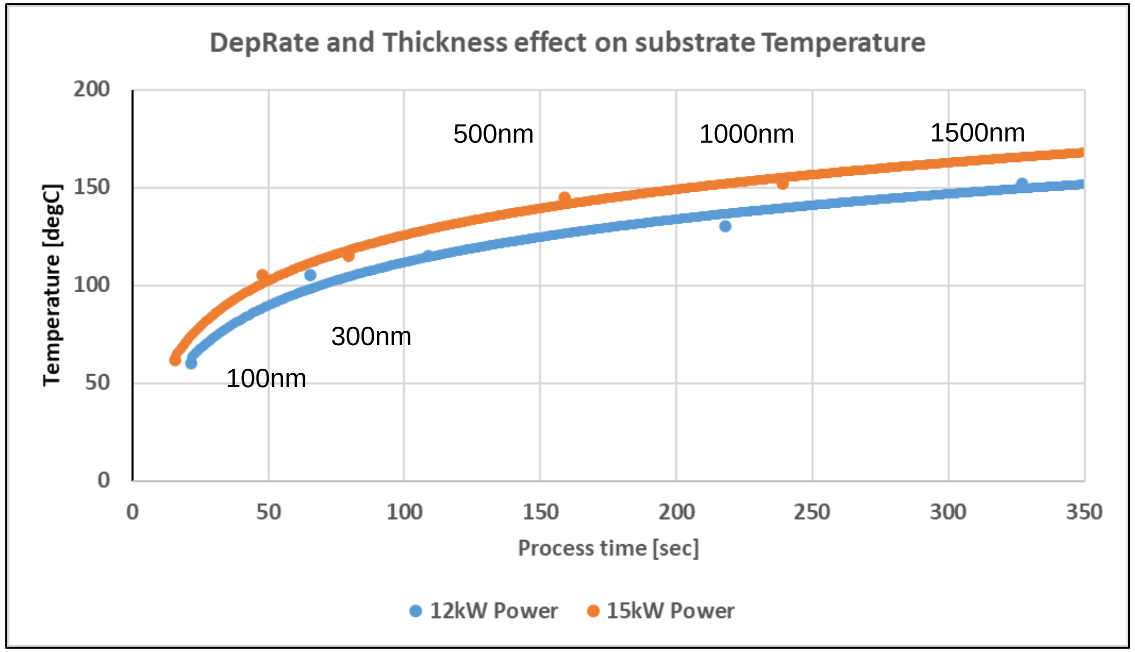


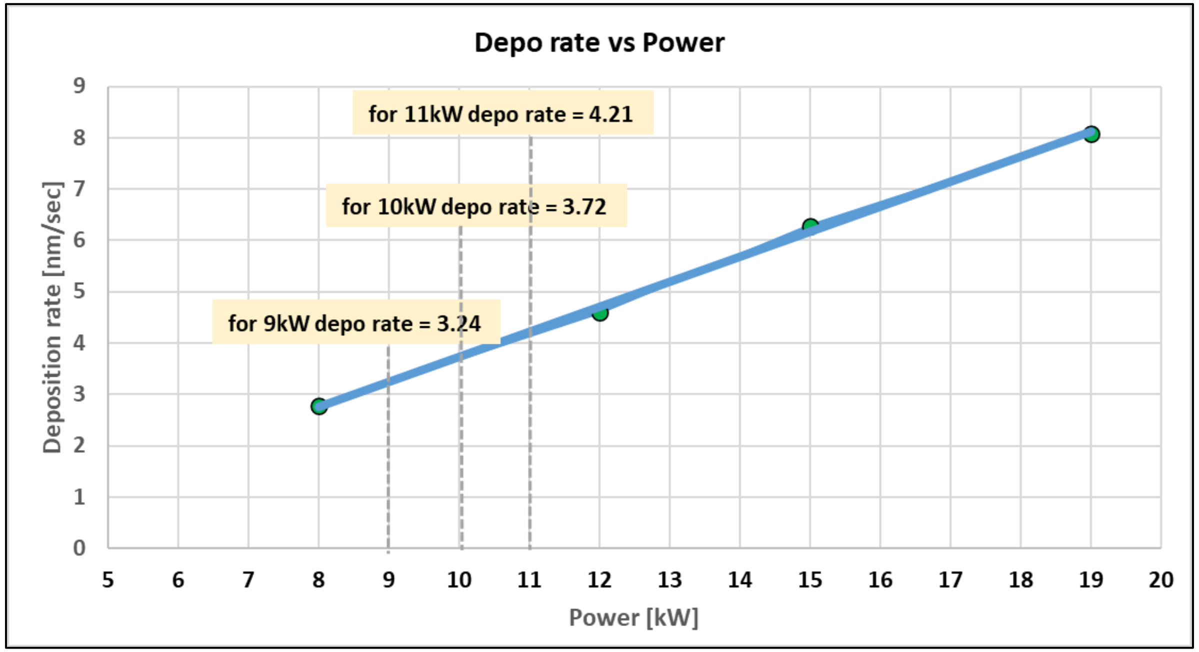


CLUSTERLINE® 200E

PVD EQUIPMENT SETUP (300MM)

300mm Production Setup Used to Validate Low Temp at High deposition Rate SiN





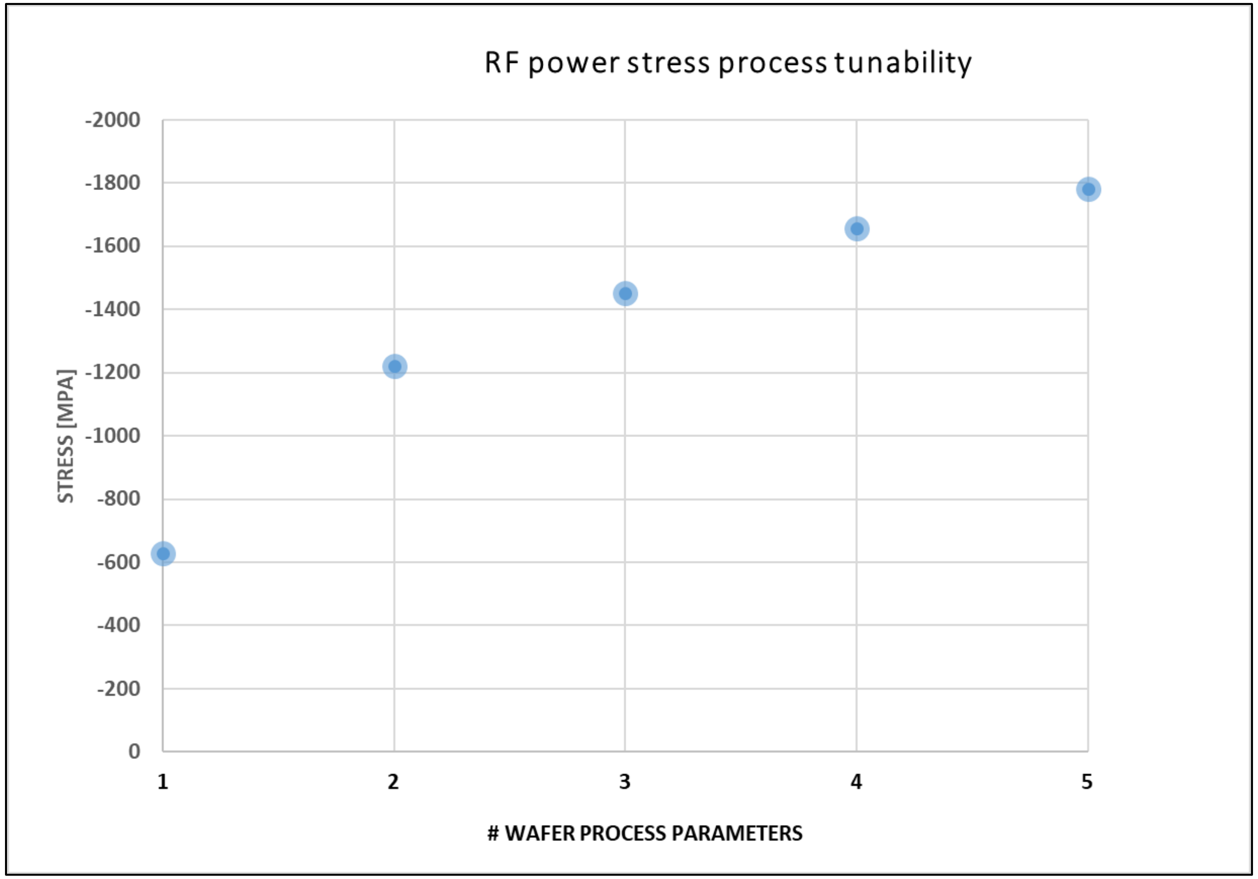
Takeaway #5: HighRate Deposition at Low Temp (<200C) Has Been Demonstrated for Thicker Applications (2-5um)

SIN STRESS TUNABILITY

- compressive stress range from -600 MPa to -1800 MPa, confirming the tunability of the dielectric layer.

PVD Benefits for Stress Compensation

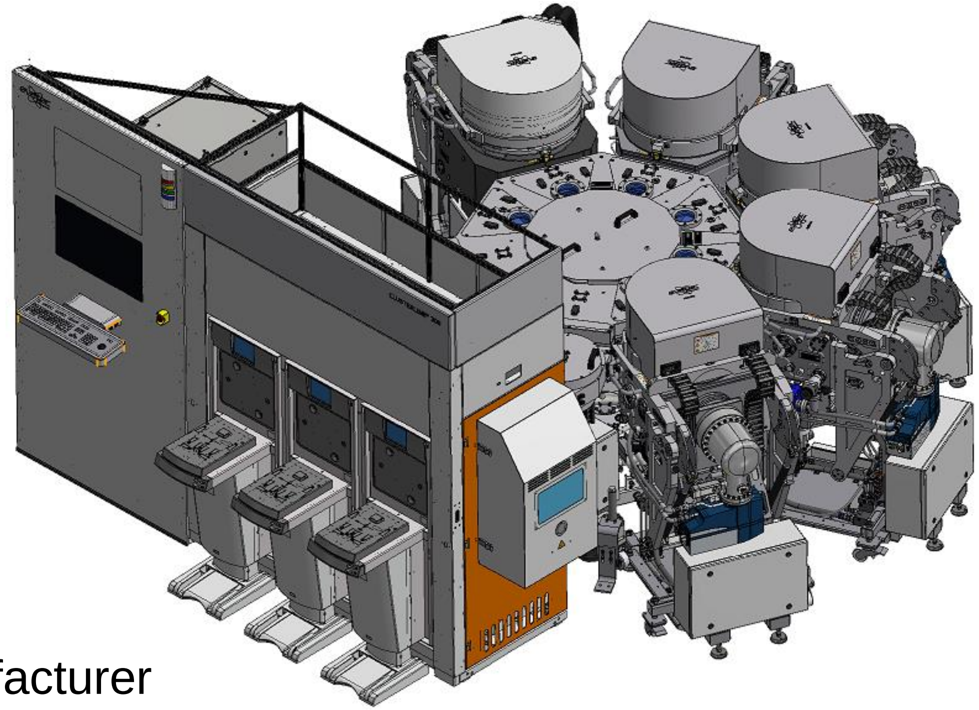
- High Efficiency (less film thickness required vs. PECVD for same bow compensation)
- Tunability of stress levels through adjustable process parameters



Takeaway #6:Tunability of stress levels through adjustable process parameters

CLN300 EQUIPMENT OVERVIEW

- High stress (>1.2GPa) PVD dielectric deposition process has been demonstrated both for SiN and SiON
- Stress tunability (400 to 1800 MPa compressive) at constant layer thickness
- Warpage correction and control up to 1000um
- Good Thickness Uniformity
- High Deposition Rate
- Temperature Control
- Stable particle performance over target lifetime
- Wafer Frontside protected from deposition
- Shutter feature for pasting and conditioning
- 2 – 3x Higher Warpage Correction Efficiency vs. PECVD
- Qualified for compressive stress at major 3D-NAND Manufacturer



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SUMMARY

- PVD SiN Films Deposited at Very **Low Temp** (<200C) can be used for Bonding Applications
- PVD SiN Process is **Compatible** with **Organic Materials**
- **No Outgassing** with **PVD SiN** Films compared to PECVD SiN
- **High Rate Deposition** at Low Temp
- PVD SiN Films are used for 3D NAND Processing (Sacrificial Layer) due to Robust Qualities
- PVD SiN for wafer **Stress compensation and Warpage Correction**
- **Tunability of stress** levels through adjustable process parameters
- **Evatec's** Clusterline Platform Offers **Flexibility for Various Processes**

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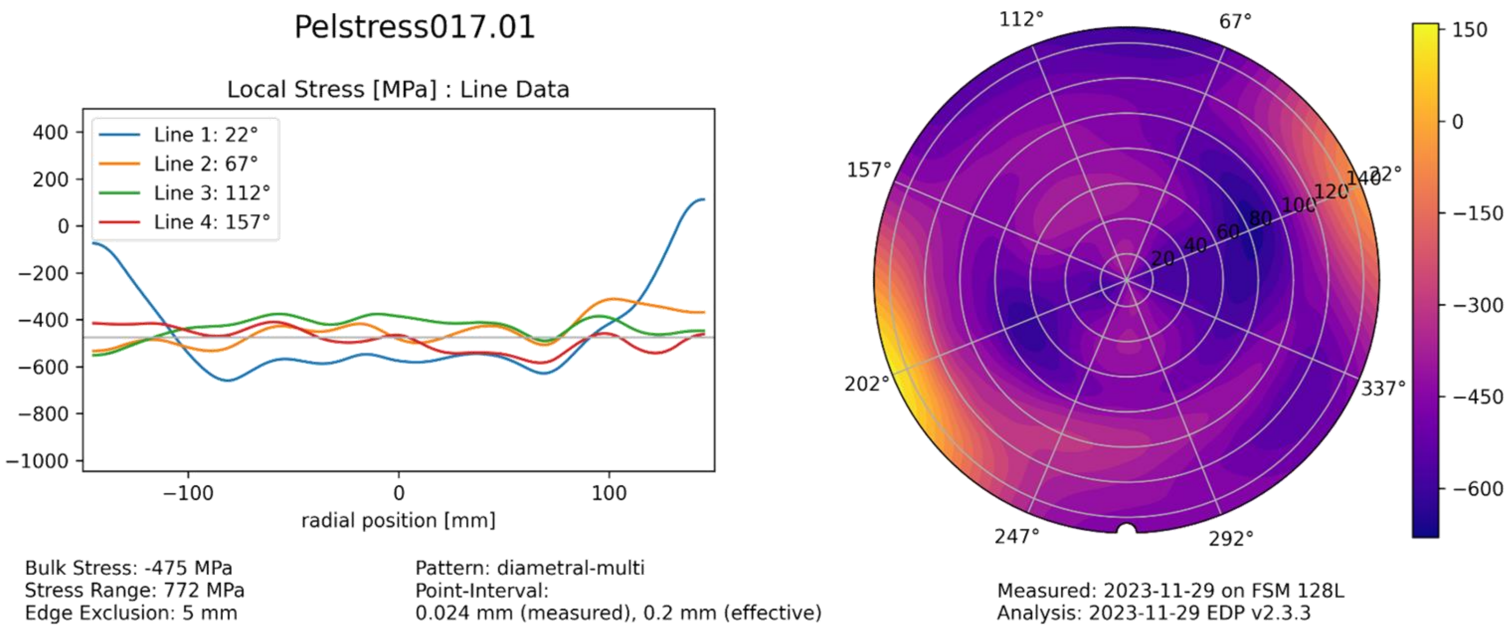
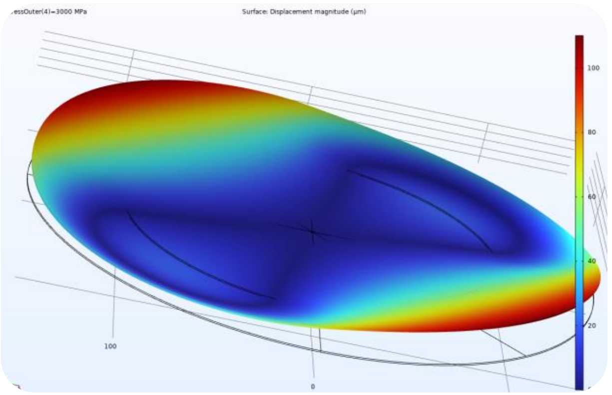
OUTLOOK: SADDLE WARPAGE CORRECTION

- Stress Range of Wafer after deposition between +150 MPa (tensile) and -600 MPa (Compressive)
- First Feasibility Results Show Stress Can Be Modulated in Certain Sectors by PVD Technique

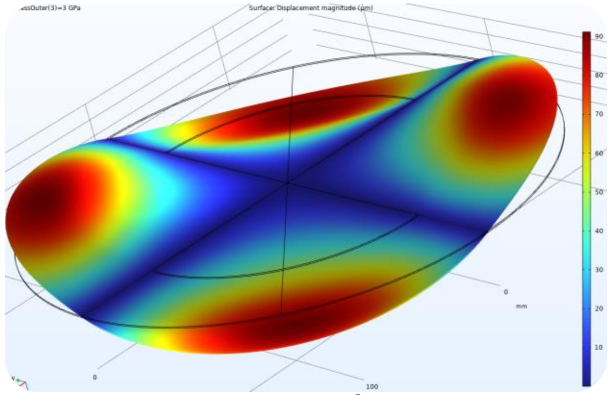


Potato Chip – One directional stress



tensile

Saddle Warp – Compressive & Tensile



compressive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FUTURE TOGETHER