Quantic Ohmega Ticer

GREENSOURCE FABRICATION

"Integrating Thin Film Resistors into Organic Substrates for Module and Integrated Circuit (IC)Packaging"

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Andreas Schilloff (Greensource Fabrication)

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21ST INTERNATIONAL CONFERENCE & EXHIBITION ON
DEVICE PACKAGING
SHERATON GRAND AT WILD HORSE PASS PHOENIX, AZ
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SPEAKERS

John Andresakis

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John Andresakis has over 40 years of experience manufacturing printed circuit boards and related products. He joined Quantic Ohmega-Ticer in January 2023 and is now the Director of Business Development. He is working on expanding the market for the company's novel thin film resistor technology.

Andreas Schilloff

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Andreas Schilloff joined Green Source Fabrication in 2018, bringing along many years of PCB fabrication experience from I3 Electronics and Sanmina Corporation. In addition, Andreas has an ME/EE degree from RIT. From 2018 through the present time as Principal Product Engineer, he has contributed to expanding GSF capabilities in producing third-party products, from the aspects of NPI/ Process/ Product engineering.

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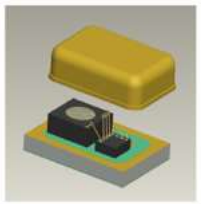
Agenda

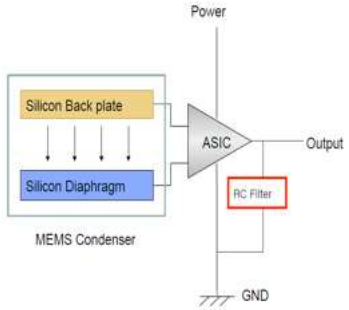
- Introductions and Benefits
- Resistor/Conductor Foil Formation
- Manufacturing Process- mSAP Overview
- Test Vehicle Design
- Experimental Results
- Optimization Strategies
- Future Directions and Opportunities
- Conclusion

Introduction and Benefits

- Integration of thin film resistors into organic substrates
- Key Benefits:
  - Significant miniaturization
  - Reduced need for discrete resistors
  - Space conservation on substrate surface
  - Compatible with existing production methods
  - Improved signal integrity

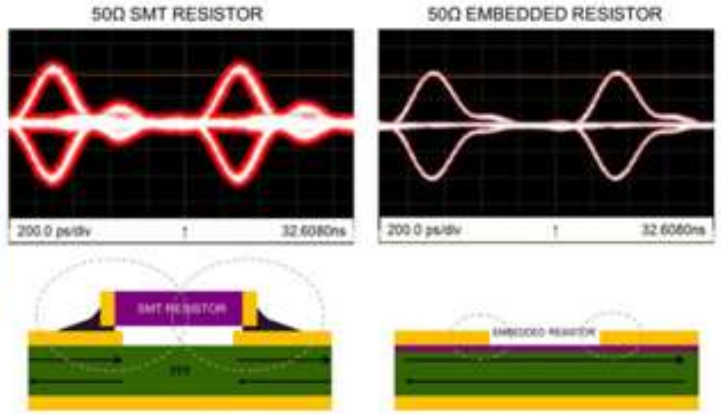
Surface Mount Embedded





EMC@217Hz &1KHz improved 20dBV from 500 to 2800MHz

Embedded Thin Film Resistors SI Improvement

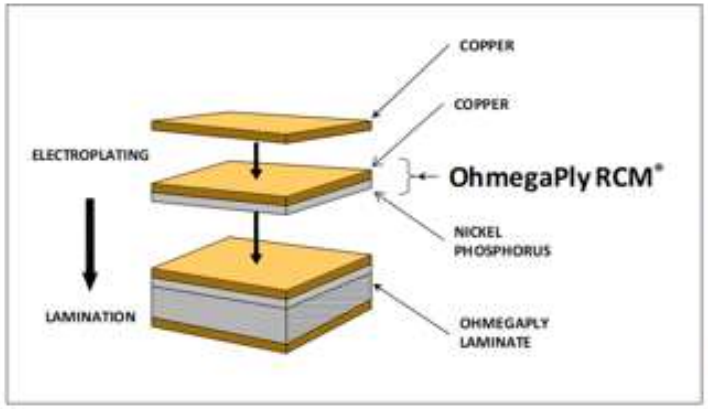


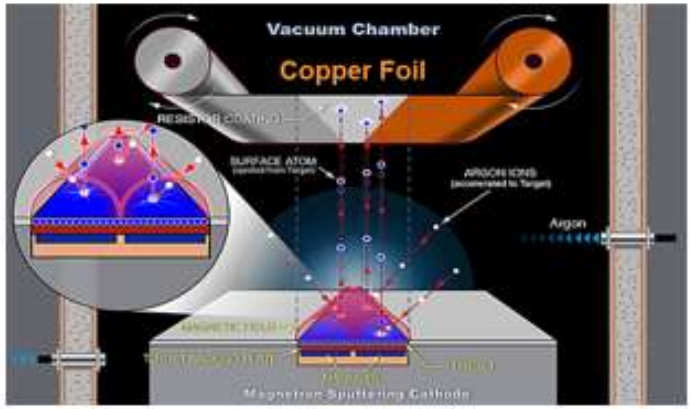
Eye diagrams show 30% reduced noise at 1 Gb/s using thin film resistor

Courtesy of Applied Laser Technology

Resistor/Conductor Foil Formation

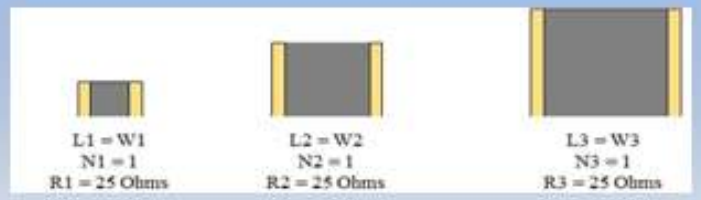
- Resistive Layer Deposition:
  - Electroplating Deposition
  - Sputtering Deposition
- Material Selection:
  - NiCr selected for optimal properties
  - Low temperature coefficient of resistance
- Carrier Foil Method Benefits:
  - Stable, flat surface
  - Precise control
  - Easy handling
  - Sub-micron thickness capability

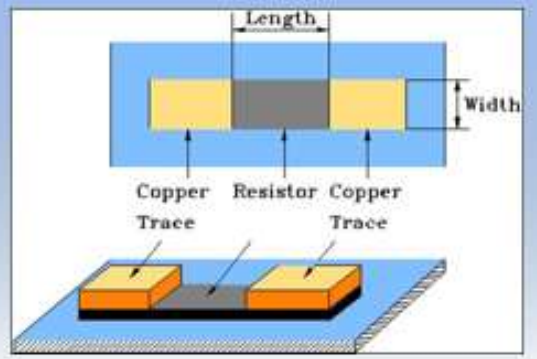




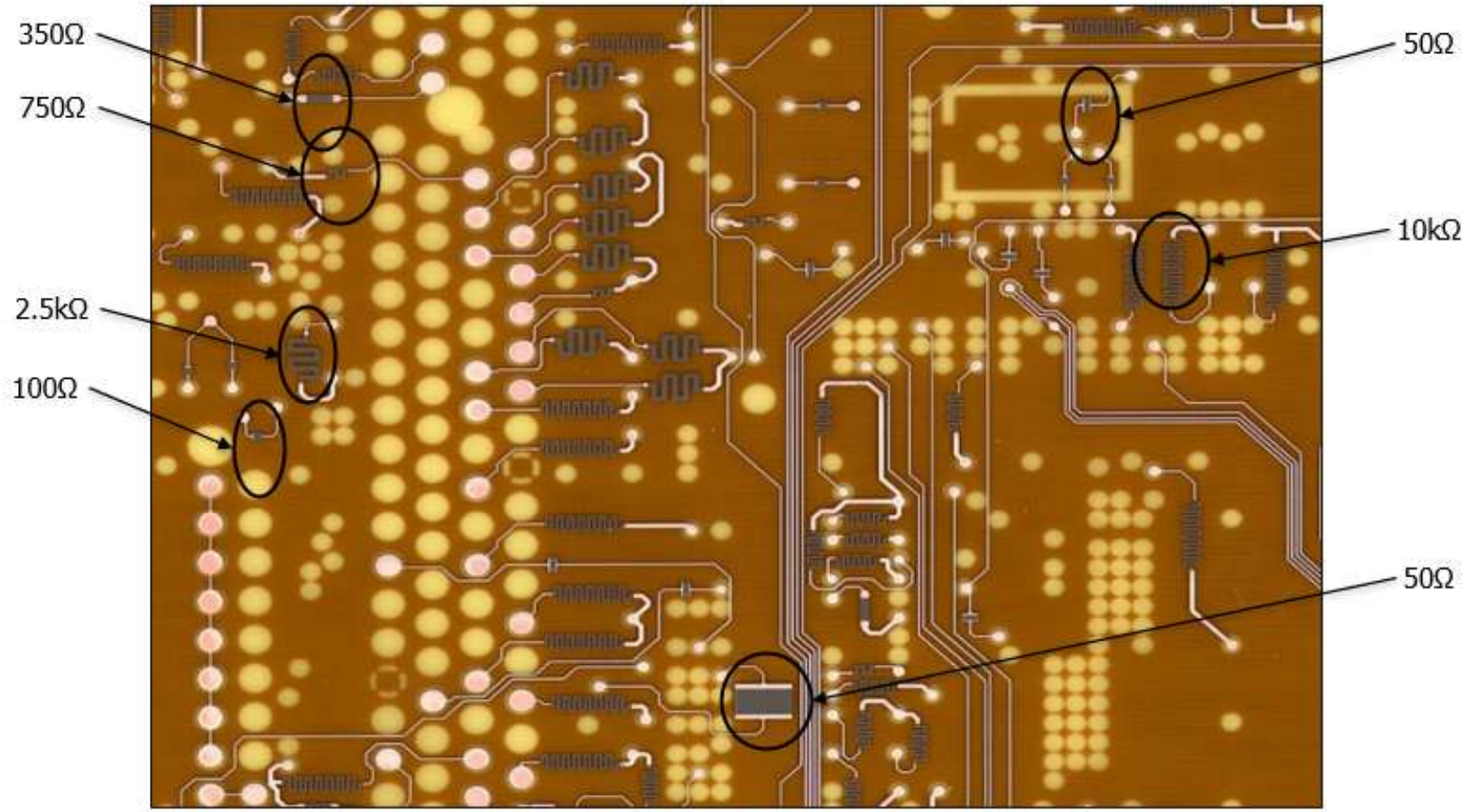
Resistivity = Ohms/square

$$R = R_s \left(\frac{L}{W}\right)$$



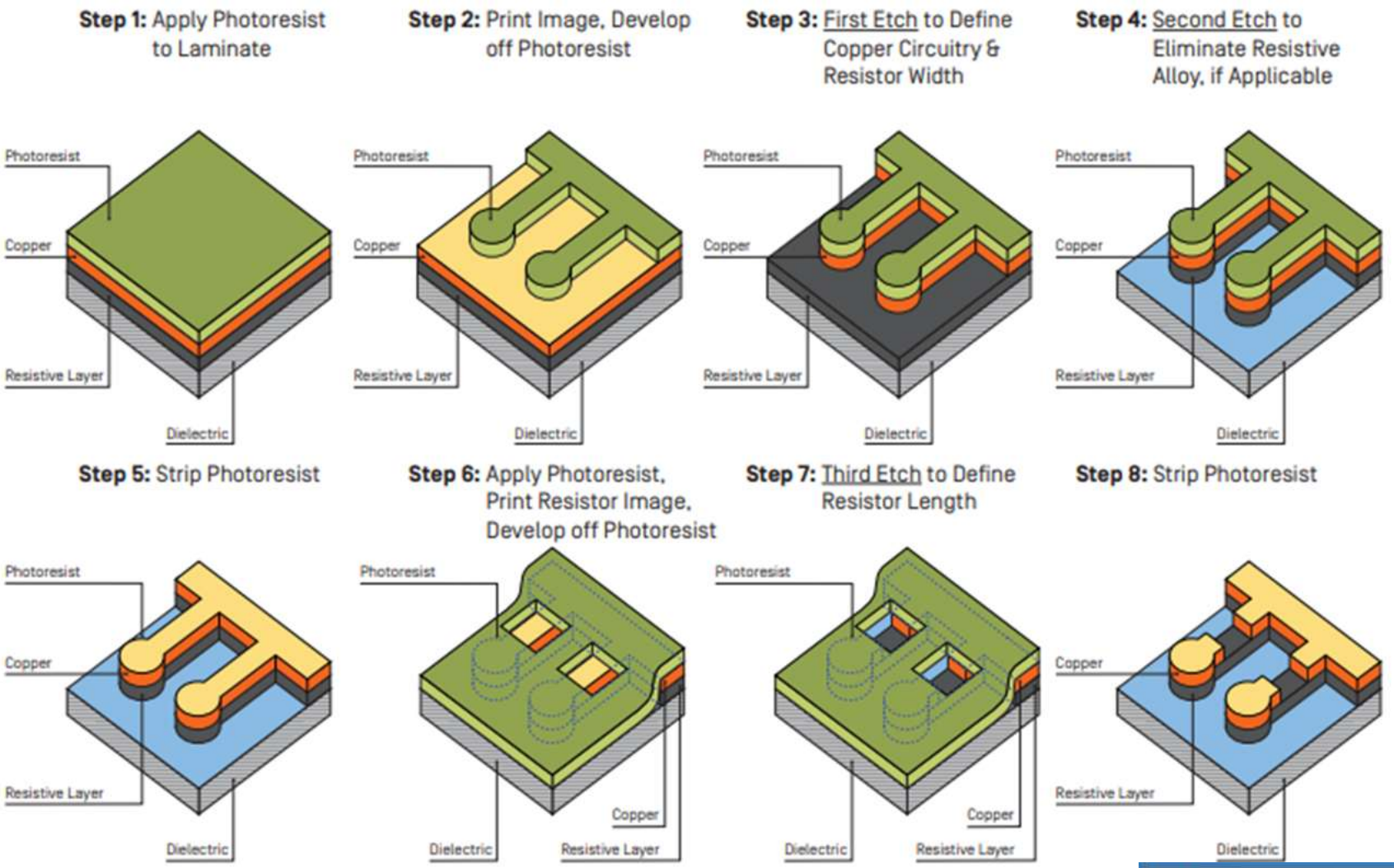


Designing with Ohms per Square (100 OPS Example)



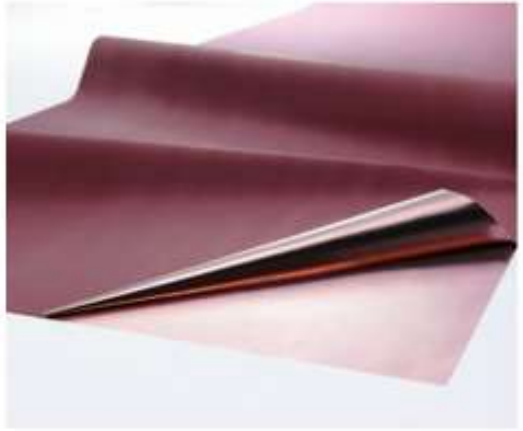
One sheet resistivity can make orders of magnitude resistors

Manufacturing Process- Standard Subtractive Method

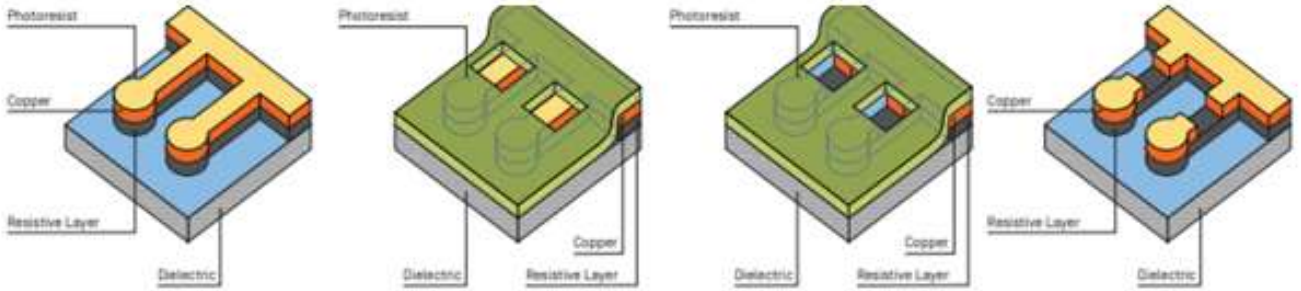


Manufacturing Process- mSAP Overview

- Seed Layer Preparation Methods:
  - Direct Metallization
  - Etching Down of 9-18 micron Foil
  - Sacrificial Carrier Foil Method (preferred)
- Process Steps:
  - Seed layer creation
  - Photoresist application and patterning
  - Trace plating (12-15 microns)
  - Photoresist stripping
  - Quick etch for seed layer and resistor material removal.
  - 2nd Imaging/etching steps to define resistors
    - *Note: Needed when using embedded resistors*



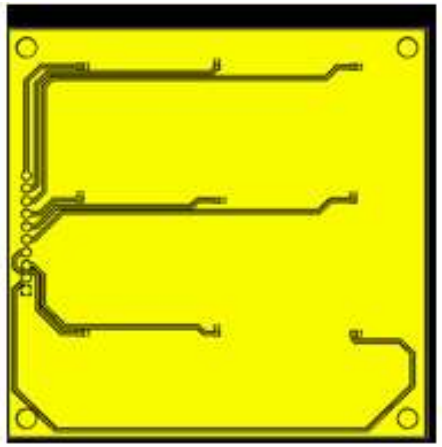
Carrier Foil
- 18 um carrier
- 3 um seed layer

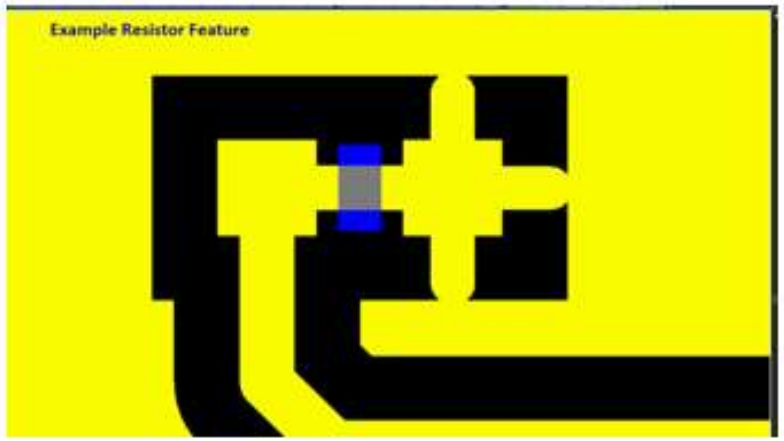


2nd Imaging/Etching steps

Test Vehicle Design

- 6-layer (2+2+2) substrate design
- Materials Used:
  - Core: Panasonic R-1515V (low CTE)
  - Build-up prepreg: AGC fastRise™ HF
  - Copper layers: 18µm, 9µm, and 3µm (after carrier removal) thicknesses
  - Resistor material on layer 2 (100 OPS NiCr)





Layer	Stack up	Base Thickness	LT	Processed Thickness	Isolation Distance (Summed)	Impedance ID	Copper Layer Type	Copper Coverage	Description
1		8.50		15.00			Signal	0.00	3um-007_3_ED_AC-007-ALUM-3um-JTCS-P1_20_X_26_NONE
		51.00	3.23	48.75	48.75				RF-HF-051_BP_51um_18.5_X_24.5
2		3.00		15.00			Mixed	85.00	3um-18um_3_ED_TC100-NiCr_18.5_X_24.5
		51.00	3.23	48.50	48.50				RF-HF-051_BP_51um_18.5_X_24.5
3		17.27		25.00			Plane	90.00	
4		400.00	4.40	400.00	400.00				R1515V_0160_H_VLP_H_VLP_4-2116_18G_X_24
		17.27		25.00			Plane	90.00	
5		51.00	3.23	48.50	48.50				RF-HF-051_BP_51um_18.5_X_24.5
		3.00		15.00			Mixed	85.00	3um-18um_X_ED_MT18EX_20X26
6		51.00	3.23	48.75	48.75				RF-HF-051_BP_51um_18.5_X_24.5
		8.50		15.00			Signal	0.00	3um-007_3_ED_AC-007-ALUM-3um-JTCS-P1_20_X_26_NONE

Copper Thickness = 110.000 | Dielectric Thickness = 594.504 | Solder Mask Thickness = 0.000 |
Stack Up Thickness = 704.504 | Stack Up Thickness with Soldermask = 704.504

704.5

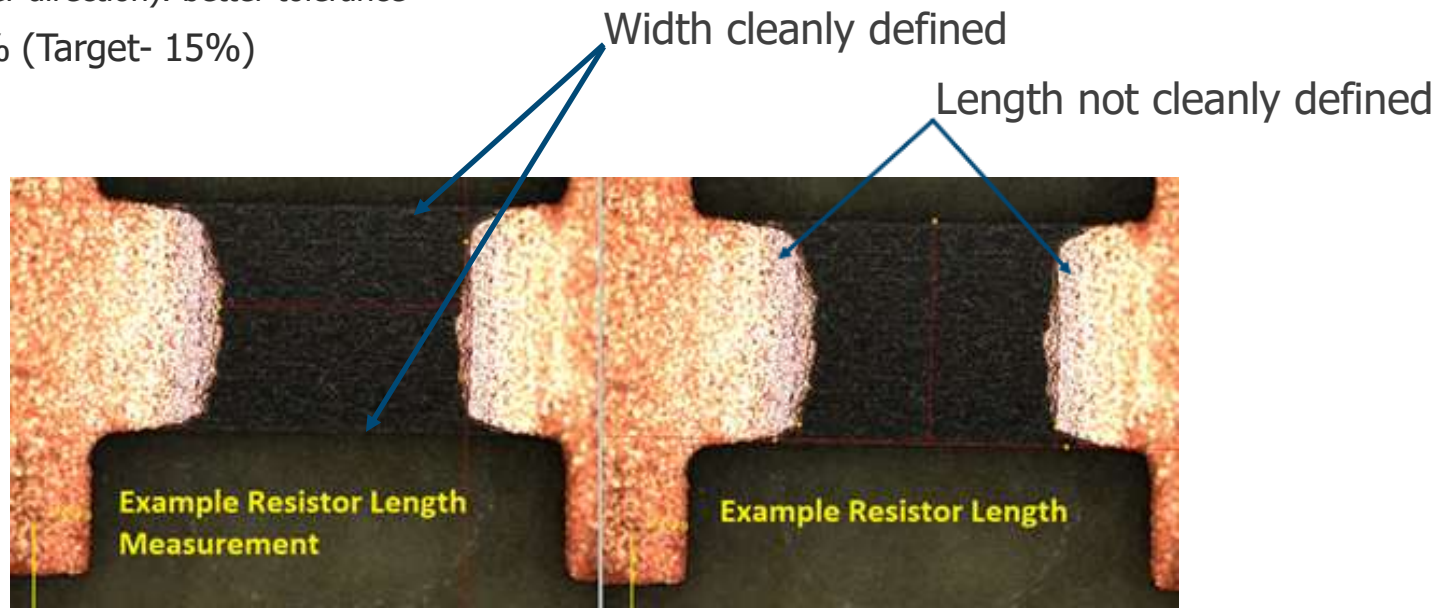
Notes
buried/ blinds are mainly for D-coupon/ reliability testing (both stacked and staggered)
layers 2/5 are MSAP for resistor process
outers are HF plated to finish at around 15um to demonstrate .150mm pitch BGA pattern

Experimental Results

Target: 100 ohms resistors (0.01”(0.254mm) x 0.01”(0.254mm)) using 100 Ohms/square material

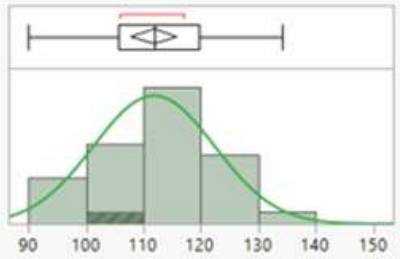
Key Findings:

- Successful embedding of resistors
- Good material adhesion to build-up film
- Orientation affects resistance values and tolerance
  - Perpendicular resistors (to etcher direction): better tolerance
- Overall tolerance: +/- 20-25% (Target- 15%)



Experimental Results

PERP



Compare Distributions

Show	Distribution	AICc	BIC	-2*LogLikelihood
☑	Normal	229.87753	232.23548	225.43309

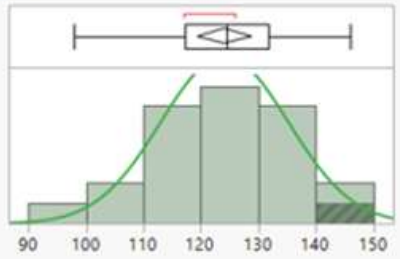
Quantiles

100.0%	maximum	134
99.5%		134
97.5%		134
90.0%		124.8
75.0%	quartile	119.75
50.0%	median	112
25.0%	quartile	105.75
10.0%		95.3
2.5%		90
0.5%		90
0.0%	minimum	90

Summary Statistics

Mean	111.83333
Std Dev	10.537563
Std Err Mean	1.9238869
Upper 95% Mean	115.76812
Lower 95% Mean	107.89854
N	30
N Missing	24

PARA



Compare Distributions

Show	Distribution	AICc	BIC	-2*LogLikelihood
☑	Normal	187.21387	188.99655	182.64244

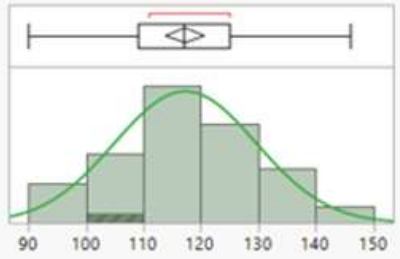
Quantiles

100.0%	maximum	146
99.5%		146
97.5%		146
90.0%		139
75.0%	quartile	131.75
50.0%	median	124.5
25.0%	quartile	117.25
10.0%		108.5
2.5%		98
0.5%		98
0.0%	minimum	98

Summary Statistics

Mean	124.08333
Std Dev	11.100007
Std Err Mean	2.2657793
Upper 95% Mean	128.77046
Lower 95% Mean	119.39621
N	24
N Missing	30

OVERALL



Compare Distributions

Show	Distribution	AICc	BIC	-2*LogLikelihood
☑	Normal	427.76238	431.50506	423.52709

Quantiles

100.0%	maximum	146
99.5%		146
97.5%		144.5
90.0%		134
75.0%	quartile	125
50.0%	median	117
25.0%	quartile	109
10.0%		99
2.5%		90.375
0.5%		90
0.0%	minimum	90

Summary Statistics

Mean	117.27778
Std Dev	12.327935
Std Err Mean	1.6776195
Upper 95% Mean	120.64266
Lower 95% Mean	113.9129
N	54
N Missing	0

Note: For the size resistors used in this study, if made using the standard subtractive process, the tolerance can be > +/- 30%

Optimization Strategies

Design/Process Improvements:

- Orient resistors perpendicular to the etcher direction
- Alternative: 45° angle processing in etcher
- Enhance plating distribution
- Modified copper plating process (do not plate up over resistor areas)
- Utilize standard first article procedure

Material Improvement

- Optimize resistivity uniformity of resistor/conductor foil
- Utilize lower Ohms/square value (thicker coating is more uniform)

Future Directions and Opportunities

Upcoming Research:

- Tolerance Improvement
- Material characterization (CTE, peel strength, etc.)
- Long-term reliability testing
- High-frequency electrical testing (40+ GHz)

Industry Collaboration:

- Open to partnerships
- Focus on practical implementations
- Scaling opportunities

Conclusions

- We have demonstrated that thin film resistors can be embedded in organic packaging substrates using resistive layers on 3-µm copper (with a carrier) using the mSAP process.
- We did not meet the targeted tolerance but have a path to improve.
- Modules and IC Packages can utilize the potential benefits of embedded resistors.
  - Miniaturization and/or increased functionality
  - Improved electrical performance
  - Improved reliability
- Seeking opportunities for collaboration

MORE INFORMATION

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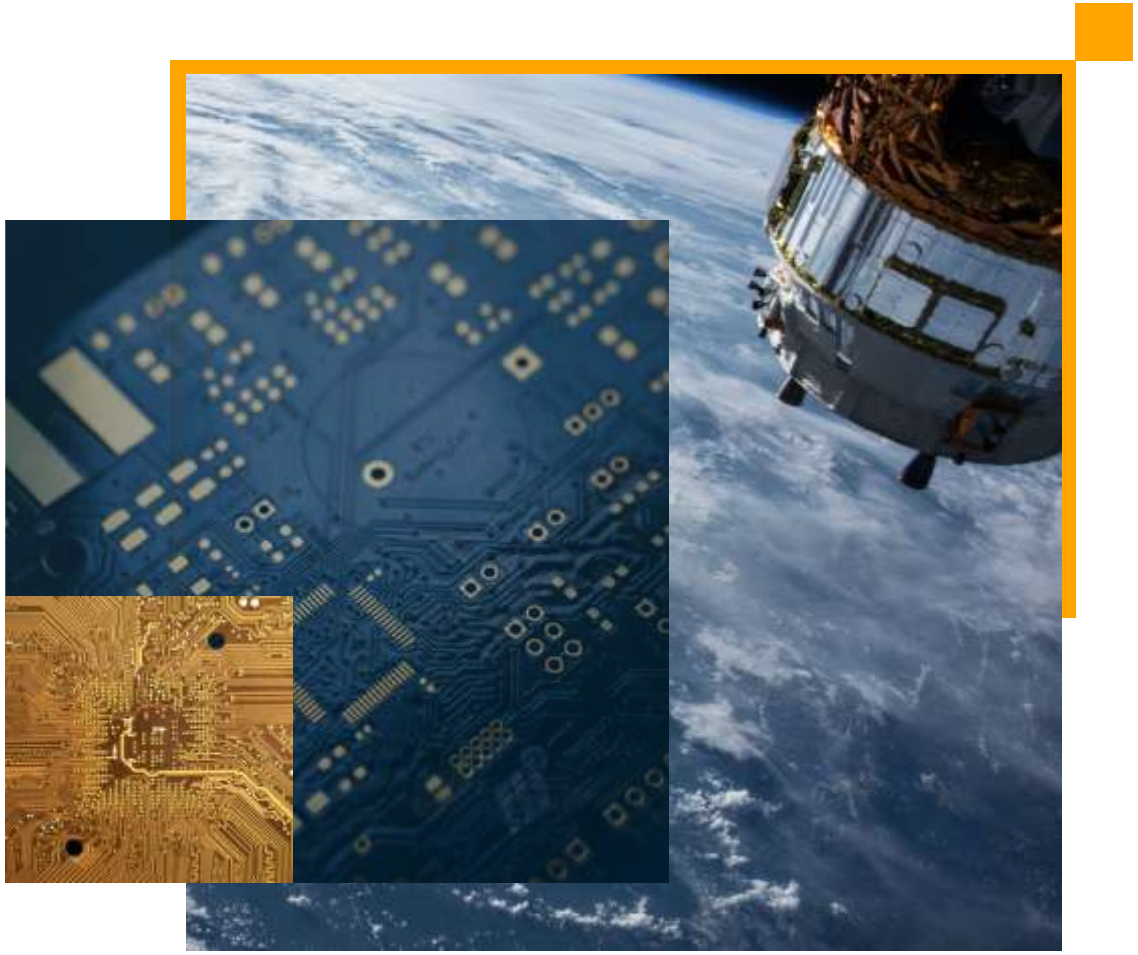
Questions?



Thank You!

John Andresakis

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