S-Parameter Rational Function (SRF) Based Effective Power Delivery Analysis for 3D Foveros Packages

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Speaker's Bio

- **Mohammad S Islam** completed his Ph.D. degree from the Department of Electrical, Computer, and Systems Engineering (ECSE) at Case Western Reserve University (CWRU) in Cleveland, Ohio in 2020.
- Currently, serving as a Senior Analog Engineer in ATTD Architecture, Design & Technology Solutions (ADTS) at Intel Corporation.
- Published over 25 papers in peer-reviewed journals and conferences, one book chapter, and has been submitted multiple IDFs.
- Received the best paper award in SNUG 2024 and best paper finalist in IFCS-ISAF 2020.
- Expertise lies in power distribution Network (PDN) modeling and analysis for Package and Motherboard (MB), co-design constraints, and trade-offs for optimized and cost-effective solutions for advanced semiconductor packages.

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Outline of the Presentation

☐ Background

☐ Problem Statement

☐ Proposed Solutions

-Analysis flow with SRF Model

☐ Case Study: AC & Transient Correlation

- Frequency domain (FD)

-Time domain (TD)

☐ Ongoing Activity & Conclusion

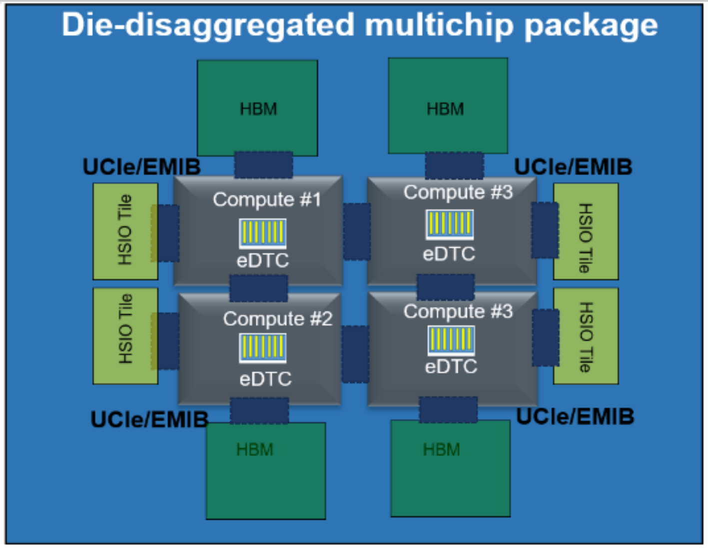
Acronym List:

- SRF- S-parameter Rational Function
- AC- Alternative Current
- DC- Direct Current
- FD- Frequency Domain
- TD- Time Domain
- PDN- Power Delivery Network
- MB- Motherboard
- PKG- Package
- VRM- Voltage Regulator Module
- MCP- Multi-Chip Package
- TSC- Top-Side Capacitor
- BSC- Back-Side Capacitor
- PI- Power Integrity
- PD- Power Delivery
- HPP- HSPICE Precision Parallel

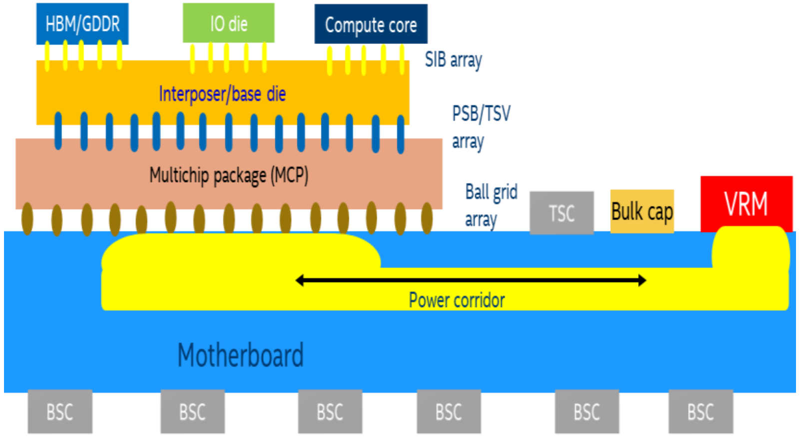
Background

- ❑ Power delivery simulation of 3D Foveros/ Heterogeneously integrated Package is very time-intensive, with original S-parameter models of packages, motherboards, & dies, in dealing with numerous ports (> 200) in a S-parameter model
  - ✓ This simulation complexity grows with iterative changes of die, package and MB databases in multiple iterations of optimization cycles

- ❑ Macro model is chosen over original S parameter model with IFFT for Tran. analysis, because IFFT necessitates evenly spaced frequency sampling, easily leads to non-convergency in transient/Time domain sims
  - ✓ Streamlining the process is needed to improve the efficiency, consistency and accuracy, in handling S-parameter model, during iterations



Heterogeneously Integrated & die-disaggregated 3D Foveros (MCPs)

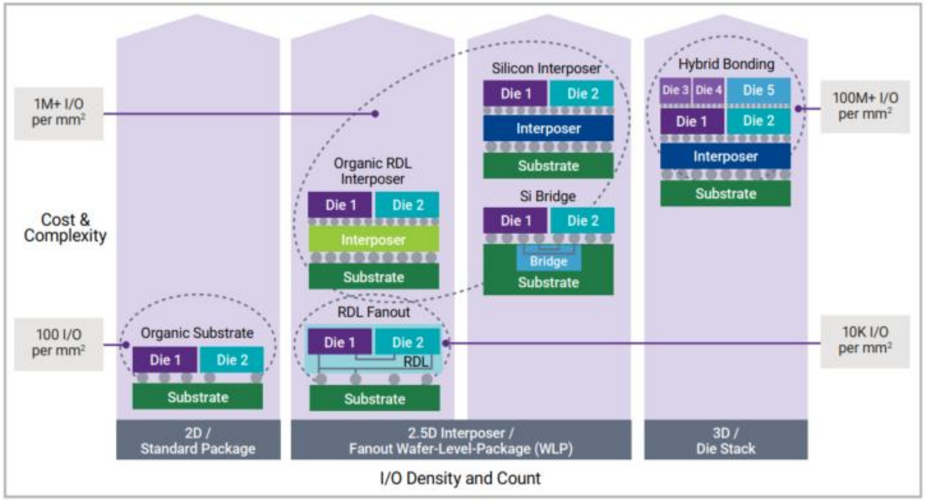


Power delivery network (PDN)
- lateral and/or vertical paths
in a multi-chip package (MCP)

Die-disaggregated multichip package (MCP) (Not New!) /Multi-die ecosystem

❑ Process of converting large monolithic SoC into smaller dies (e.g., chiplets)- Reassembled in PKG (can be Heterogeneous Integration)

- Advantages
  - Better yield, performance, economical to fabricate smaller dies and design flexibility
- Challenges
  - Low latency C2C communication and low PDN impedance
  - Assess system-level tradeoffs in performance HSIO IPs
  - Pitch→ cost scaling



I/O density in multi-die ecosystem in package

Source: Synopsis.com

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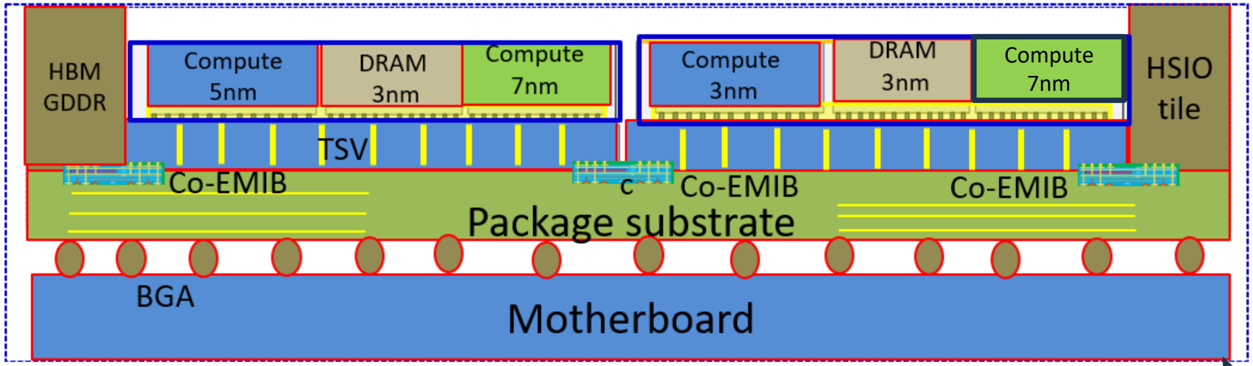
Die-Disaggregation packaging challenges



Focus of this presentation

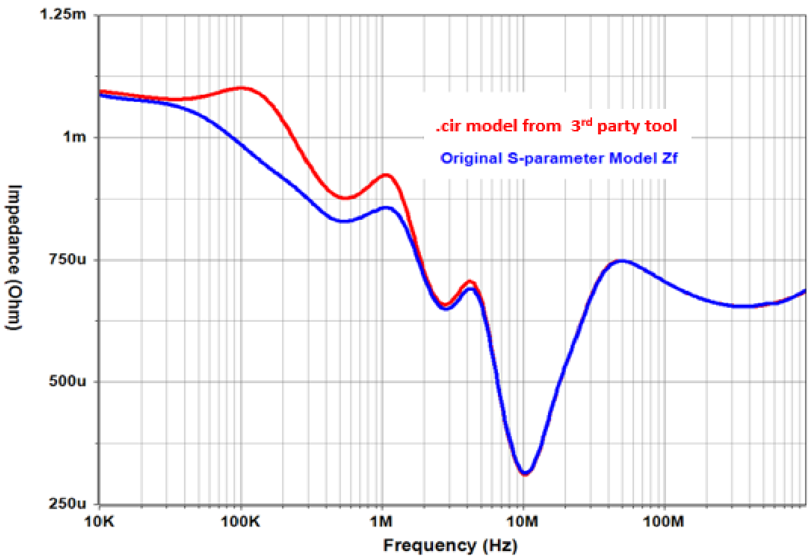
Overall Challenges

- Disaggregation overhead: Added area, power & latency
- 3D die stacking: Thermal hotspot mitigation/IP reuse
- 3D die stacking: Power delivery modelling flow/Signal Integrity/eye diagram
- Characterization (Electrical)
- Quality and Reliability
- SW deployment
- Complex design enablement
- Cost and Time-to-Market

- Plethora of opportunities
- Need reasonably initial assessments of overall product ROI
- Reduce tax on latency (IO near to CPU), power, increase B/W with optimizing signal routing

Problem Statement (1)

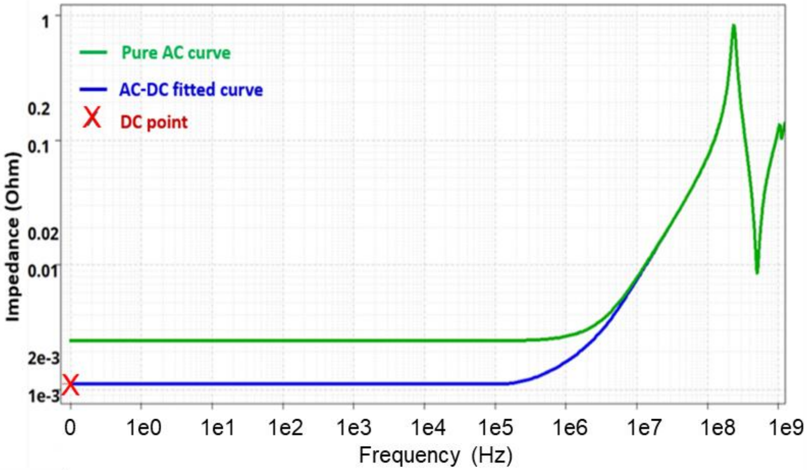
- The state-quo transient simulation flow with a SPICE-ready macro-model, converted from a raw S-parameter, is resource intensive in both headcount and cost in $
  - ✓ SPICE-ready macro-model conversion usually takes several hours manually tuning of various parameters for a reasonable Z(f) correlation in frequency domain
  - ✓ Substantial license cost for the industry-standard 3rd party macro-modeling conversion EDA tool
  - ✓ Transient simulation in time domain is also very time consuming, due to the intricate frequency-dependent network with numerous ports



Impedance miscorrelation between .cir model from 3rd party EDA tool, and original S-par model

Problem Statement (2)

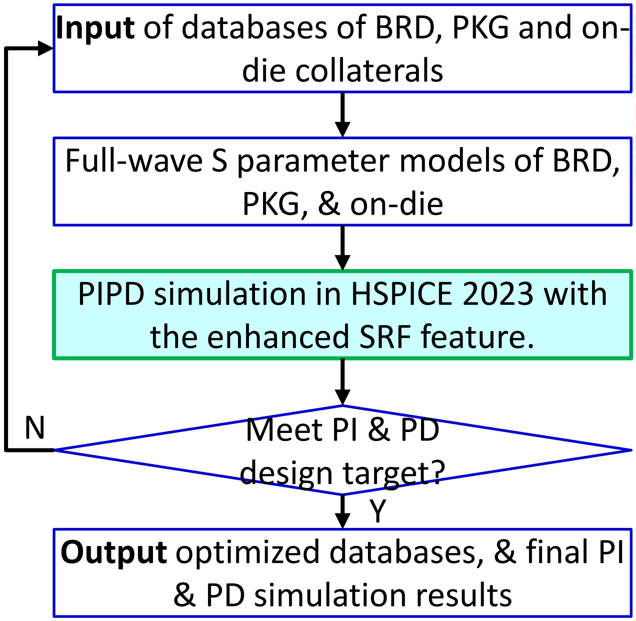
- ☐ S parameter model DC point, solved from DC solver, not being anchored at, leads to inaccurate PIPD sim
  - ✓ S parameter solved with AC solver is not accurate in low frequency, from several MHz down to DC
  - ✓ During AC-DC blending anchoring at 1Hz instead of DC, leads to incorrect results in low frequency
- ☐ A SRF model converted from a S parameter model, without anchoring at DC point, will lead to inaccuracy in low frequency, from several MHZ down to DC
  - ✓ Even from a DC-fitted S parameter, with DC point, and then frequency points start from 10KHz



Impedance with AC-DC fitting blending:

- Correctly converged at 0 Hz (blue curve)
- Non-converged at 0Hz (green curve)

Proposed Solutions (1)



Input of databases of BRD, PKG and on-die collaterals

Full-wave S parameter models of BRD, PKG, & on-die

PIPD simulation in HSPICE 2023 with the enhanced SRF feature.

Meet PI & PD design target?

N

Y

Output optimized databases, & final PI & PD simulation results

Enhanced SRF conversion in low frequency range: several MHz down to DC

Saves significant resource in converting a raw S parameter model into a SRF model directly in HSPICE than that in a 3rd party EDA tool

- **Transient Simulation with SRF Model directly in HSPICE, after achieving AC impedance correlation between SRF and original S parameter model, to achieve preferred significantly improved efficiency, accuracy & consistency**

Proposed Solutions (2)

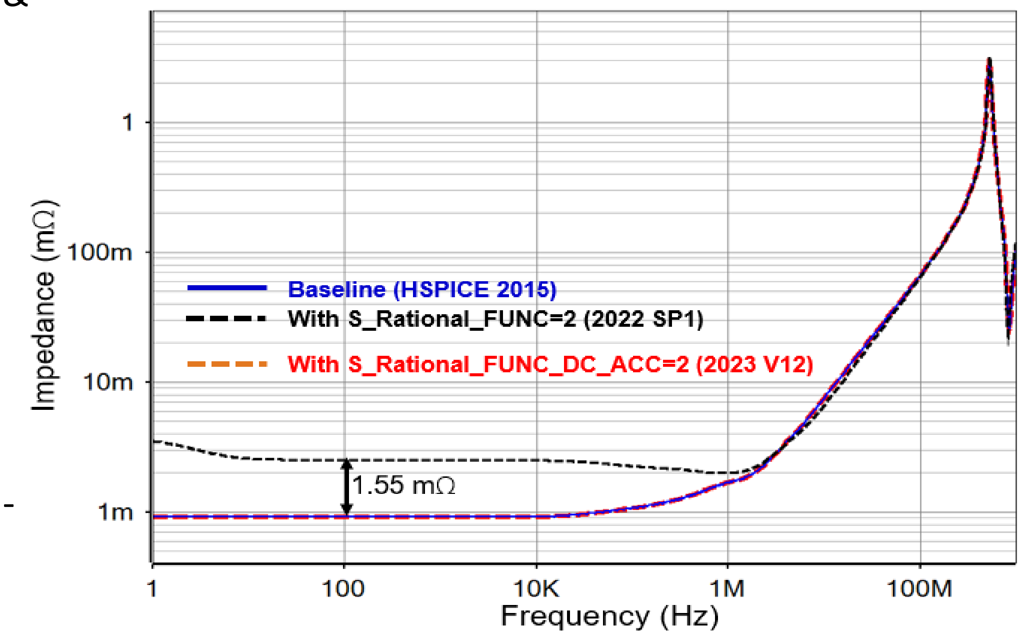
Improved S-par Rational Function (SRF) option in HSPICE 2023.12

- ☐ In HSPICE 2022
  - S_RATIONAL_FUNC=2 results in impedance offset, due to arching at 1Hz
- ☐ In HSPICE 2023.12
  - SRF algorithm has been improved by S_RATIONAL_FUNC_DC_ACC = 2
  - ○ Enforce SRF model conversion from the raw S-parameter exactly anchoring at DC (0Hz) , ensuring the accuracy in whole frequency range, for AC and transient analysis
  - ○ Make sure the impedance simulation with the SRF model is correlated that with the raw S-parameter model, before the converted SRF being used in transient simulation
  - ○ Help remove impedance glitches in low frequency range, which help further mitigate the non-convergence issue in transient simulation.

Improved SRF Model in HSPICE 2023-V12

To achieve Z(f) correlation between using raw S Parameter model and SRF model-

- ☐ The raw S-parameter model included in HSPICE deck should always have DC point, & DC-AC fitted
- ☐ The raw S-parameter with 200+ ports converted into SRF model in HSPICE 2022 SP1, results in impedance offset, below ~1MHz
- ☐ This impedance offset is mainly due to the setting SRF=2, prompting significant manipulation SRF algorithm in HSPICE, by Synopsys R&D
- ☐ With enhanced SRF model in HSPICE 2023-V12, impedance offset is eliminated, correlated w/ baseline case of the raw S-parameter model

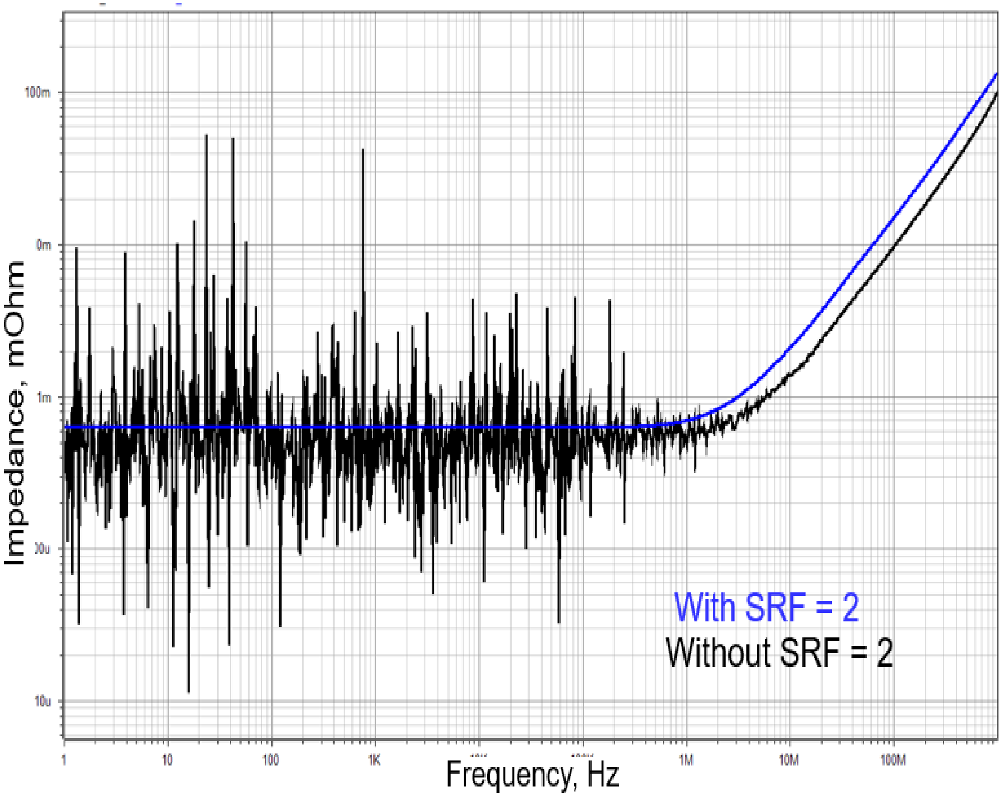


Impedance offset with SRF=2 with HPP

- checked in HSPICE 2022 SP1;
- fixed in HSPICE 2023 V12

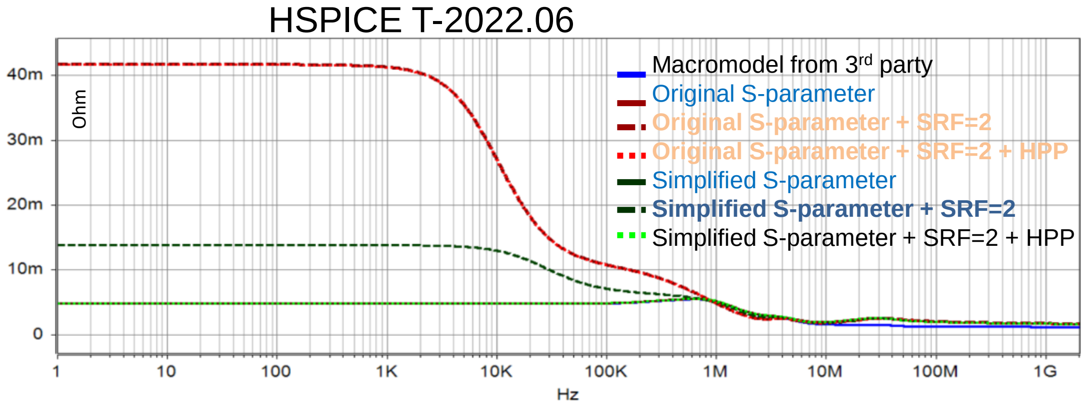
Reduced Impedance Glitch in Low Frequency Range with S_RATIONAL_FUNC_DC_ACC = 2

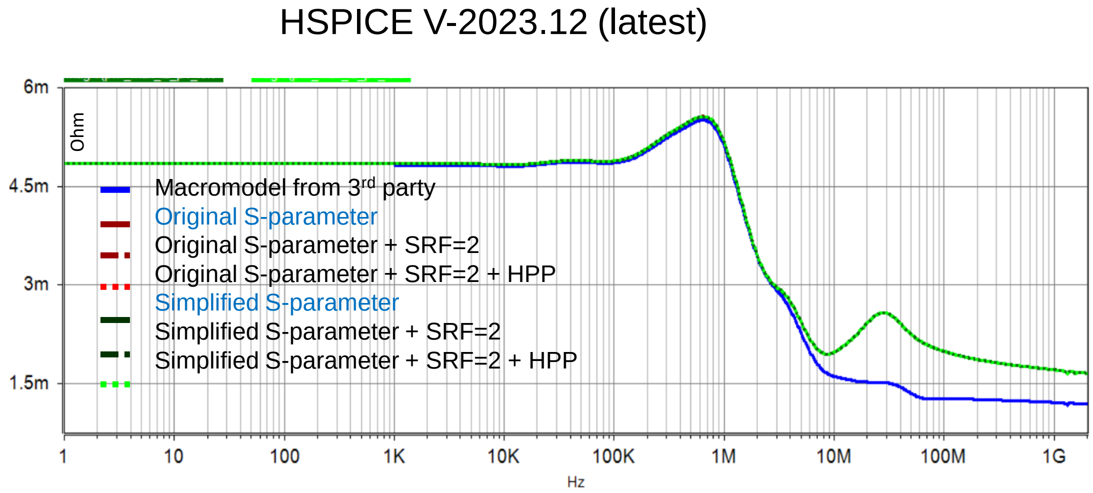
- ☐ With S_RATIONAL_FUNC=2 in HSPICE 2022.06- SP1
  - – there **is possible** impedance glitches in low-frequency range from ~1MHz down to DC
- ☐ With S_RATIONAL_FUNC_DC_ACC=2 in HSPICE 2023.12
  - – the impedance curve remains smooth across the entire bandwidth (Blue curve)



Case Study 1: AC Impedance, Z(f) Correlation

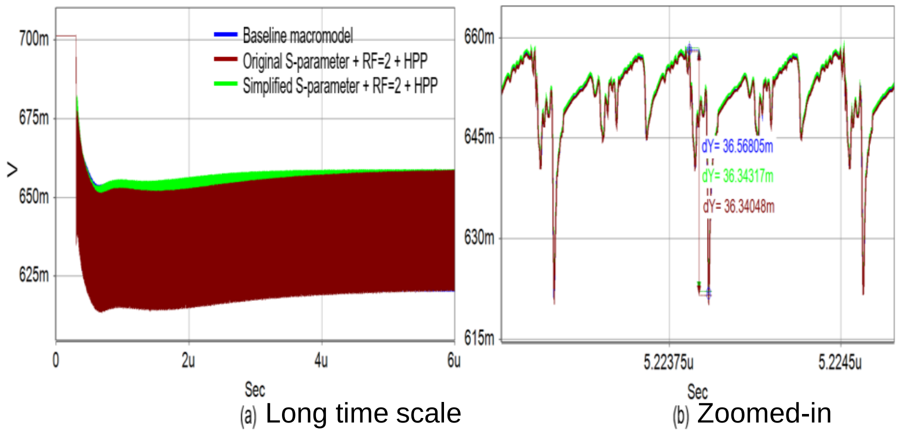
- ☐ With SRF=2 in HSPICE T-2022.06, impedance in low frequency range boosts x3 (worst-case) with simplified or original S-parameter
- ☐ S_RATIONAL_FUNC_DC_ACC = 2 in HSPICE V-2023.12, Z(f) correlates well, with or w/o HPP
  - ☐ With latest HSPICE V-2023.12, no impedance-boosting issue in below 1MHz down to DC
  - ☐ S_RATIONAL_FUNC_DC_ACC = 2 helps more accuracy in high frequency above 1MHz.


HSPICE T-2022.06


HSPICE V-2023.12 (latest)

Case Study: Transient Simulation in Time Domain

Case-1

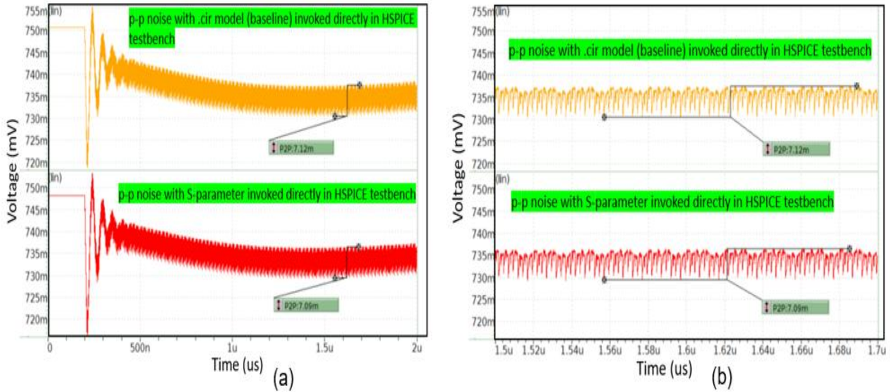


Long time scale

Zoomed-in

Delta: 0.22/36.56=0.6%

Case-2



Long time scale

Zoomed-in

Delta: 0.03/7.12=0.4%

- ☐ Transient simulation results correlated well between using .cir macro model converted by 3rd party tool and SRF model directly converted in HSPICE, from the same raw S parameter model
  - High frequency Vpp noise difference is <1%, between baseline .cir model & SRF model

Case Study: Transient Performance Metrics

Case-1	Model type	Simulation time (days)	Output file size (GB)
Baseline	Macromodel (*.Cir)	3.8	17.3
Test 1	Original S-parameter	4.4	33.5
Test 2	Simplified S-parameter	3.2	16.8
Test 3	Original S-parameter + SRF=2 + HPP	1.76	17.4
Test 4	Simplified S-parameter + SRF=2 + HPP	1.74	17.5

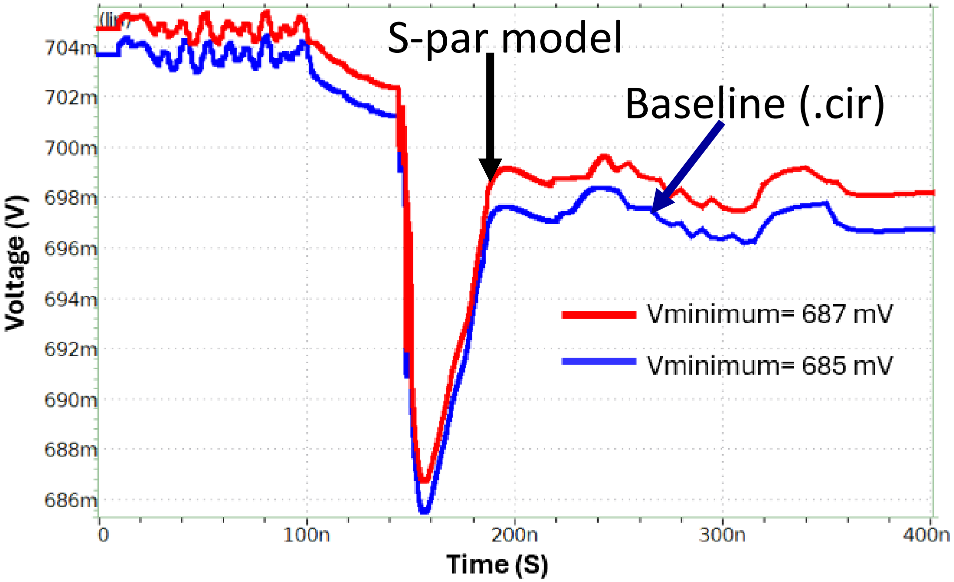
❑ With S_RATIONAL_FUNC_DC_ACC = 2

– the simulation efficiency is improved, while maintaining the same accuracy
  - Case-1 ~50%, ~(3.2-1.74)/3.2 as listed in the table, and
  - Case-2 ~66.7%, not listed in the table

– the simulation consistency is achieved
  - without any ambiguity in converting into *.SRF model directly in HSPICE from a raw S-parameter model (200+ ports)

Case Study on 3D Foveros Package: Time Domain (TD) Metrics

- Motherboard and 3D Foveros package S-par model cascaded for TD analysis
- SRF with DC accuracy=2; DCFitted S-par including 0Hz
- High current power domain in the Package
- Difference of Vminimum between .cir model and S par model = 2 mV (~0.3%)
- The simulation runtime using SRF is 52% lower than the baseline test case



1st voltage droop performance with baseline and S-par models

Test type	Model type	Simulation time	Vminimum (mV)
Baseline	Macromodel (*.Cir)	28.10 hrs	685
S-par model	Original S-parameter (BRD and PKG)	13.46 hrs	687

Ongoing Activity

- ☐ Expand and testify the workflow for simulating and correlating of AC impendence and transient peak-to-peak noise, with
  - ✓ Closed loop VRM based transient noise simulation
  - ✓ More sophisticated on-die model, including mixed signal components

Conclusion

- An automated and self steering flow is created & correlated within HSPICE to improve the effectiveness of platform level power delivery network (PDN) design for 2.5D Co-EMIB/3D advanced (Foveros) packages in practical product
  - S_RATIONAL_FUNC_DC_ACC = 2 in HSPICE 2023, boosts transient simulation efficiency
  - Parallel computing HPP, further boosts sim efficiency, significantly reducing simulation time
  - The simulation consistency is achieved without any ambiguity in SRF model conversion
- This novel workflow improves simulation efficiency by reducing correlation time, & optimizing resources, and ensuring precise power delivery and power integrity analysis
  - The said flow is validated through multiple practical PDN design cases for 3D Foveros packages with >300 RF ports

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