Saras eVR STile - Enabling the Next Generation of AI & HPC Power Delivery Network Designs

Bart DeProspo
Senior Director of Business Development

Outline

- Company Introduction
- Power Challenges
- Saras STile Solution
- Summary and Conclusions

Saras Micro Devices Introduction

APRIL 2021
Founded in Atlanta, GA by Novelis

NOVEMBER 2021
Acquired and fully funded by KCK Group

AUGUST 2022
Opened Cupertino, CA sales office

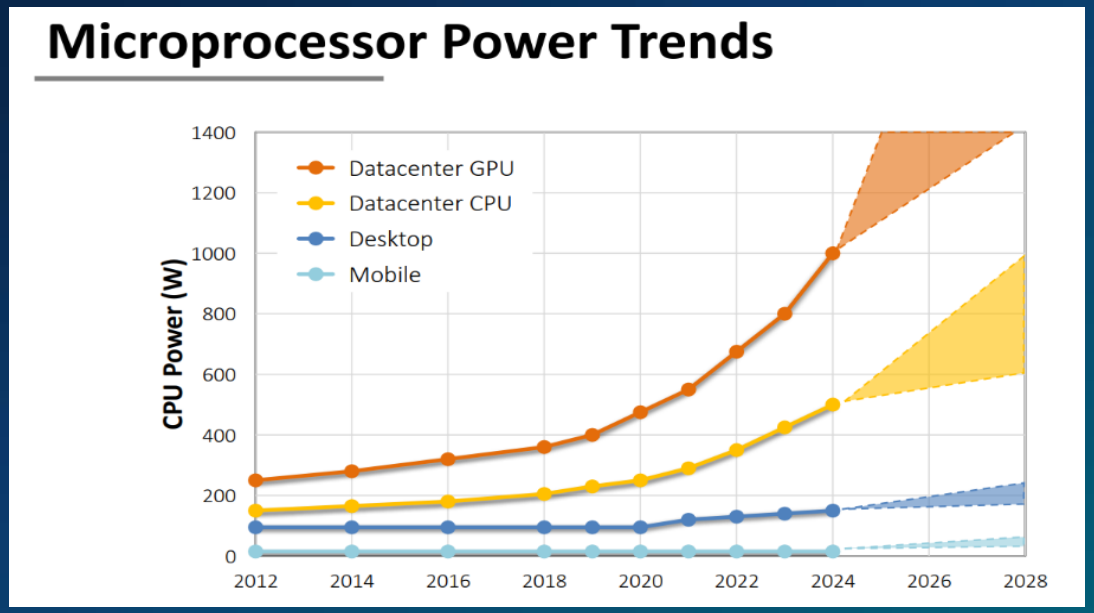
MARCH 2023
Awarded 'Start-Up of the Year by 3D Incites

AUGUST 2023
Opened new Atlanta, GA R&D Center: Inland Tract

JANUARY 2024
Opened new Chandler, AZ HQ and US Manufacturing Center of Excellence

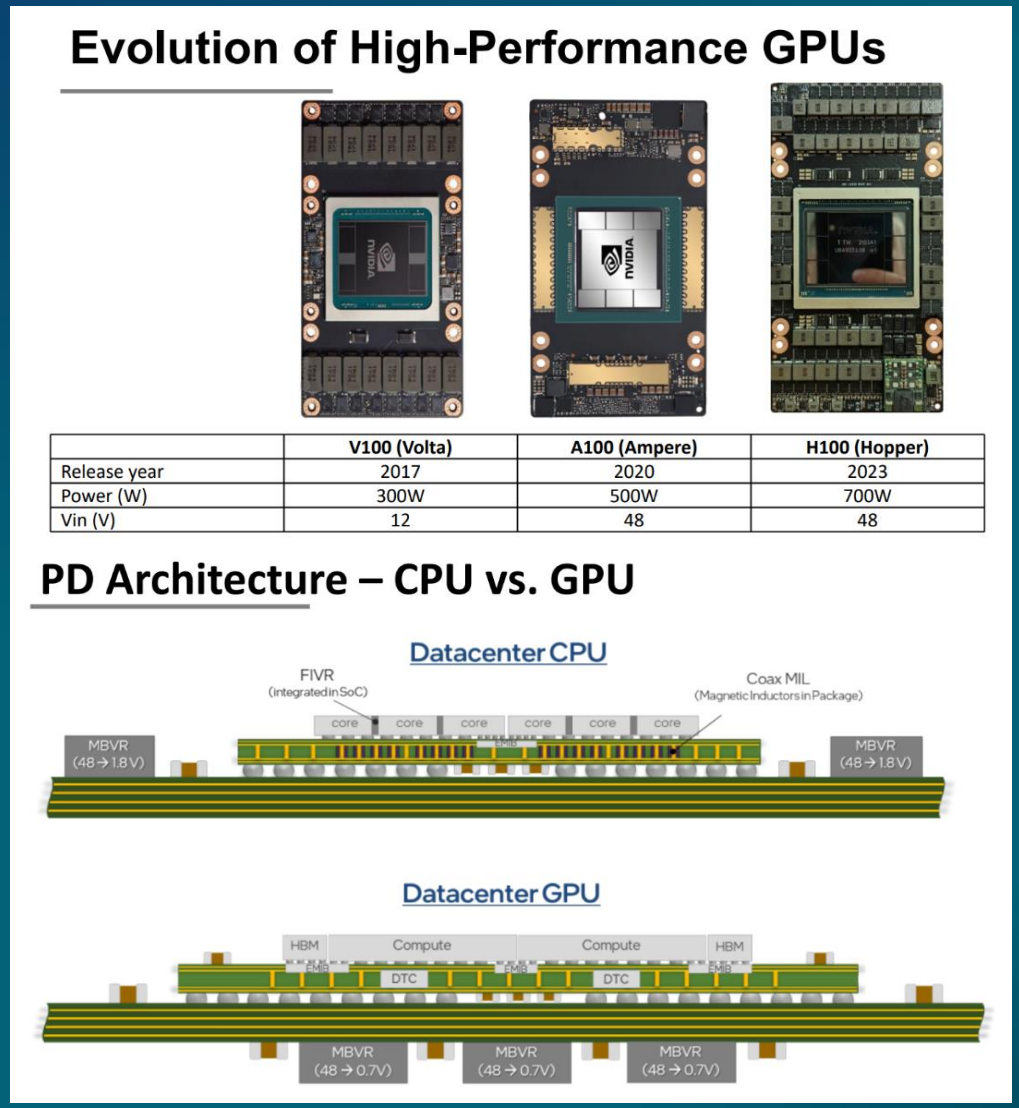
To be the leading supplier of embedded power delivery solutions for AI and HPC devices

Power Problem



Source: Intel 2024[1]

- Increasing Power and Current Density
- Rising I^2R losses due to higher I and lower V
- Reduced space for package level Caps

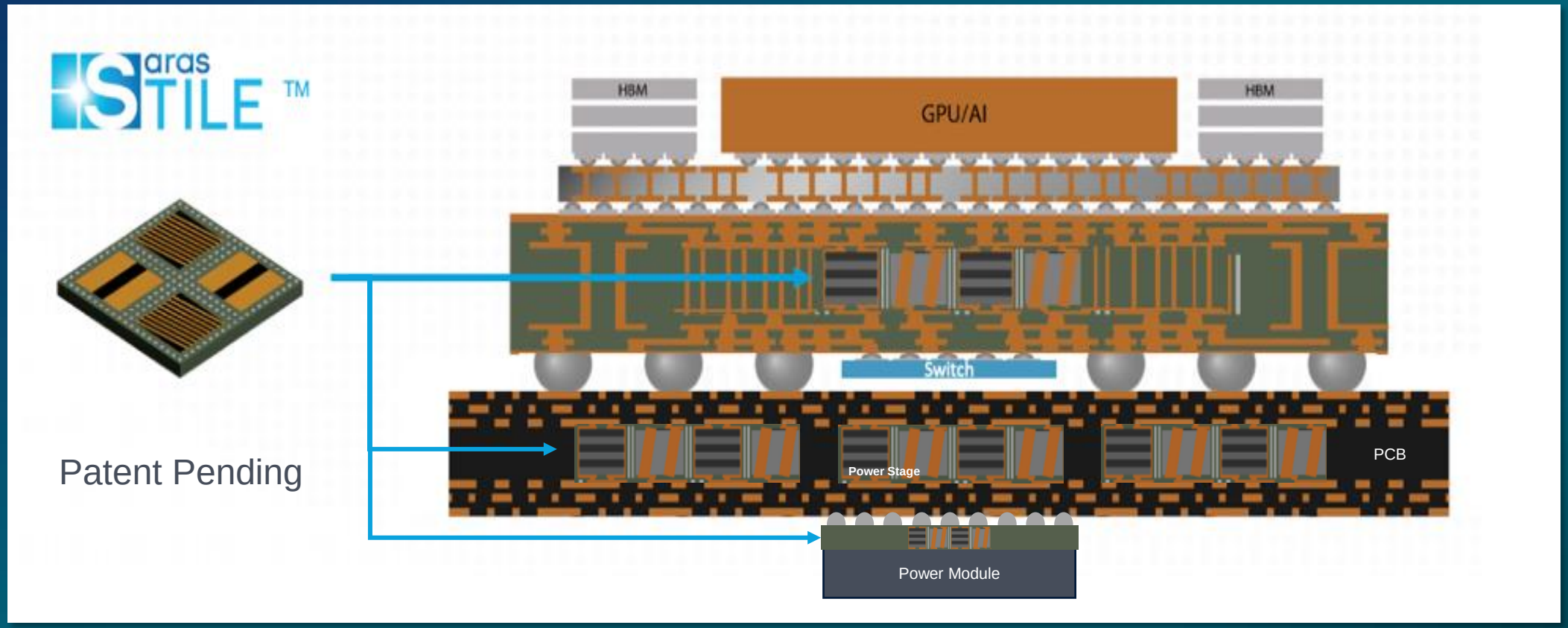


	V100 (Volta)	A100 (Ampere)	H100 (Hopper)
Release year	2017	2020	2023
Power (W)	300W	500W	700W
Vin (V)	12	48	48

Source: nVidia 2024[2]

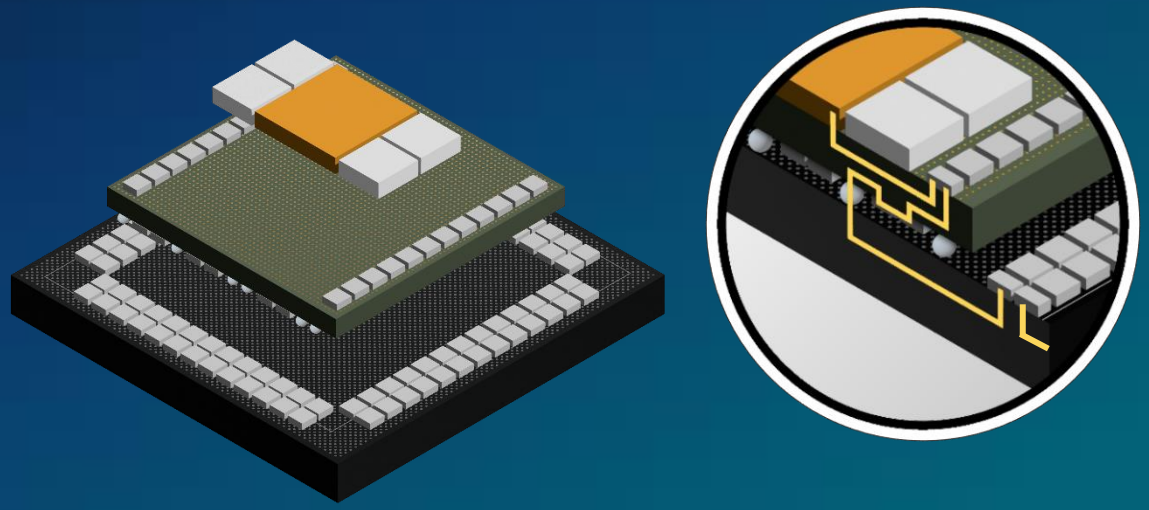
Saras Tile (STILE ™) | Applications

- Saras substrate integrated passive STILE ™ solutions enable the next generation of power delivery architectures for data center processors & accelerators



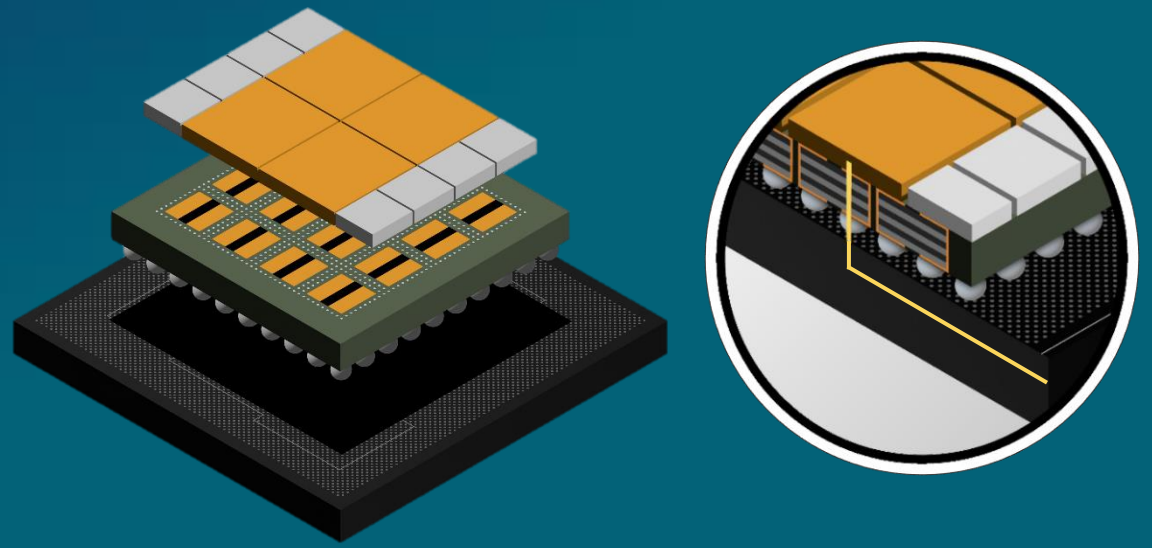
Saras STile™ | Benefits

Existing Designs



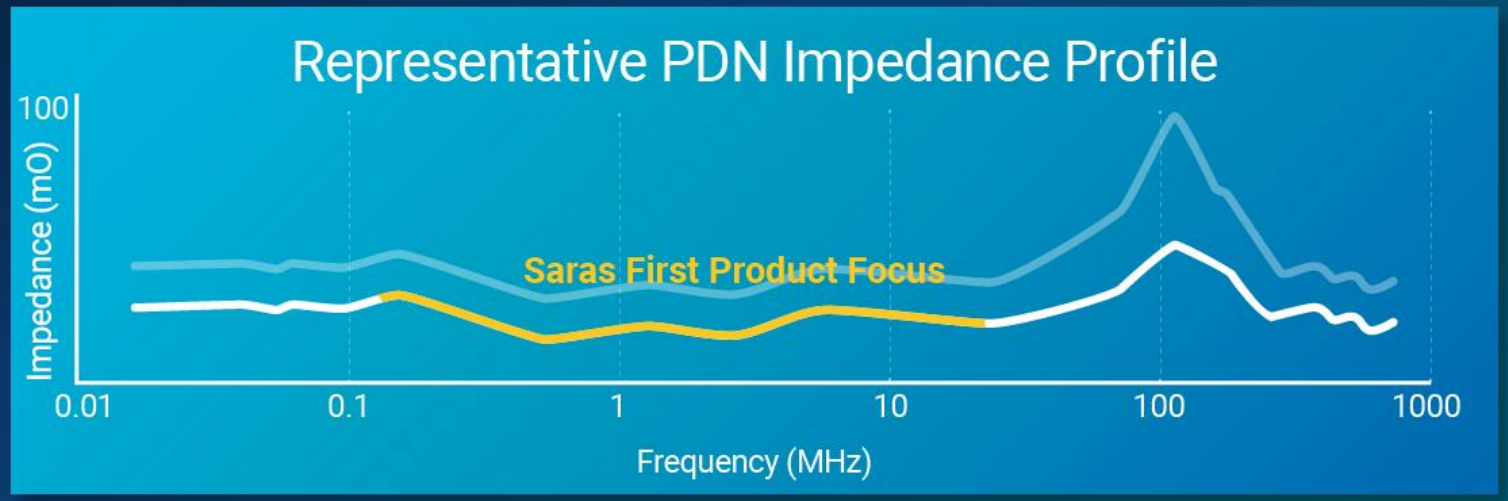
- PCB located power conversion
- Long power path routing lengths – high IR loss
- Hundreds of passives required

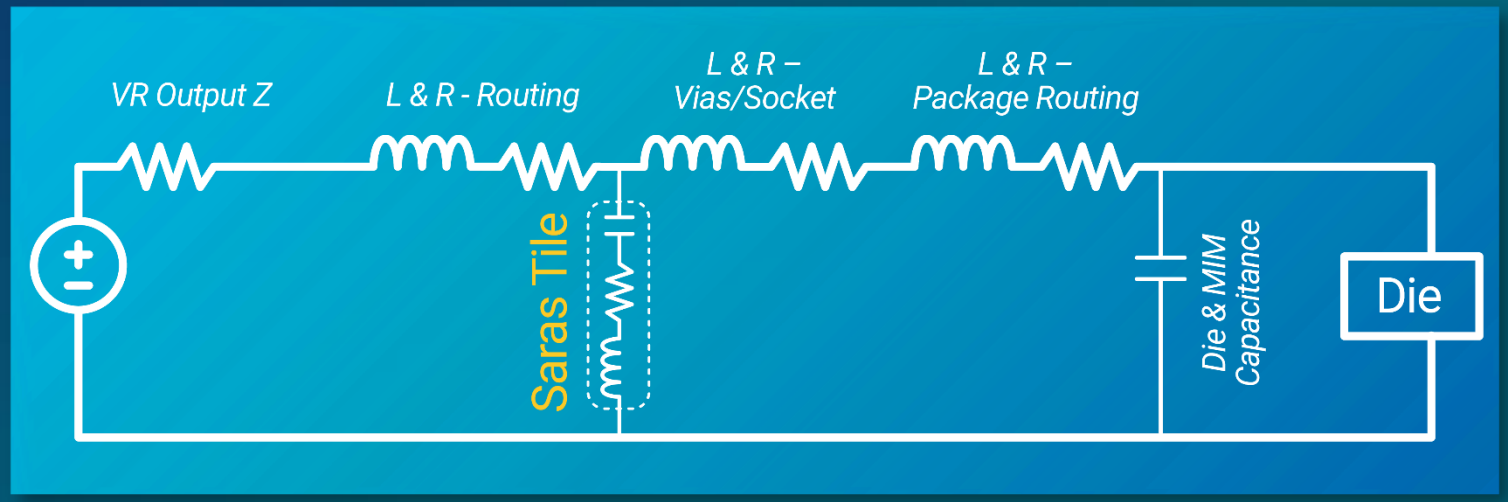
Saras STile™ Enabled Design



- Device specific STile – embedded & known-good
- Vertical Power Delivery – significantly lower IR loss
- No routing restrictions from passive components

Product Application Focus

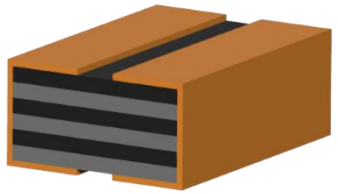




STile PDN Benefits

- Design Simplicity
- Higher Performance
- Larger Area Real Estate for Silicon

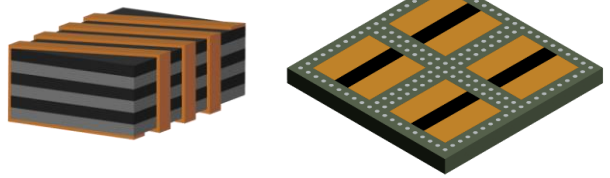
Product Development Roadmap



Capacitor Development

- Stacked Capacitive Element Development
- Formfactor and Performance Customizability

Continuous Improvement

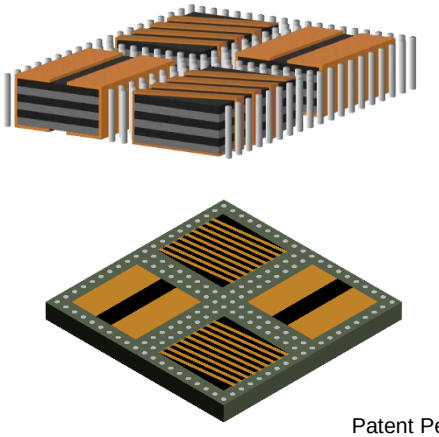


Patent Pending

Inductor Development & STILE ™ Integration

- Inductor Introduction
- Multi-domain Capacitor Tile

Focus - 2024



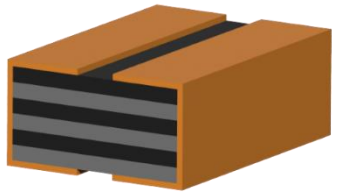
Patent Pending

Embedded VR Filter

- Combination L+C Tile Technology
- Performance optimization under workload variability

Introduce 2H 2025

Product Development Roadmap



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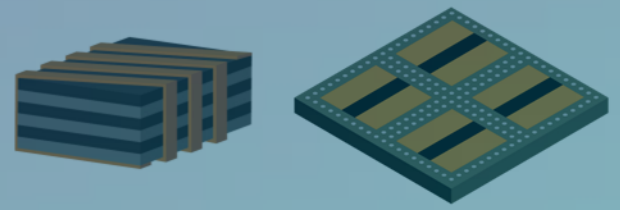

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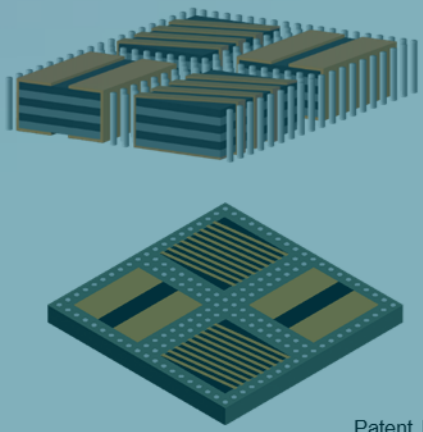

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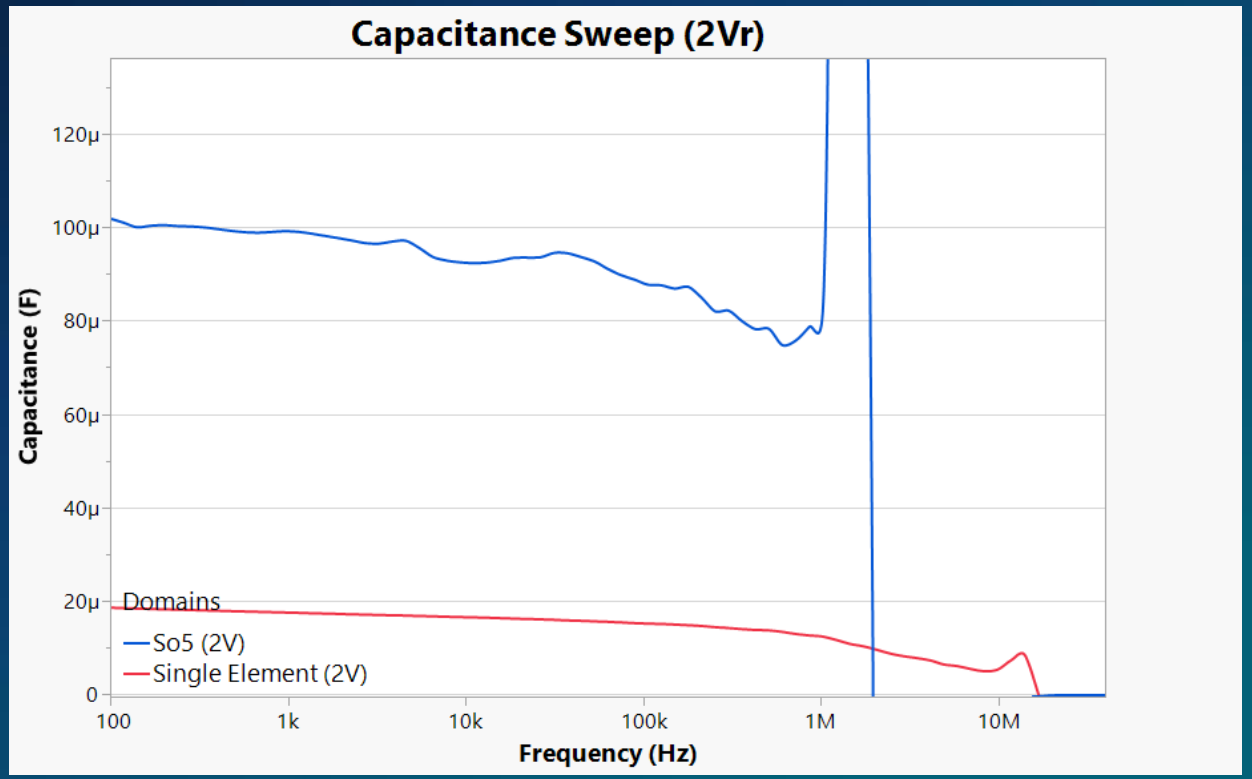
Introduce 2H 2025

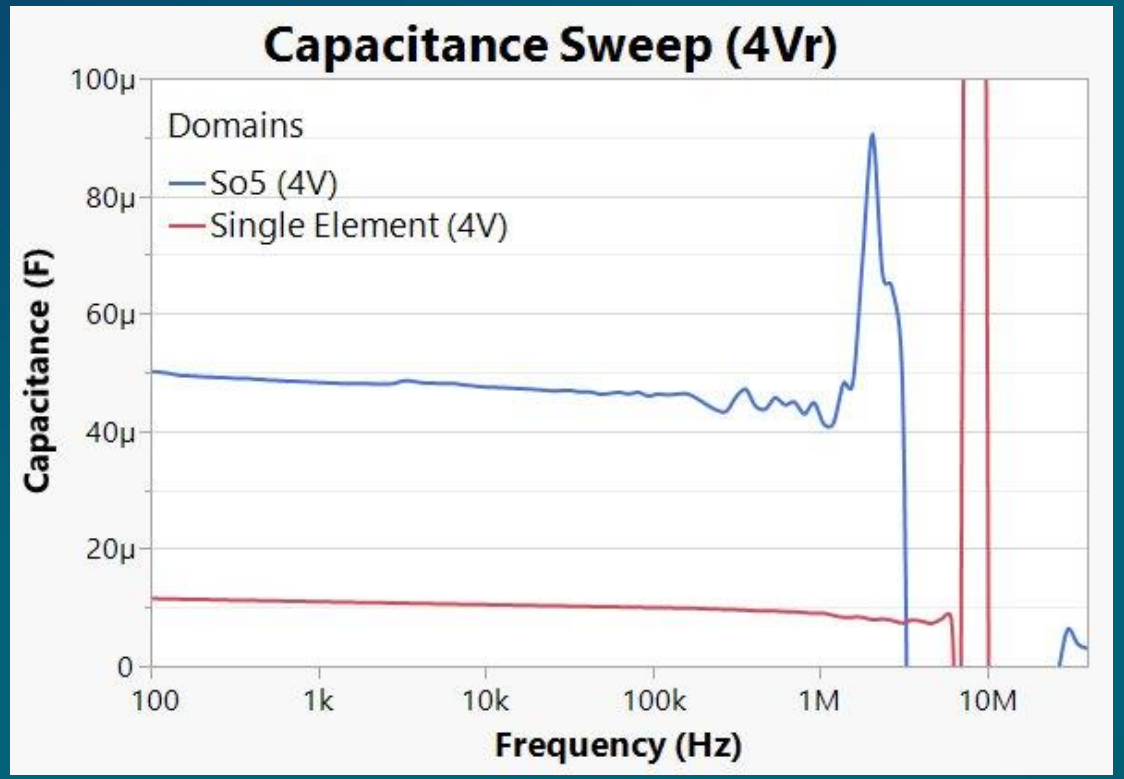
Capacitor Device Performance

Capacitive Cell Size Examples		2V	4V	Comment
Dimension XY (mm)		4.0 x 4.0		Additional customization available upon request
Min. Capacitance (uF) @ 100kHz	800 um high	64	24	1.5 µF/mm^2 – 4.0 µF/mm^2. Higher Density on Request
	1000 um high	72	32	2.0 µF/mm^2 – 4.5 µF/mm^2. Higher Density on Request
	1200 um high	80	40	2.5 µF/mm^2 – 5.0 µF/mm^2. Higher Density on Request
R_s @ 100 KHz (mΩ)		< 15	< 15	
ESR @ S.R.F. (mΩ)		< 10	< 10	
ESL*		< 20 pH	< 20 pH	
Resonant Frequency		< 5 MHz		Dictated by Capacitance Value
Operating Temperature Range		0ºC – 125ºC		
Capacitance Variation versus Temperature		< 10%		Preliminary Reliability Data
Rated Voltage		2V / 4V		Higher RV possible
Capacitance Variation versus RVDC		< 5%		Limited Test Data Available

- Cell sizes shown are for illustrative purposes – custom sizes available based on customer design specifications
- All table values are preliminary and subject to change

Performance Customizability

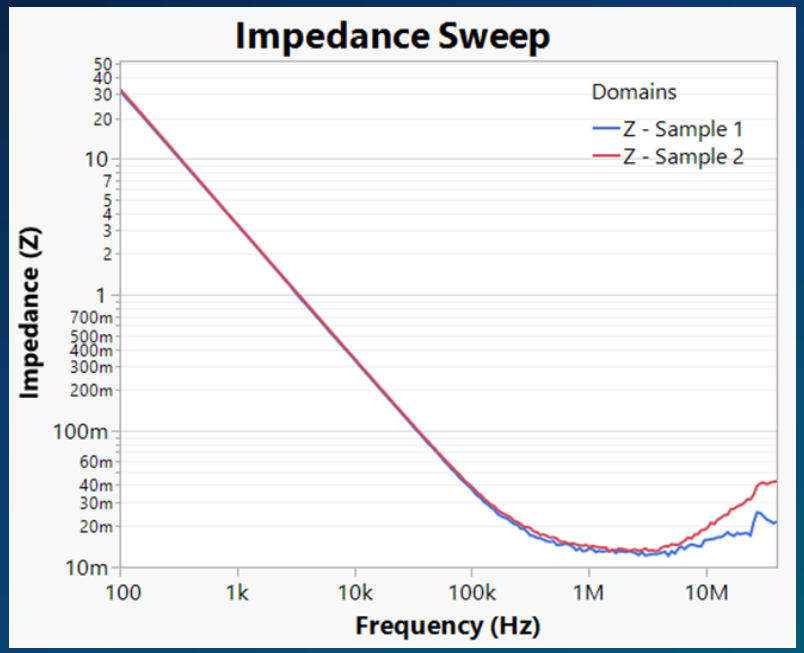


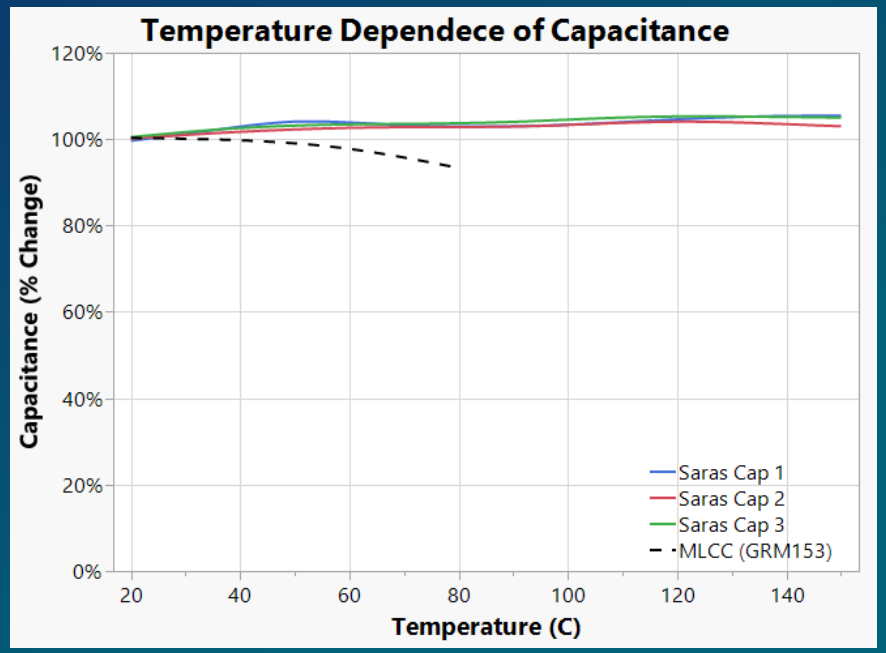


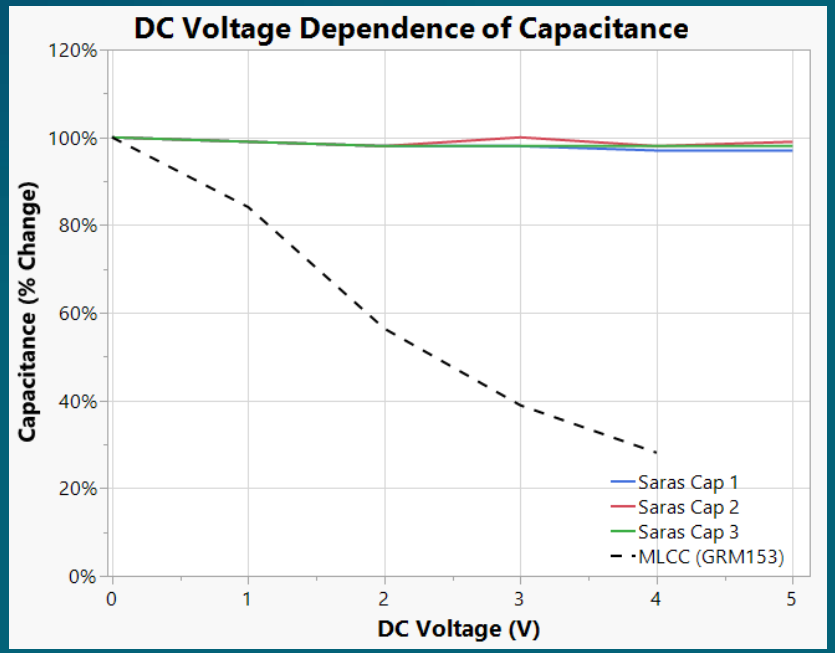
- Cell Size: 4 x 4 mm
- Single layer vs. five layer
- 2V operating rated vs. 4V operating rated

- Capacitance increases with lower operating voltage rating
- Resonant frequency decreases with cap density increase

Capacitor Performance







- Broadband impedance
  - Measured data for single layer 4x4mm cell
- Capacitance change temperature
  - <10% change in capacitance from 25ºC to 150ºC
- Capacitance change versus DC bias
  - <5% change through increasing DC Bias

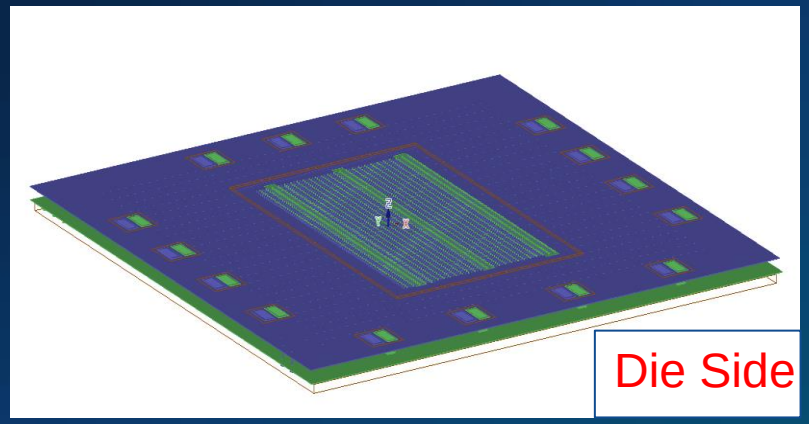
Saras Capacitors Outperform MLCC's

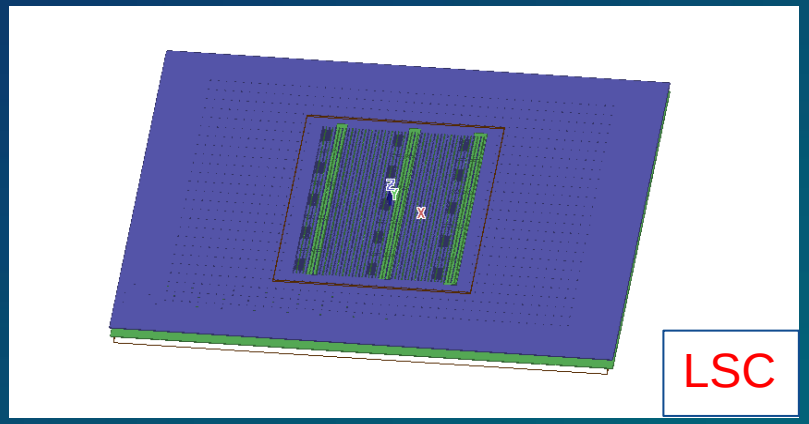
Capacitor Reliability Testing

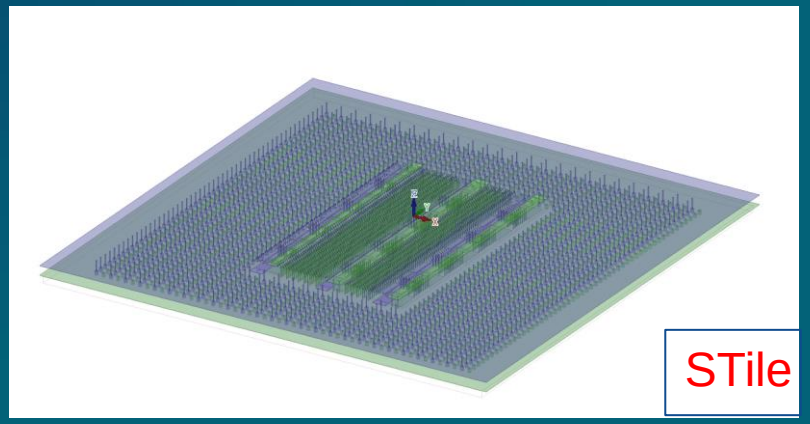
Test	Test Conditions	Test Targets	Test Duration	Results
HTS	150°C	500 Hours	500 Hours	**<10% Change in C_s/R_s**
Bias Test	4V @ 105°C	150 Hours	720 Hours	**<10% Change in C_s/R_s**
TCG	-40°C to 125°C	1000 Cycles	1200 Cycles	**<5% Change in C_s/R_s**
T/H-1	85°C / 85% RH	500 Hours	1000 Hours	**<10% Change in C_s/R_s**
T/H-2	110°C / 85% RH	100 Hours	800 Hours	**<5% Change C_s/R_s**
bHAST	4V @ 110°C / 85% RH	24 Hours	48 Hours	**<5% Change in C_s/R_s**

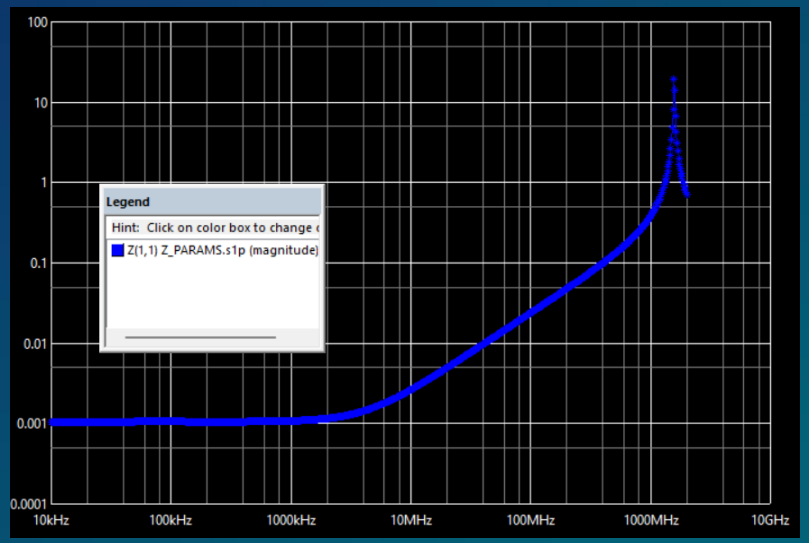
- Capacitor stability through extended reliability test conditions

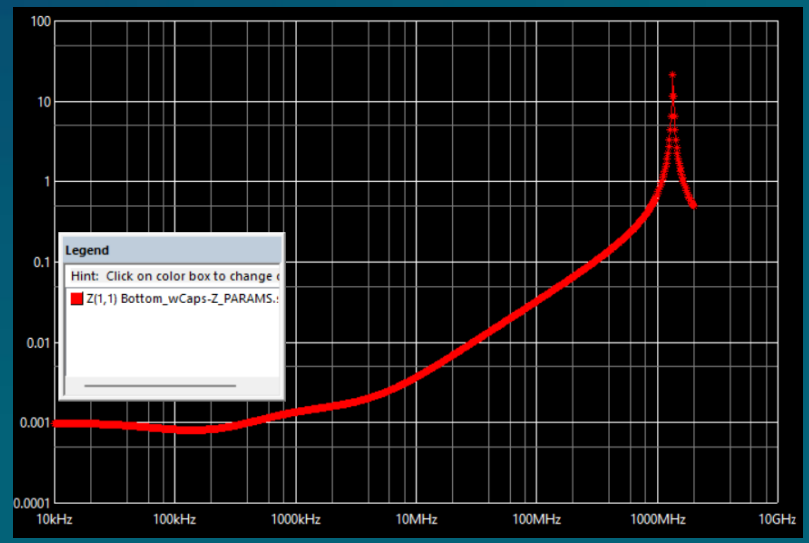
System Level Electrical Models

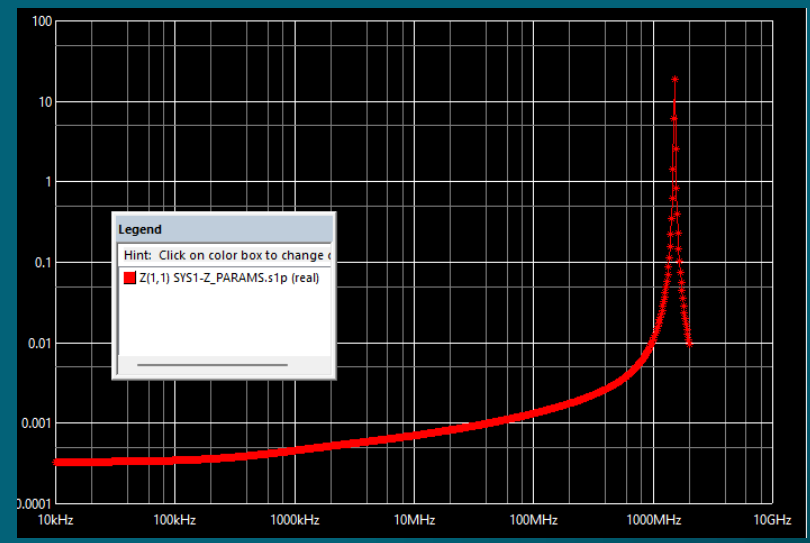






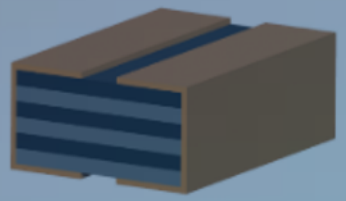






- Significantly lower impedance for all frequency bands with embedded STile

Product Development Roadmap



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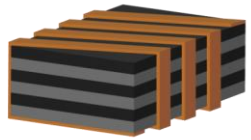
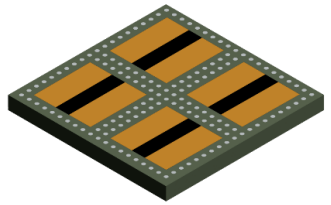
Continuous Improvement





Patent Pending

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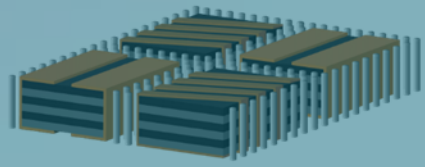
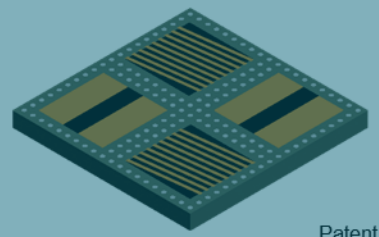
- Inductor Introduction
- Multi-domain Capacitor Tile

Focus - 2024





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Introduce 2H 2025

Inductor Development | Progress Update

Demonstrated Performance

Parameter	Unit	eVR (Co-Axial)	VRM (Solenoid)
Switch Freq	MHz	> 100	1 – 5
DCR	mΩ	< 0.5	< 20
Inductance *	nH	3 – 7	10 - 60
Current Density	A/mm2	> 4	> 4
Q Factor		> 10	> 20
Thickness	mm	0.2 – 1.2	0.8 – 1.2
Area	mm2	~ 0.5	design dependent
Vin	V	1.2 – 3.3	12 - 48
Vout	V	< 1	0.5 – 3.3

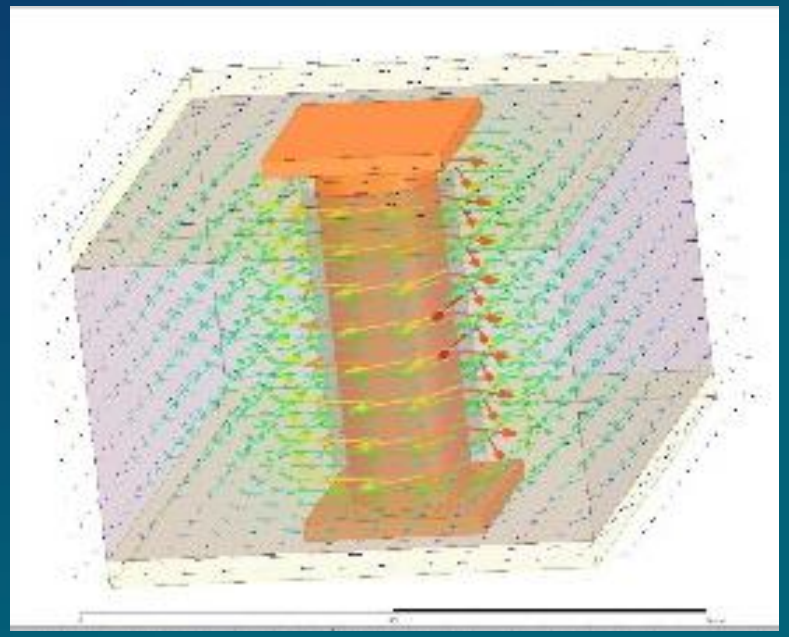
* Inductance density >10 nH/mm^2

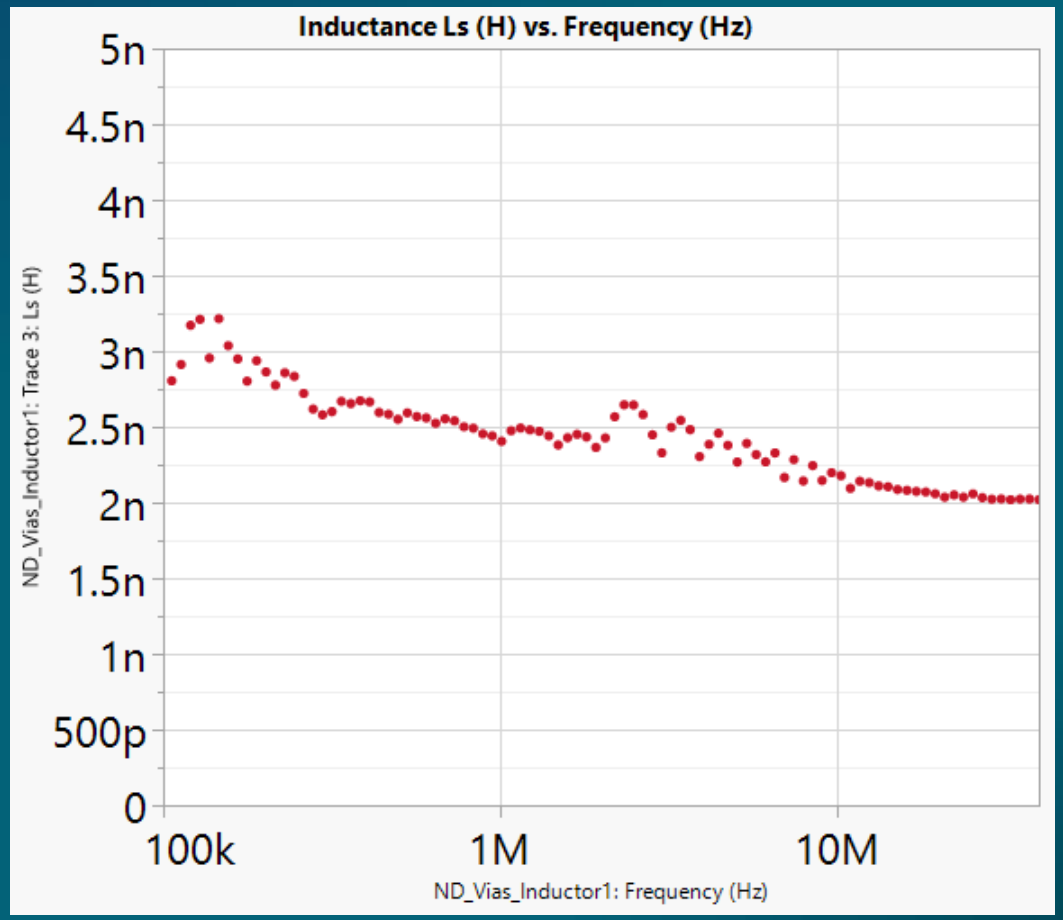
- Various inductor configurations under evaluation
- Co-Axial performance can be varied with via length and diameter
- Solenoid performance can be varied with number of windings
- Inductors for co-integration with capacitors to deliver eVR for processor or power module substrate

Inductor Design | Co-Axial

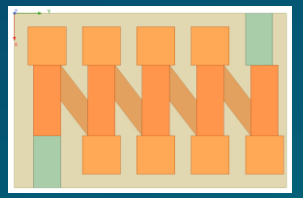
Via Dimension & Performance

- 200um diameter, 550um thickness/length
  - Inductance per via: 2-3nH
  - Inductance density: > 10nH/mm^2
  - < 0.5mΩ DCR





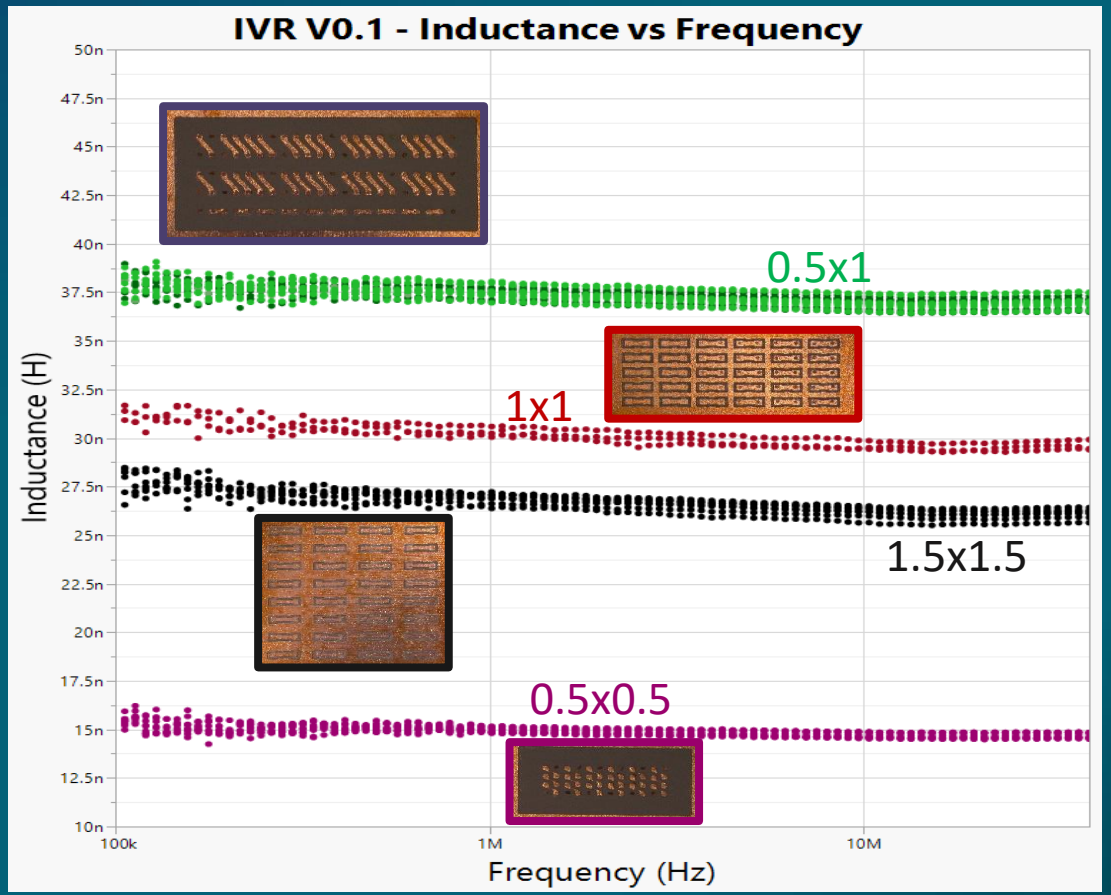
Inductor Design | Solenoid



Performance

- Inductance Density >11nH/mm^2 on 4-turn inductor (~14mΩ DCR)
  - Potential to increase:
    - Higher permeability material
    - Increase material thickness to 1mm
- I_{sat} >100A, I_{rms} limited by dissipation in windings (DCR)

MEASUREMENTS			
Via Pitch – (mm)	(N)	**Avg Measured Ls (nH)**	**Avg Measured DCR (mΩ)**
0.5x0.5	3	15.01	58.70
0.5x1	4	37.54	13.84
1x1	4	30.59	15.84
1.5x1.5	3	26.89	16.53



Conclusions

- Power delivery challenges require new innovations beyond Silicon
- The Saras STile addresses these challenges by:
  - Best in class Capacitance Domain Platform
  - Customizable Inductor Domain Platform
- Introduction of Inductor and Capacitor STile by 2025

Powering the Future

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