

Performing Multiphysics Analysis During Heterogeneous Integration



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3DIC Encapsulates Many Challenges ..

Traditional chiplet design and signoff

- Fit for purpose and manufacturable

Substrate design and signoff

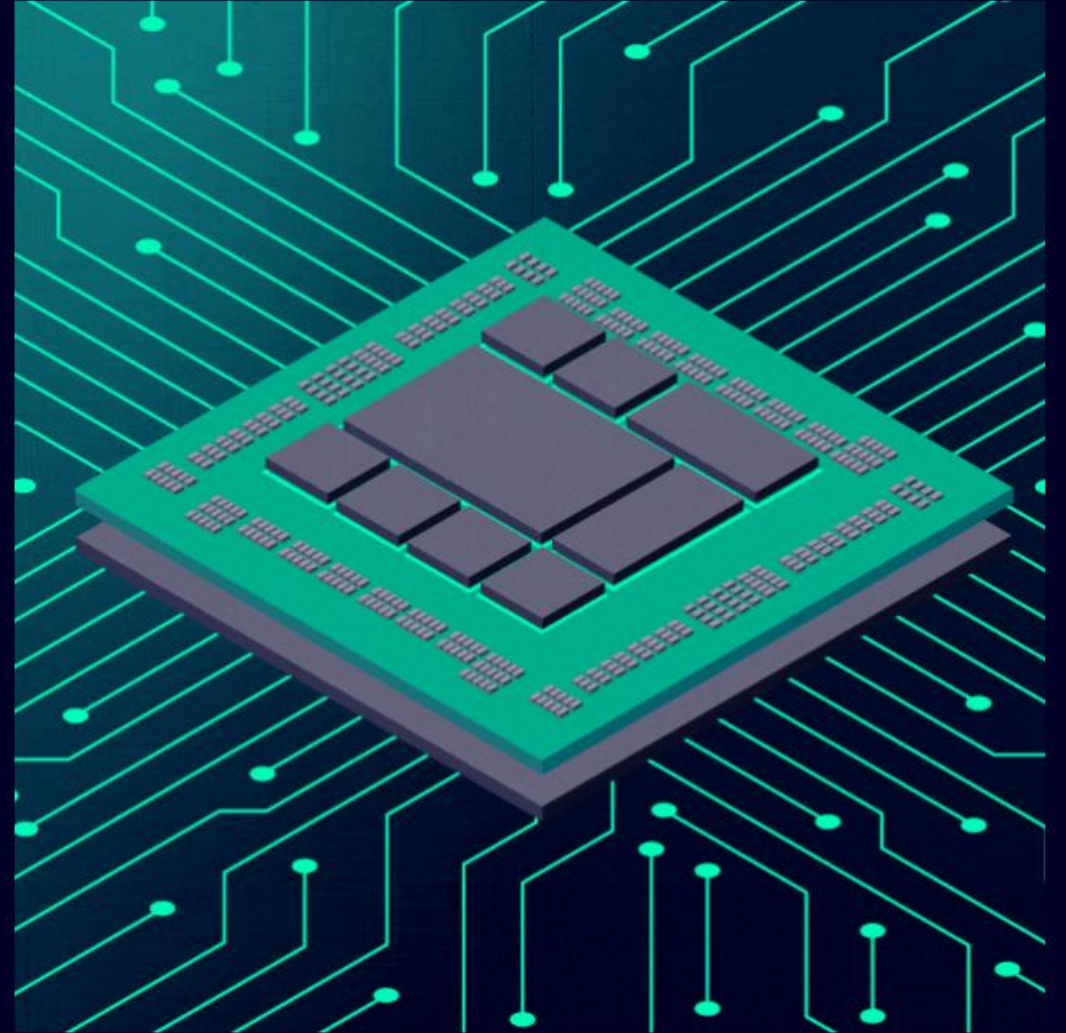
- Interposer and package Substrate

System-level planning and sign off

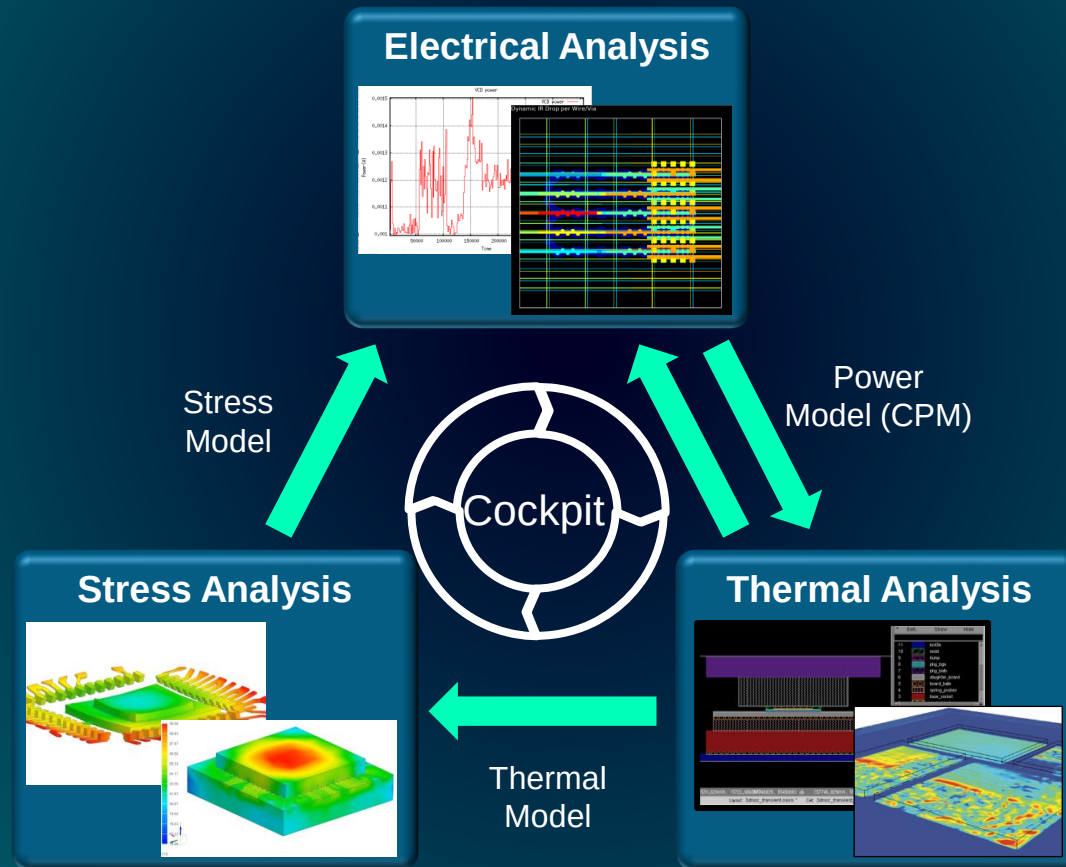
- Across multiple design domains

System-level “Multiphysics” design and signoff

- Die, package, in-system



3DIC Multi-Physics Analysis



“multiphysics simulation (often shortened to simply "multiphysics") is defined as the simultaneous simulation of different aspects of a physical system or systems and the interactions among them.” wikipedia

Electrical power affects thermal behavior

- Due to the resistance of the conductors

Thermal issues affect electrical behavior

- Resistivity of interconnects change with heat

Thermal issues affect stress behavior

- Different CTEs between substrates result into warpage

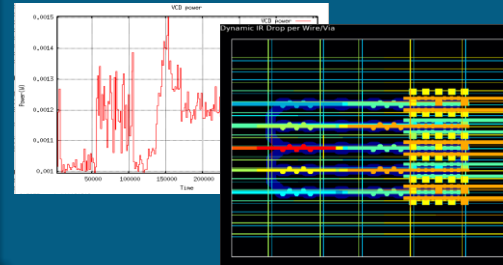
Stress issues affect electrical behavior

- Transistors characteristics change with applied stress

The System Designer Challenge

How Can EDA help?

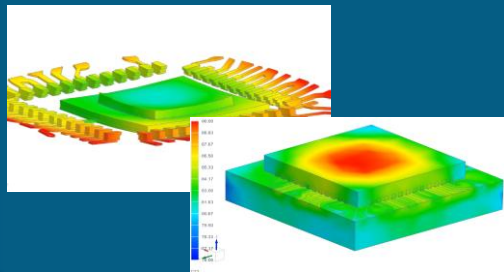
Electrical Analysis



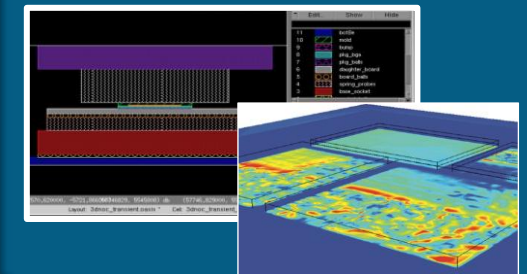
System Level/3D-IC Designer

- Often has an EE or ME background
- Can't be an expert in every verification/analysis flow
- Needs to take “system level” decisions:
 - 3D-IC technology vendor
 - Substrate type (silicon interposer, organic interposer,
 - Die(s) floor planning, etc ..
 - Needs to take the decisions as early as possible

Stress Analysis



Thermal Analysis

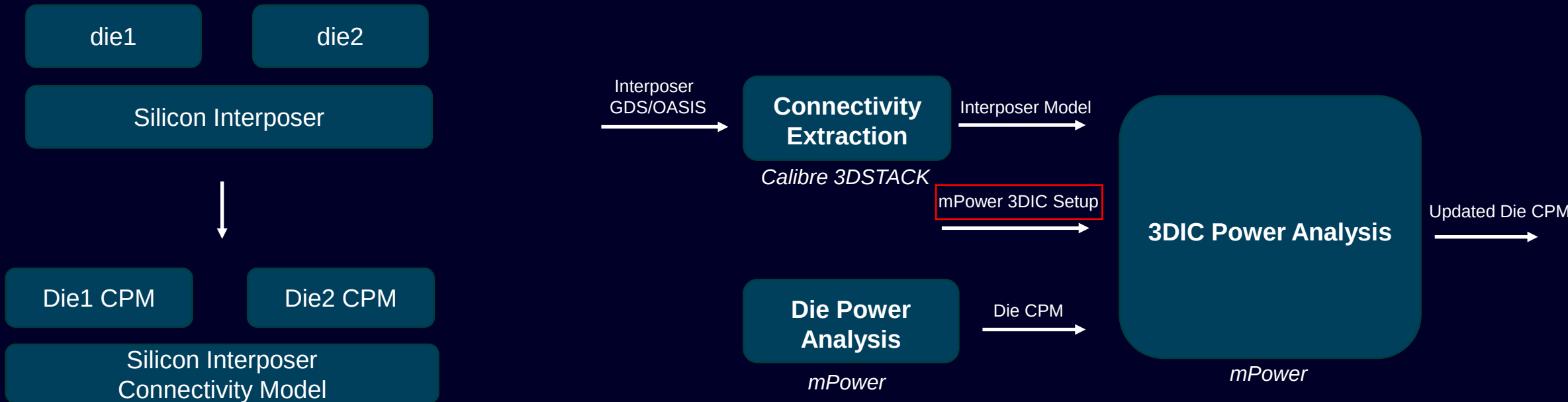


3D-IC Electrical Analysis

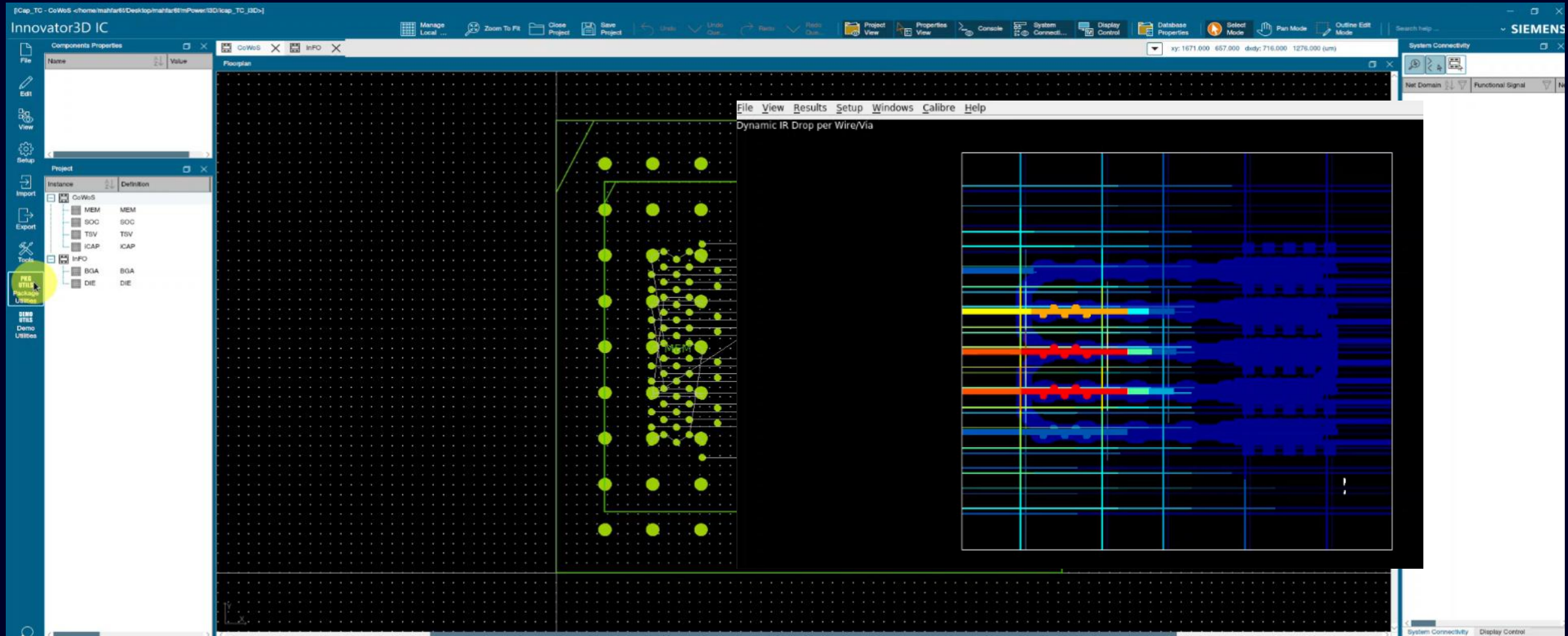
Power is delivered to the die “through” a silicon interposer

- How to account for interposer “non ideal” routing?

Die CPM needs to be updated with “Interposer” effect



3D-IC Electrical Analysis: *Innovator3D IC* & *mPower 3D-IC*



3D-IC Thermal Analysis: *Need*

Greater thermal interaction

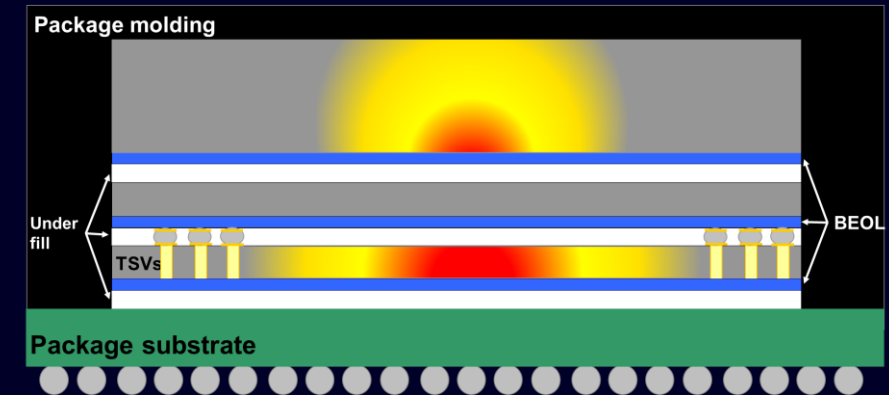
- Active dies are in closer proximity
- Heterogenous integration/different process nodes

Heat dissipation is a main challenge

- Higher power density
- Die bonding results into vertical thermal resistance
- Thinned dies results into lateral thermal resistance

Increased Thermal Gradients

- Non homogenous distribution of 3D interconnects



3D stacked IC



Thermal-related issues

SIEMENS

3D-IC Thermal Analysis: *Requirements*

Die Power Information

- Typically, PD team needs to freeze die design and run power analysis
- To enable early thermal analysis, cockpit platform should generate early power estimates

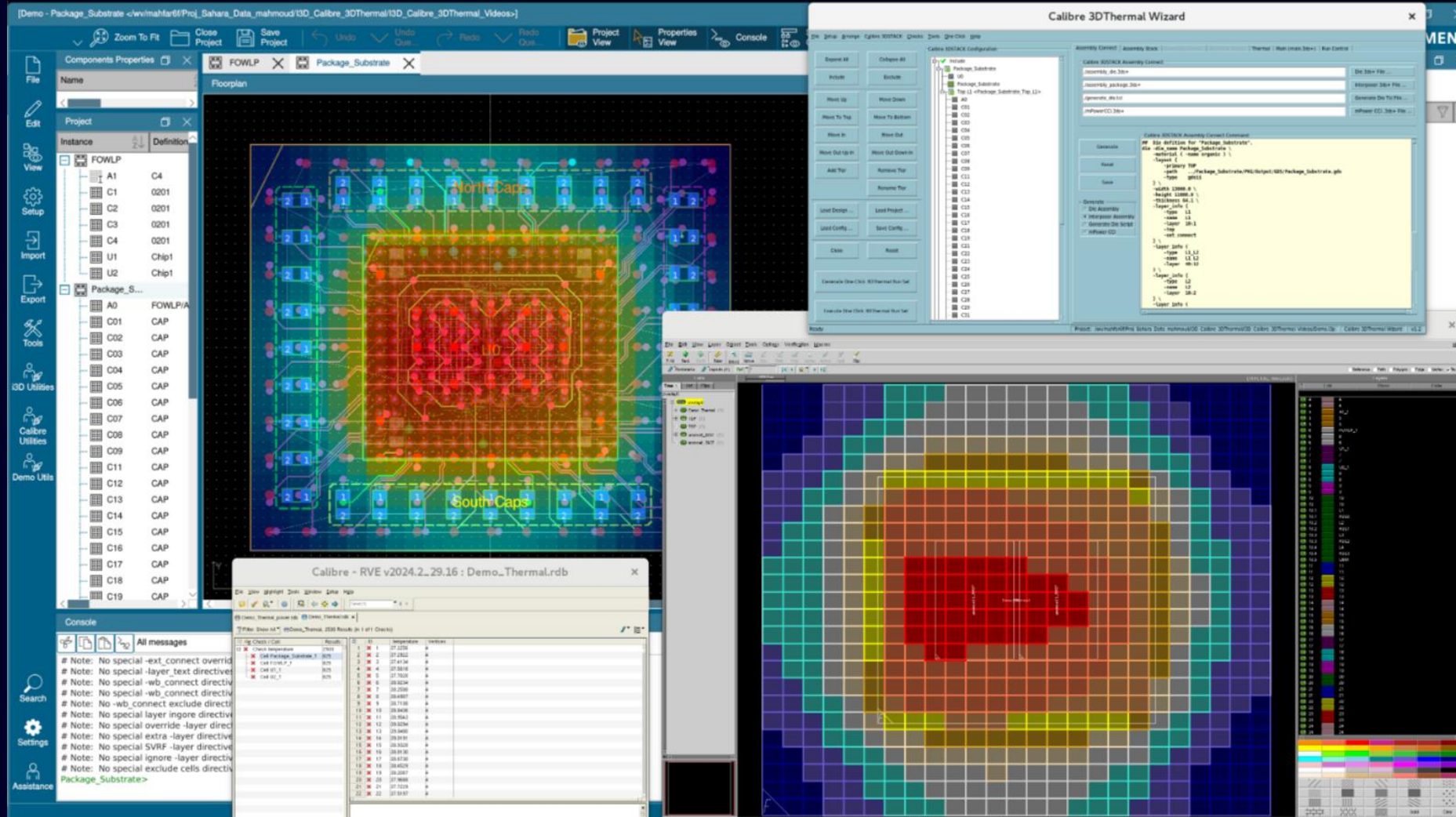
Material Thermal Properties

- Traditionally, die is modeled thermally as “silicon”
- How to account for metallization, TSVs, etc .. in die thermal modelling?
- For accurate die level analysis, “effective” thermal properties should be calculated

3D-IC Assembly Data

- Does the user need to describe assembly, again?!
- Cockpit platform already includes the assembly database

3D-IC Thermal Analysis: *Innovator3D IC & Calibre 3DThermal*



3D-IC Thermal Analysis: *Innovator3D IC Power Map Generation*

Power Map

```

1 #POWER = W
2 #DISTANCE = um
3 0.0 0.0 601.92 668.16 4.000 "U1 (block 0,0)"
4 0.0 668.16 601.92 1336.32 3.000 "U1 (block 1,0)"
5 0.0 1336.32 601.92 2004.48 1.000 "U1 (block 2,0)"
6 601.92 0.0 1203.84 668.16 4.000 "U1 (block 0,1)"
7 601.92 668.16 1203.84 1336.32 2.000 "U1 (block 1,1)"
8 601.92 1336.32 1203.84 2004.48 1.500 "U1 (block 2,1)"
9 1203.84 0.0 1805.76 668.16 4.000 "U1 (block 0,2)"
10 1203.84 668.16 1805.76 1336.32 5.000 "U1 (block 1,2)"
11 1203.84 1336.32 1805.76 2004.48 2.500 "U1 (block 2,2)"
12 1805.76 0.0 2407.68 668.16 4.000 "U1 (block 0,3)"
13 1805.76 668.16 2407.68 1336.32 5.500 "U1 (block 1,3)"
14 1805.76 1336.32 2407.68 2004.48 3.000 "U1 (block 2,3)"
15 2407.68 0.0 3009.6 668.16 4.000 "U1 (block 0,4)"
16 2407.68 668.16 3009.6 1336.32 6.000 "U1 (block 1,4)"
17 2407.68 1336.32 3009.6 2004.48 8.000 "U1 (block 2,4)"

```

Output Power Map File

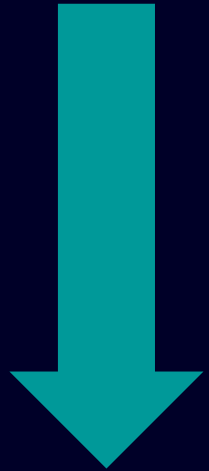
/w/mahfar6/Proj_Sahara_Data_mahmoud/3D_Calibre_3DTherm Power Map File ...

Calibre - RVE v2024.2.29.16 : Demo_Thermal_power.rdb

ID	Block	Power (W)	Distance (um)	Coordinates (X, Y, Z)
1	U1 (block 0,0)	0.0	4.000	0.0, 0.0, 601.92
2	U1 (block 1,0)	0.0	3.000	668.16, 0.0, 601.92
3	U1 (block 2,0)	0.0	1.000	1336.32, 0.0, 601.92
4	U1 (block 0,1)	601.92	4.000	0.0, 668.16, 601.92
5	U1 (block 1,1)	601.92	2.000	668.16, 668.16, 601.92
6	U1 (block 2,1)	601.92	1.500	1336.32, 668.16, 601.92
7	U1 (block 0,2)	1203.84	4.000	0.0, 1805.76, 601.92
8	U1 (block 1,2)	1203.84	5.000	668.16, 1805.76, 601.92
9	U1 (block 2,2)	1203.84	2.500	1336.32, 1805.76, 601.92
10	U1 (block 0,3)	1805.76	4.000	0.0, 2407.68, 601.92
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12	U1 (block 2,3)	1805.76	3.000	1336.32, 2407.68, 601.92
13	U1 (block 0,4)	2407.68	4.000	0.0, 3009.6, 601.92
14	U1 (block 1,4)	2407.68	6.000	668.16, 3009.6, 601.92
15	U1 (block 2,4)	2407.68	8.000	1336.32, 3009.6, 601.92

3D-IC Thermal Analysis: *Enable Thermal Through Design Cycle*

As design matures



Feasibility Analysis – *Accurate/early enough for floor planning decisions*

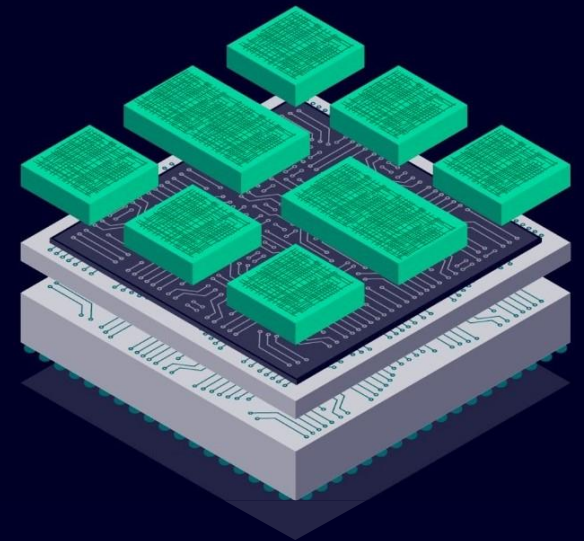
- Calibre 3Dthermal is easy to use for system designer
 - Calibre interface
 - Simplified setup compared to CFD tools/Automated setup using i3D
- Die GDS is not 100% ready – model as silicon
- i3D enables generation of “early” power map
- i3D enables thermal map overlay to visualize effect on floorplan

Sign off Analysis – *“die level” focus*

- Insert “accurate” power map after die power analysis
- Die GDS is ready – model using EFP (silicon + metals/TSVs)
- Calibre 3DThermal enables electro-thermal simulation

Sign off Analysis – *“system level” focus*

- Use thermal models from Calibre 3DThermal as input to Simcenter FloTherm (die + Package + PCB)

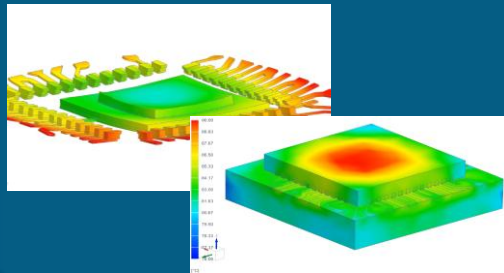


The System Designer Challenge: *Summary*

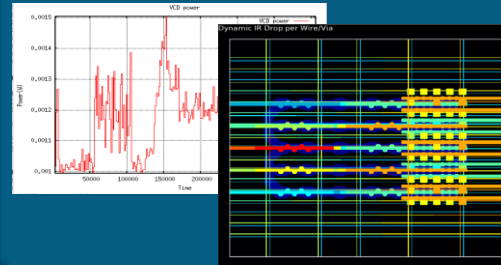
Innovator3D IC as a Multiphysics Cockpit

- An automated setup generation for every respective tool
 - i3D generates setup for mPower and Calibre 3DThermal (and more!)
- Multiphysics tools with the “IC” look & feel (Calibre-based)
- i3D/Calibre allows early vs. sign off analysis

Stress Analysis



Electrical Analysis

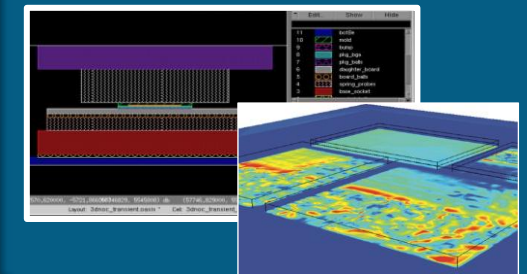


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Thermal Analysis





Q&A